Regular paper http://dx.doi.org/10.13067/JKIECS.2014.9.7.747

Decoupled Plasma Nitridation에 의한 Flicker 노이즈 개선에 관한 연구

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A study on Flicker Noise Improvement by Decoupled Plasma Nitridation

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요 약

본 논문은 0.13um 기술의 디자인을 10% 축소하는데 기존의 로직 디바이스만의 축소와는 달리 로직뿐 아니라 입, 출력 회로의 축소에 관한 것이다. 게이트 산화막(1.2V)을 decoupled plasma nitridation(DPN) oxide로 변경함으로써 flicker 노이즈를 축소 전 공정에 비해 1/3-1/5배 감소됨을 확인하였다. 또한, 축소에 의한 피할 수 없는 문제는 일반적인 metal insulator metal(MIM)의 캐패시터 문제이다. 이를 해결하기 위하여 20% 높은 MIM 캐패시터(1.2fF/㎛^{2})를 개선하고 그 특성을 평가하였다.

ABSTRACT

This paper relates 10% shrink from 0.13㎛ design for logic devices as well as input and output (I/O) circuits, different from the previous shrink methodologies which shrink only core device. Thin gate oxide was changed to decoupled plasma nitridation(DPN) oxide as a thin gate oxide (1.2V) to reduce the flicker noise, resulting in three to five times lower flicker noise than pre-shrink process. Unavoidable issue by shrink is capacitor for this normally metal insulator metal (MIM). To solve this issue, 20% higher unit MIM capacitor (1.2fF/㎛2) was developed and its performance were evaluated.

키워드

Flicker Noise, Gate Oxide, Shrink
Flicker 노이즈,게이트 산화막, 축소

Ⅰ. Introduction

As the requirement for cost down by increasing the number of semiconductor chips within wafer, the scaling trend becomes accelerated in process technology. However, the jump to the new technology such as from 0.13μm to 90㎚ or 65㎚ technology is extremely challenging in terms of development cost and resources. To overcome this problems, the shrink technology has been adopted by many chip makers. The target is spice performance matching after shrink (normally 10%) to the performance of pre-shrink, which is very challenging. That is the reason why the shrink

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접수일자 : 2014. 05. 30 심사(수정)일자 : 2014. 06. 23 게재확정일자 : 2014. 07. 11

technologies have been related to core transistors only excluding input and output (I/O) transistors, because the I/O shrink is much more challenging.

Operation voltage for core logic is 1.2V and for I/O circuit is 3.3V. We found many barriers by the shrink in terms of process, devices and reliabilities.

First, there were special requirements to be improved for the existing pre-shrink 0.13μm technology such as gate oxide integrity (GOI) especially for flicker noise[1-2]. The thick gate oxide is exposed to cleaning chemical during thin gate oxide formation process in dual gate process of core and I/O. It was found that the GOI is very sensitive to the chemical. This paper suggests process to improve the GOI. Another special request for this shrink process was flicker noise which was very critical in analog circuit or RF circuit especially. The root cause of the flicker noise is nitrogen between Si and gate oxide interface, causing interface trap (Q_{it})[3-4]. New thin gate oxide scheme was proposed to locate the nitrogen between gate oxide and gate poly, making the Q_{it} far away from carrier path in channel, in stead of the Si and gate oxide interface, near to carrier path, to reduce this flicker noise.

Second, the shrink reduces the total metal insulator metal (MIM) capacitance and can't be recovered without 20% increasing unit capacitance. For this, 20% higher unit MIM capacitor (1.2fF/μm^2) than existing 1.0fF/μm^2 MIM was proposed and its performance were evaluated.

II. Experimental

2.1 Flicker noise improvement for thin transistor

Decoupled plasma nitridation (DPN) as gate oxidation in stead of rapid thermal nitridation oxide (RTNO) can reduce the nitrogen in Si-SiO_2. The DPN process changes the nitrogen location from Si-SiO_2 to SiO_2-Poly-Si interface far from the Si-SiO_2 interface. The DPN process flow is as follows; Oxidation using rapid thermal oxidation (RTO) and then nitridation using nitrogen plasma in DPN reactor and then rapid thermal anneal (RTA) with 1100℃. The detail condition is as follows; 200sccm N_2, 300W, 20mT, 90rpm of stage rotation, 25sec. If skip or reduce the RTA temperature, V_{th} is seriously unstable due to the plasma damage on oxide. The RTA is for the plasma damage curing.

2.2 Higher MIM unit capacitor development

To meet the 20% higher unit capacitance, different thinner nitride dielectric thickness was evaluated to find the best thickness target. The nitride thickness should be reduced from 650Å to 550Å to increase the unit capacitance from 1.0 to 1.2fF/μm^2. This optimization of thickness was determined through correlation check. If the thickness reduces, the possibility of nitride punch through during the top electrode etching increases, requiring the etching target optimization also. The new MIM characterization was done for breakdown voltage, leakage, temperature coefficient of capacitance(T_{CC}) and voltage coefficient of capacitance(V_{CC}).

III. Results and Discussion

3.1 Flicker noise improvement

Flicker noise improvement for thin transistor using decoupled plasma nitridation process as a thin gate oxide in stead of NO annealed gate oxide using RTO process(RTNO).

The random telegraph signal (RTS) noise distribution according to the flicker noise mechanism of source drain current (I_{DS}) as shown in Fig. 1.

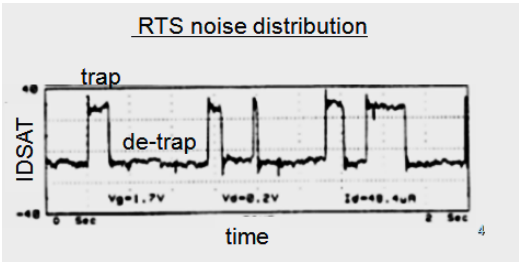


Fig. 1 RTS noise distribution according to the flicker noise mechanism

The new gate oxide process using DPN changes the nitrogen distribution from Si-SiO_2 interface to SiO_2-Poly Si interface as shown in Fig. 2[5-6].

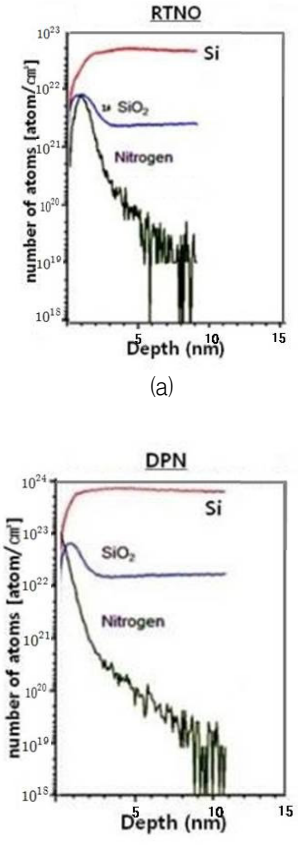


Fig. 2 Nitrogen SIMS profile difference along the Si and gate oxide interface between RTNO and DPN gate oxide (a) RTNO (b) DPN

As a result, flicker noise for 1.2V n-MOS, most sensitive to the flicker noise, was significantly improved by five and three times in sub threshold and linear, respectively as shown in Fig. 3. The change of nitrogen location shift the electrical gate oxide thickness and V_{th} by deactivating boron in surface channel, requiring adjustment of implant condition to match the spice parameters[7-8].

In this paper, we able to improve flicker noise by DPN process. In addition, the phase noise in voltage controlled oscillator(VOC) circuit is known to be significantly improved by the flicker noise improvement[9].

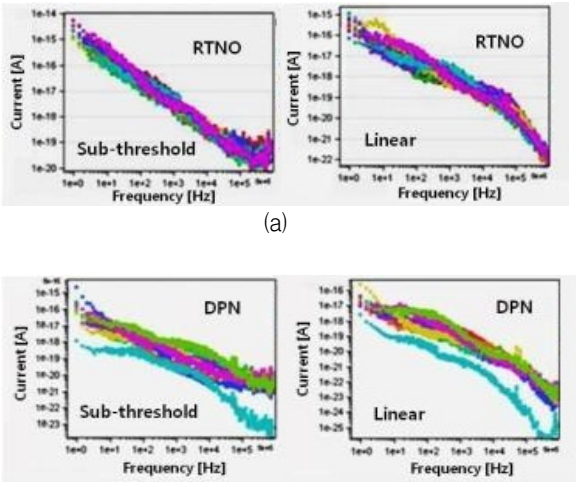


Fig. 3 Flicker noise performance difference between RTNO and DPN as a gate oxide process (a) RTNO (b) DPN

Except this DPN process, flicker noise can be suppressed by using F implant in LDD implant step. The F diffuses into poly by high diffusion rate and cures Si dangling bonds, the source of charge trap sites, in Si surface. F implant slightly shifts the device performance by increasing gate oxide thickness [10]. The other method is to increase N-H alloy anneal time or temperature. But, higher temperature can cause the device shift [11].

And, if increase final passivation nitride, flicker noise can be suppressed by increasing hydrogen inside the nitride. More hydrogen inside nitride can cure more Si dangling bonds after N-H alloy anneal [12].

3.2 Higher MIM unit capacitor (1.2fF/μm^2) development

Dielectric nitride 550Å was found to meet the target 1.2fF/μm^2 as shown in correlation curve, Fig. 4, and the MIM performance also found to be comparable to 1.0fF/μm^2 before shrink as shown in Table 1.

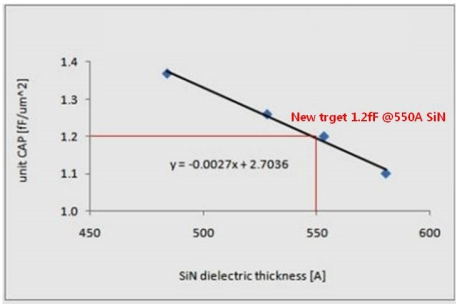
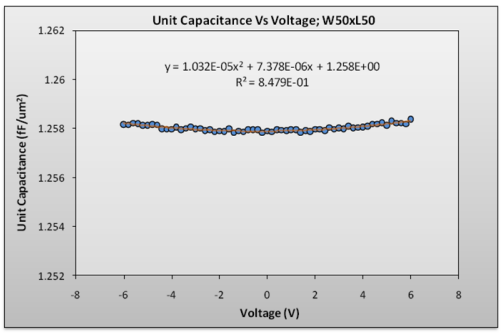


Fig. 4 Correlation between dielectric nitride thickness and unit MIM capacitance

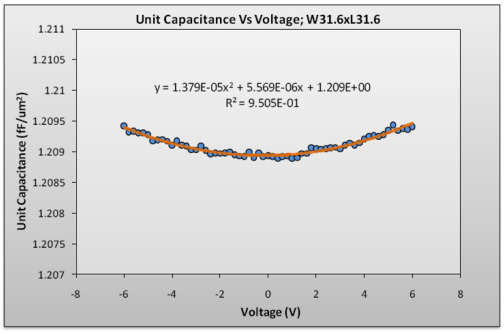
Table 1. MIM capacitor performance comparison between 1.0fF/μm2 and 1.2fF/μm^2

Parameter	1.0fF/μm^2 (before shrink)	(1.2fF/μm^2 (After shrink)		Spec
		Dual MIM	Single MIM	
Leakage [A]	1.9E-13	2.5E-13	1.0E-14	25E-09
BV @1㎂ [V]	57	30	40	>10V
$T_{C}1$ [ppm/℃]	28.4	51	55	<100
$T_{C}2$ [ppm/℃^{2}]	0.13	-0.004	0.05	-
$V_{CC}1$ [ppm/℃]	9.93	5.9	4.6	50
$V_{CC}2$ [ppm/℃^{2}]	6.24	8.2	11.4	10

As in Table 1, the various electrical parameters after shrink could be confirmed that satisfies a specification.



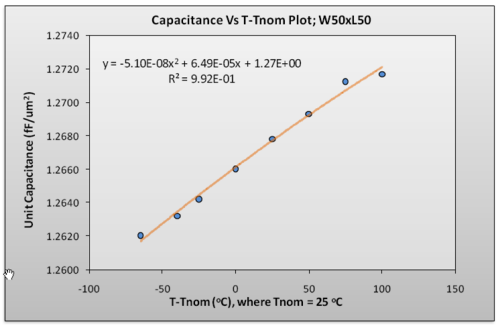
(a)



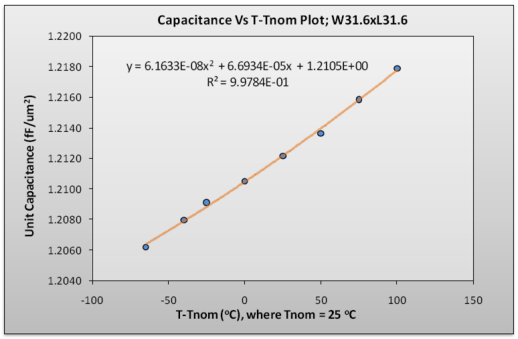
(b)

Fig. 5 VCC performance for 1.2fF/μm^2 of (a) dual and (b) single MIM

The voltage coefficient of capacitance(V_{CC}) and temperature coefficient of capacitance(T_{CC}) perfo-rmance of the new MIM were also evaluated as shown in Fig. 5 and Fig. 6 and found to be quite satisfactory performance.



(a)



(b)

Fig. 6 TCC performance for 1.2fF/μm^2 of (a) dual and (b) single MIM

Ⅵ. Conclusions

This study found that proposed gate oxide by plasma nitrided oxide scheme reduced the flicker noise. The flicker noise improvement using the new shrink process showed much better performance than pre-shrink process, which makes the new shrink process very promising for device application. By 10% shrink, total capacitance loss by 20% in capacitor is inevitable. For MIM, unit capacitance should be increased from 1.0fF/μm^2 to 1.2fF/μm^2 by optimizing dielectric nitride. We confirmed that optimized gate oxide and dielectric nitride to match the DC parameters of pre-shrink matched them within 5%.

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