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# Digital Controller Candidate for Point-of-load Synchronous Buck Converter in Tri-mode Mechanism

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## Abstract

A digital controller with a low-power approach for point-of-load synchronous buck converters is discussed and compared with its analog counterpart to confirm its feasibility for system integration. The tri-mode digital controller IC in 0.35 μm CMOS process is presented to demonstrate solutions that include a PID, quarter PID, and robust RST compensators. These compensators address the steady-state, stand-by, and transient modes according to the system operating point. An idle-tone free condition for Σ–Δ DPWM reduces the inherent tone noise under DC-excitation. Compared with that of the traditional approach, this condition generates a quasi-pure modulation signal. Experimental results verify the closed-loop performances and confirm the power-saving mechanism of the proposed controller.

**Key words:** CMOS integrated circuit, DC–DC converter, Digital control, Digital pulse width modulator, System on-chip

## I. INTRODUCTION

Drivers, power switches, passive components, and controllers are the building blocks of low-power DC–DC converters. Integrating these building blocks into a single chip has become possible with the development of modern semiconductor technologies. This trend has facilitated the emergence of power supply on-chip (PwrSoC), the application of which covers the typical operations of battery-powered embedded systems. Some PwrSoCs require high switching frequency at multi-MHz to maintain a relatively small size of on-chip and accompanying passive components. Meanwhile, this componentreduce the additional losses caused by the increase in switching frequency to ensure low power consumption .

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Two solutions can be used to implement a controller in PwrSoC. Digital control is less sensitive to external perturbations, such as process, voltage and, temperature variations, than analog control . The former enables effective but complex control strategies to improve dynamic performance. Moreover, the digital controller design cycle can be accelerated by using available electronic design automation (EDA) tools. The verified digital controller code at the register transfer level (RTL) is an intellectual property (IP) core that can be reused in different technologies. Therefore, digital control is becoming a potential alternative for its analog counterpart [1]-[8].

Scaling semiconductor technologies improves controller power efficiency from the digital designer viewpoint in creating the PwrSoC prototype. Therefore, the power consumption of a digital controller must be compared with that of analog controllers to evaluate the feasibility for application to PwrSoC. This study proposes a power-aware digital controller devoted to PwrSoC. On the basis of the experimental results from a 0.35 μm test chip that underwent a CMOS process, we illustrate a power assessment model with suggested feasible applications.

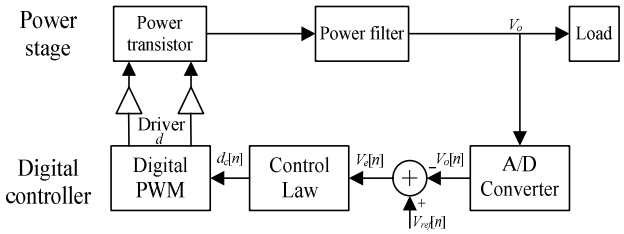


Fig. 1. Schematic diagram of synchronous DC–DC voltage regulator under digital control.

Fig. 1 shows a typical digitally controlled synchronous DC–DC voltage regulator. The feedback loop is composed of an analog-to-digital converter (ADC), a digital control law, and a digital pulse width modulator (DPWM). ADC is traditionally implemented through windowed-based techniques [9], [10], which are not within the scope of this paper. Another issue is generating high-frequency, high-resolution DPWM signals to satisfy the accuracy requirement for the converter output, to ensure low system clock frequency, and to achieve reasonable power consumption [11].

The performance of dedicated compensators is critical to conversion efficiency. An ideal compensator operates well in both static and transient states, as well as performs with a relatively simple physical implementation. Most existing digital controllers are designed by using linear PID control [9], [12], [13]. Implementing linear compensators in a field programmable gate array (FPGA) or application specific integrated circuit (ASIC), notably the voltage-mode PID controller, is beneficial for hardware resources. However, performance generally depends on operating conditions; the presence of parasitic elements, time-varying loads, and variable supply voltages can degrade control performance. Robust RST control has been proven efficient against load, reference, and quantization variation [14]. R – S – T refers to each polynomial to be deduced by the design procedure. Based on an offline tuning polynomial algorithm, RST control outperforms the PID controller but requires more hardware resources and consequently has higher power consumption.

This study proposes a tri-mode controller that achieves a tradeoff between dynamic response and power consumption. For high dynamic performance, RST control is applied in the transient mode, PID control is applied in the steady-state mode, and PID compensator is applied in the stand-by mode. The appropriate parameters are tuned to ensure that the clock frequency is below the switching frequency.

With sufficient resolution achieved by using the noise-shaping concept, an effective DPWM solution is achieved through a Σ–Δ modulator over several switching periods. Compared with delay-line methods, this solution is achieved without sacrificing hardware resources [9], [15], [16]. However, slow convergence occurs because of low-frequency periodic behavior in the lower order Σ–Δ DPWM This behavior is also known as idle-tone, which produces low-frequency noise in the power stage [9]. An idle-tone detection function is presented to detect the idle-tone sensitive binary word $d_c[n]$ (refer to Fig. 1). The results of pre-verification ensure an idle-tone free Σ–Δ DPWM.

An IC controller implements the proposed tri-mode control strategy for buck converter with the use of a top-management finite state machine. Flexibility is achieved by integrating PID and robust RST control to reject load current variations. The proposed DPWM is also integrated onto the chip. The experimental results show that the tri-mode compensator with idle-tone free DPWM demonstrates the effective power consumption model of the digital controller. This model can estimate digital controller power consumption and even determine the effect on PwrSoC power efficiency for a given output power as switching frequency is increased.

This paper is organized as follows: Section 2 provides details on the proposed tri-mode digital control. Section 3 describes an idle-tone free Σ–Δ DPWM. Section 4 discusses the experimental results on the IC controller. Section 5 concludes the study.

## II. TRI-MODE DIGITAL CONTROL

PwrSoC requires a high-performance digital compensator with low power consumption. Therefore, a tri-mode controller is proposed to minimize power consumption during controller operation in the steady-state and stand-by modes. This controller also achieves efficient dynamic response when external load features are transient. PID control and robust RST control are adopted to realize tri-mode control.

### *A. PID Control*

A discrete-time PID controller can be written as

$$\begin{aligned} d[n] &= a_1 d[n-1] + a_2 d[n-2] \\ &\quad + b_0 e[n] + b_1 e[n-1] + b_2 e[n-2] \end{aligned} \tag{1}$$

where $d[n]$ is the PWM output discrete value; $e[n]$ is the error signal discrete value between reference voltage $V_{ref}$ and regulated output $V_o$; $d[n-i]$ and $e[n-i]$ are respectively the PWM output and error values at $i^{th}$-cycles prior to the current cycle; and $a_1$, $a_2$, $b_0$, $b_1$, and $b_2$ are control parameters determined by a pole assignment method.

### *B. Robust RST Control*

Compared with PID control, robust RST control enables the consideration of different dynamics for reference tracking and disturbance rejection. An RST controller achieves significant output disturbance rejection while maintaining

satisfactory robustness. The structure of an RST-controlled buck converter system is presented in Fig. 2.

If In transfer function $P(z)=\frac{B(z)}{A(z)}$, $B(z)$ and $A(z)$ are polynomials. This function describes the discrete time switched-mode power supply (SMPS) model. Thus, the sensitivity function can be expressed as

$$\begin{aligned} S_{yy} &= \frac{A(z)S(z)}{A(z)S(z)+B(z)R(z)} \\ S_{yb} &= \frac{-B(z)R(z)}{A(z)S(z)+B(z)R(z)} \\ S_{yu} &= \frac{B(z)S(z)}{A(z)S(z)+B(z)R(z)} \end{aligned} \quad (2)$$

The same denominator in (2) can determine closed-loop poles. Knowledge of acceptable disturbances leads to designing RST control in terms of pole and zero assignments. Some fixed parts can be specified for polynomials *S(z)* and *R(z)*. For example, a pole for *z*=1 in *S(z)* is needed for static error elimination to ensure output accuracy. Closed-loop poles are chosen to filter effects in certain frequency regions or improve robustness of the closed-loop system. For output disturbance at pulsation $\omega_c$ (output filter corner frequency), efficient disturbance attenuation is achieved when $S_{yy}$ gain is reduced. However, we observed that a large attenuation of $S_{yy}$ at $\omega_c$ results in a large area of $S_{yy}$ over zero value, which increases the maximum value of $S_{yy}$. Given that the maximum value of $S_{yy}$ is inversely proportional to the modulus margin $\Delta M$, large output noise rejection degrades robustness. Fig. 3 describes the aforementioned sensitivity functions of a robust RST controller. The gain of $S_{yy}$ at $\omega_c$ (15 KHz) is -41 dB.

The robust RST control can be written as:

$$\begin{aligned} d[n] = {} & t_o w[n] + t_1 w[n-1] + t_2 w[n-2] \\ & + t_3 w[n-3] - r_0 y[n] - r_1 y[n-1] \\ & - r_2 y[n-2] - s_1 d[n-1] - s_2 d[n-2] \end{aligned} \quad (3)$$

where $d[n]$, $w[n]$, and $y[n]$ are PWM output discrete value, reference voltage $V_{ref}$, and regulated output $V_o$; $d[n-i]$, $w[n-i]$, and $y[n-i]$ are corresponding values at the $i^{th}$-cycles prior to the current cycle; and $t_0$, $t_1$, $t_2$, $t_3$, $r_0$, $r_1$, $r_2$, $s_1$, and $s_2$ are optimized control parameters.

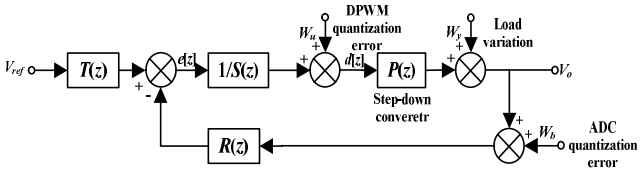


Fig. 2. Block diagram of an RST scheme.

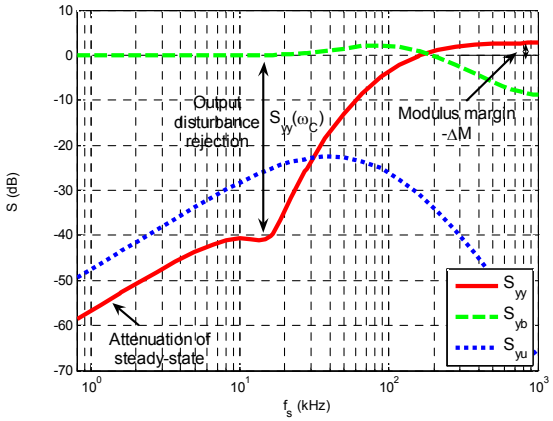


Fig. 3. Sensitivity function of a robust RST controller.

### C. *Comparative study of PID Control and RST Control*

A fixed-point simulation is performed in Matlab by using a non-ideal buck converter model written in S-function. All circuit parameters have the same values as the values on the test board. Default switching frequency is $f_s = 2\text{MHz}$, filter inductor is $L = 4.7\mu\text{H}$, filter capacitor is $C = 22\mu\text{F}$, and nominal load is $R_L = 5\Omega$. Fig. 4 presents the output-to-output sensitivity function in the frequency domain for RST control and PID control to quantify control dynamics, robustness, and output noise (load variation) rejection properties.

The gain of $S_{yy}$ at corner frequency $f_c = 13\text{KHz}$ determines output disturbance rejection in the SMPS test vehicle used in the experiment. Low $S_{yy}$ gain (13 KHz) equates to efficient output disturbance attenuation. Moreover, the maximum value of $S_{yy}$ corresponds to the inverse value of modulus margin $\Delta M$; $\Delta M$ is the minimum distance of the open-loop transfer function with respect to the critical locus (-1) in the Nyquist plan.

The modulus margin quantifies robustness with respect to modeling uncertainties. Fig. 4 shows that $S_{yy}$ gain at 13 KHz for RST control is -41 dB, whereas that for PID control is -20 dB. PID and RST exhibit similar robustness ($\Delta M_{RST}$=0.88, $\Delta M_{PID}$ =0.87).

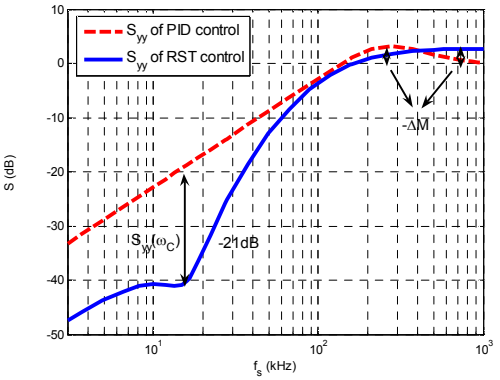


Fig. 4. $S_{yy}$ sensitivity function for RST control and PID control.

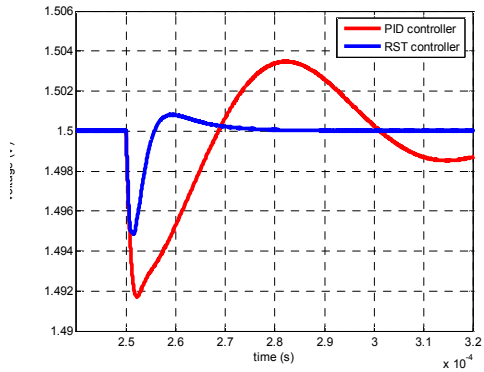


Fig. 5. Simulation of RST control and PID control in a load transient from 0.3 A to 0.45 A.

Based on the aforementioned test-bench, a closed-loop fixed-point simulation is performed to compare the performances of the two compensators. Fig. 5 shows the simulation performance results of RST control and PID control in a load transient (0.3 A to 0.45 A) to ensure continuous conduction mode (CCM) operation. Load transient response of RST control is superior to that of PID control; RST control offers shorter rise time and produces smaller undershoot.

### *D. Tri-Mode Compensator Operation*

A comparative study shows that RST control exhibits better dynamic behavior against load variation than PID control under similar robustness with respect to modeling uncertainties. However, RST control requires a complex implementation of extra combinational cells across the data-path according to (1) and (3). The primary task of a compensator is to maintain a stable output voltage in an acceptable error range when the buck converter operates in steady-state (i.e., the external load is stable). Thus , a simple control law, such as PID control, is preferable for control performance. Moreover, using PID control during steady-state satisfies performance specification and relaxes the tight algorithm computation requirement, further reducing power consumption.

Many portable devices are in idle state (i.e., stand-by mode). Thus, quarter PID control is proposed. Quarter PID control and PID control have the same structure when applied under normal operations, but quarter PID control is clocked at a quarter of the switching frequency. That is, quarter PID control updates its computation every four periods.

The proposed tri-mode compensator in Fig. 6 consists of a mode arbitration logic that switches among three modes: robust RST control for the transient mode, PID control for the steady-state mode, and quarter PID control for the stand-by mode. The tri-mode compensator depends on an external activity signal *m*, which is normally obtained by a sensor to select an appropriate mode. Digital functions inside any low-powered system can issue such a signal. For example, the activity signal in a mobile phone is set to *m*=0 when in stand-by mode and *m*=1 when in normal operation. Change among the three states is performed through mode arbitration logic. The block function detects the activity signal state and selects the corresponding control mode. The tri-mode control (Fig. 7) is designed to eliminate potential stability problems related to dynamic mode switching between different control modes. The mode change procedure is detailed in Fig. 8. Tuning times $\Delta t_1$ and $\Delta t_2$ in RST control can be adjusted to satisfy practical application needs during the transient state. These two tuning times can be implemented using two ladders of D-flip-flops arbitrated by activity signal *m* (Fig. 6). For example, constant tuning time $t_{tune1}$ is set for $\Delta t_1$ and $t_{tune2}$ for $\Delta t_2$. Voltage error $e[n]$ obtained from reference voltage $V_{ref}[n]$ and regulated output $V_o[n]$ is normalized in the discrete-time format; the maximum allowed voltage error is set as threshold $e_{th}$. In the experimental test-bench, $e_{th}$ is set to 15 mV (1% of the nominal output voltage). Fig. 6 shows that $e_{th}$ is compared with current error signal $e[n]$. Fig. 7 and 8 shows that logic-glue ensures correct functions and timing sequences to enable the two controls. A frequency divider provides a quarter in the system clock of PID control in stand-by mode. Detailed operation of the tri-mode compensator is described as follows:

1) After initialization of SMPS, the compensator is assumed to be in stand-by mode and quarter PID is used to regulate output voltage; the compensator is kept in this state until output variation is larger than error threshold (i.e., $e[n] > e_{th}$ (normalization) or an activity signal *m*=1 is detected). Then, the compensator switches to procedure 2;

2) The compensator switches to transient mode using the RST control law to regulate output voltage of SMPS. This control mode is maintained long enough ( $\Delta t_1 > t_{tune1}$ ) to achieve $e[n] < e_{th}$ ; SMPS then enters a steady-state mode;

3) The compensator selects PID control in steady-state mode to regulate output voltage. This state is maintained until

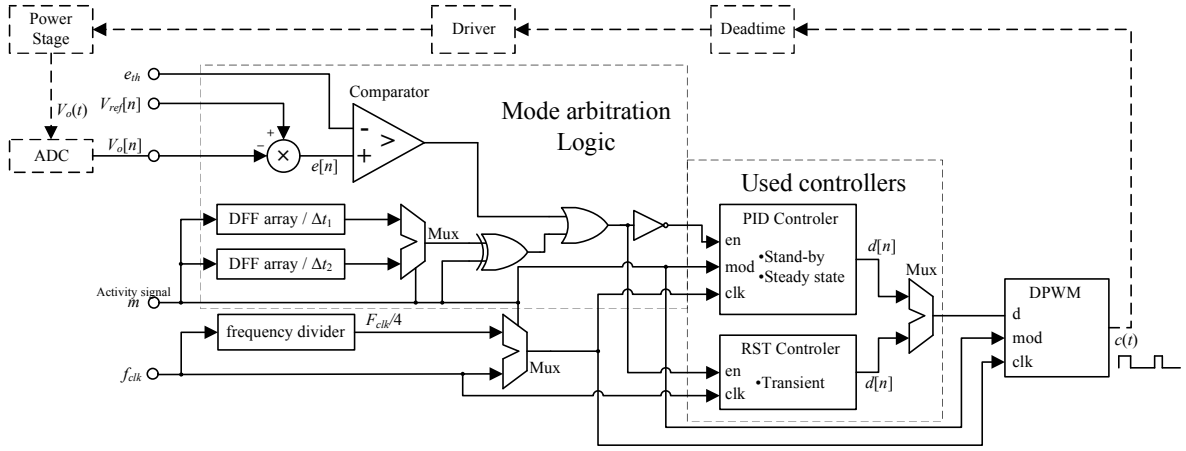


Fig. 6. Block diagram of tri-mode controller.

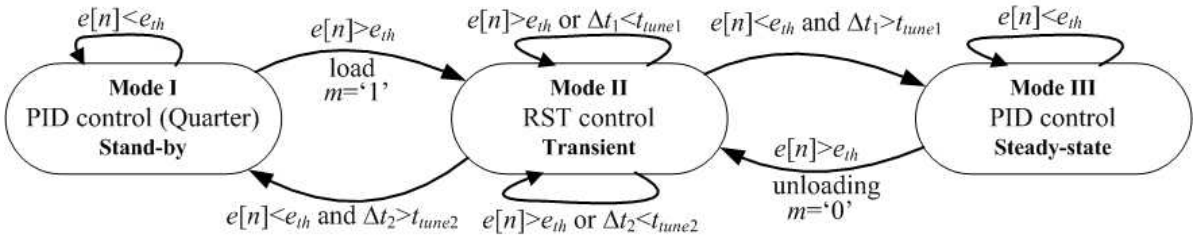


Fig. 7. State-switch diagram of mode arbitration block.

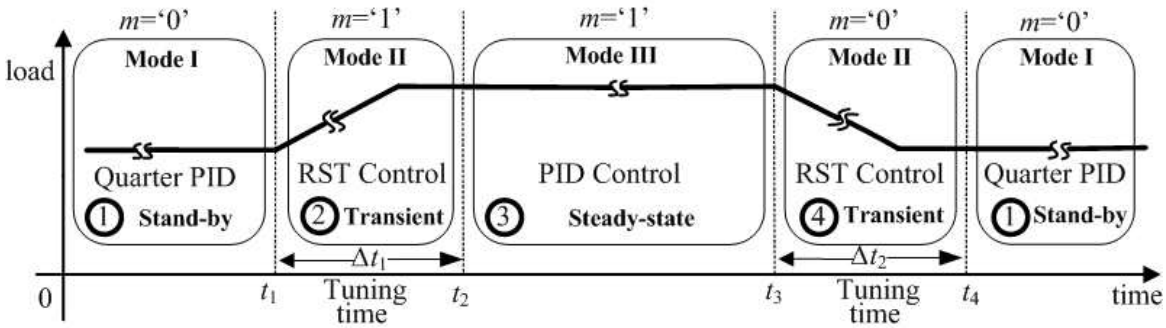


Fig. 8. Mode change procedure of tri-mode controller.

output variation is larger than error threshold (i.e., $e[n] > e_{th}$ or an activity signal $m$=0 is detected);

4) RST control is selected again for regulating unloading in the transient mode. This control mode is held long enough ($\Delta t_2 > t_{tune2}$) until $e[n] < e_{th}$ is achieved. Unloading is then finished, and SMPS once again reaches steady-state mode;

5) The controller stays in an unloaded situation after the transient mode and is set in stand-by mode; then, the controller is back to procedure 1 to wait for the next operation cycle.

Compared with the dual-mode controller designed with a simple hysteretic logic method, the proposed controller offers a more flexible selection to reduce the energy consumption of the control algorithm with three modes. With the tri-mode controller, quarter PID control updates the whole control-law computation under-sampled mode at $1/(4 \cdot f_s)$ frequency. This feature reduces energy consumption relative to stand-alone PID and RST controllers.

### *E. Stability During Mode Change*

According to (1) and (3), current period control output $d[n]$ is derived on the basis of the state variables in previous cycles. For example, PID controller requires state variables from at least two cycles prior to the current period. If no operation overlap in the time domain is found, then the

controller generates a large offset in the first period after mode change. A pre-post-operation in transient mode is proposed during mode change to overcome this difficulty.

Fig. 8 shows that robust RST control is next to any adjacent control. For example, RST control operation can manually extend to quarter PID control interval when the mode changes from stand-by to transient. This extension should be long enough to set up a stable closed-loop RST control response. Hence, RST control can be regarded as pre-operation. By contrast, RST control extends to PID interval to perform post-operation when the mode changes from transient to steady-state. In the second situation, several periods during the mode change are sacrificed to avoid potential instability. Therefore, two overlaps requiring only small modifications to hardware configuration are suggested (Fig. 6):

1) Extend tuning time $\Delta t_1$ and $\Delta t_2$ to $\Delta T_1$ and $\Delta T_2$ respectively, according to the experimental results satisfying the stability criterion during mode change;

2) Permit two controls to operate simultaneously;

3) Add another arbitrary module to select the Mux output in the used controllers block (Fig. 6) following the timing sequence discussed above.

The tri-mode controller offers a flexible selection with the three modes for saving power consumption. With the tri-mode controller, quarter PID control updates the whole control-law computation in stand-by mode at a switching frequency of $f_s/4$. This feature reduces power consumption, compared with stand-alone PID or RST controllers.

## III. Spur-Tone Free Condition for Σ–Δ DPWM

The proposed tri-mode controller output must be converted to a PWM pattern for further use. This section proposes an effective guideline to design a Σ–Δ DPWM, achieving efficient performance and maintaining acceptable power consumption.

The error-feedback model of Σ–Δ modulator is preferable if DPWM is the design target. The corresponding transfer function is given by:

$$\begin{aligned} V(z) &= STF \cdot D(z) + NTF \cdot E(z) \\ &= D(z) + (1 - H_e(z))E(z) \end{aligned} \tag{4}$$

where $D(z)$ is the input signal. The error $E(z)$ is the difference between range limited input and quantization block $V(z)$ output. $E(z)$ is then compared with input voltage by using the delay module $H_e(z)$; and *STF* and *NTF* are the signal transfer function and noise transfer function, respectively. The delay module is easily set to achieve

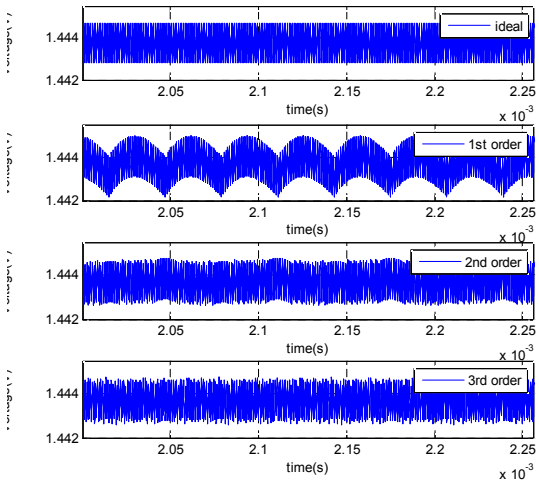


Fig. 9. Power converter output regulated by Σ–Δ DPWM of different orders.

different orders of noise-shaping effects. For example, $H_e = z^{-1}$ assures a first-order noise-shaping effect, whereas $H_e = z^{-1}(2 + z^{-1})$ assures a second-order noise-shaping effect.

A fixed-point simulation model is used to interpret the higher order DPWM advantage; the same parameters as illustrated in Section 2.3 are used. For example, input binary word in decimal format is 1025 using an 11-bit DPWM with 5-bit Σ–Δ modulator. Fig. 9 shows power converter output regulated by a Σ-Δ DPWM with corresponding orders, as well as by an ideal 11-bit DPWM. Compared with higher order Σ–Δ DPWM, regulated power converter output with first-order DPWM exhibits obvious periodic oscillation. This phenomenon is reduced by the second- and third-order modulators. Therefore, corresponding oscillation amplitude is reduced with increased Σ–Δ order.

With consideration of the filter response in the power stage, the total noise power of each input binary word is defined as the accumulation of power differences between target modulators and references within half of the switching frequency. Thus, an ideal 11-bit DPWM is simulated to provide a reference. Fig. 10 shows the simulation results of in-band quantization noise power versus input binary word. Fig. 10(a) shows three floors exhibiting two types of in-band noise. The central floor is an effective input binary word range floor, constant and symmetrical to the central binary word (1024 in this case). All input under this floor achieves better noise-shaping effects than input on other floors. The other two floors are placed at two ends of the binary word sweep range; hence, they are referred to as "side floors." These floors exhibit weaker noise-shaping effects than the central floor. The following reasons explain the phenomenon:

1) Small enough or large enough input binary words are

prone to introducing saturation into the modulator, which results in repeated low-frequency patterns that appear in converter output;

2) Compared with Σ–Δ a digital-to-analog converter, imperfect low-pass filter in the power stage (second-order for buck converter) deteriorates post-analog filter performance and introduces more serious in-band noise, especially in the side floors;

3) In-band noise has higher amplitude in first-order DPWM than in second-order DPWM, which accounts for the pattern scattering effect.

Fig. 10(b) enlarges the central floor around the central input binary word (from 1015 to 1065), showing that noise peak power always occurs at:

$$I \cdot 2^{n-m} \pm 1 \tag{5}$$

where $n$ is input bit number, $m$ is output bit number, $I \in Z^+$ and $q_{th} \le I \le 2^m - q_{th}$. $q_{th}$ is threshold absolute value in the central floor. Fig. 10 shows a confidence interval obtained from the test-bench. The example requires one side floor length to be at least 12.5% of the total length of input binary word range ( $q_{th} \ge 8$ ).

The minimum noise-shaping effect can be achieved for all modulators with different orders, provided that input binary word is maintained at $I \cdot 2^{n-m}$. All modulators generate the same output pattern without the sensitive periodic sequence. For example, modulated output of all modulators with different orders for input binary word 992 is the same output sequence as {31, 31, … 31}.

Based on the above analysis, a recommended Σ–Δ DPWM design guideline is given as follows:

1) reduce the use of the Σ–Δ modulator to generate higher frequency periodical sequences that are likely to be eliminated by the power filter;

2) A higher order modulator is always preferable to attenuate the idle-tone effect using inherent intensive scatter operations;

3) The estimation in (5) should be performed offline to determine idle-tone sensitive binary words. Corresponding regulated output should not fall into the set of sensitive output.

We use a second-order 5-bit Σ–Δ DPWM to achieve a satisfactory tradeoff between the required system clock and output signal integrity. Nominal DC–DC converter output voltage (1.5V) is normalized as:

$$\frac{V_{ref}}{V_{in}} \cdot 2^{N_{DPWM}} \notin I \cdot 2^{n-m} \pm 1 \tag{6}$$

which satisfies the proposed guideline.

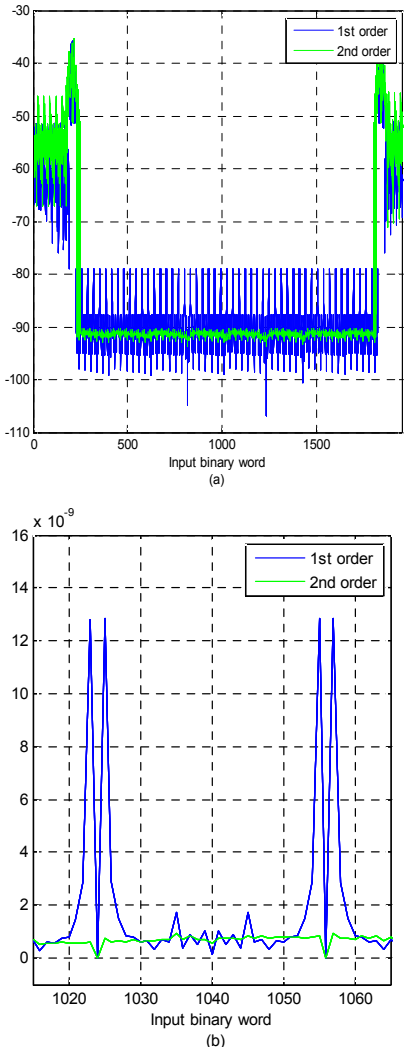


Fig. 10. (a) In-band quantization noise power versus input binary word of first-order and second-order modulators in the buck converter, (b) periodic noise peak around a specific input.

## IV. Experimental Results and Power Consumption Analysis

### *A. Experimental Results*

The proposed tri-mode digital controller is fabricated in a 0.35 μm CMOS process. Fig. 11 shows the chip die photo. The whole chip occupies 4.58 mm × 2.42 mm; RST compensator takes 1.28 mm × 1.31 mm, PID compensator (with embedded DPWM) takes 1.24 mm × 1.27 mm, and stand-alone DPWM takes 0.47 mm × 0.49 mm. Table I summarizes the test-bench specification. A Xilinx XC3S500E FPGA board is used as a motherboard to provide necessary control signals and implement the off-chip mode arbitration function.

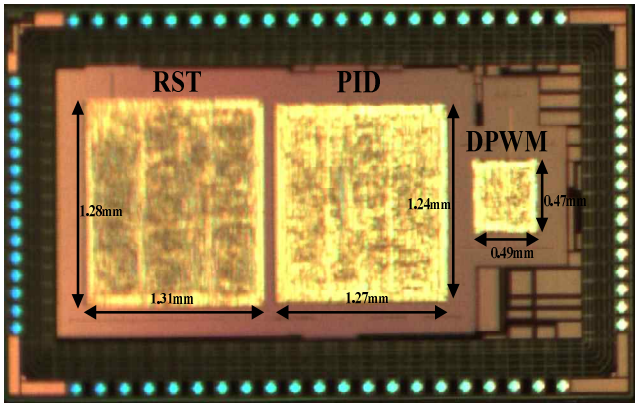


Fig. 11. Die photo of proposed controller.

TABLE I
DESIGN SPECIFICATION OF THE TEST-BENCH

| | | |
|---|---|---|
| $N$ | Number of phases | 1 |
| $V_{in}$ | Input voltage | 3.0 V |
| $V_{ref}$ | Maximum reference voltage | 1.5 V |
| $I_{max}$ | Maximum load current | 0.45 A |
| $f_s$ | Switching frequency | Up to 2 MHz |
| $N_{ADC}$ | ADC resolution | 10-bit |
| $N_{DPWM}$ | Equivalent DPWM resolution | 11-bit |
| $f_{sample}$ | ADC sampling frequency | 1 MHz |
| $\Delta V$ | ADC input range | 2 V |

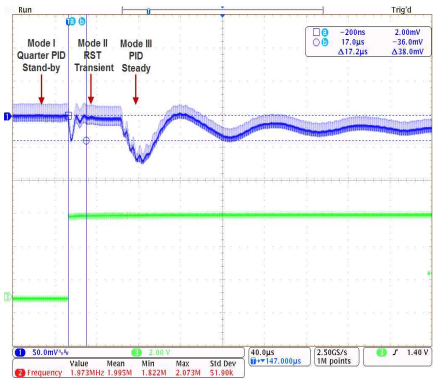


Fig. 12. Output voltage of tri-mode controller at 2 MHz under load transient from 0.3 A to 0.45 A to keep in CCM operation (50 mV/div, 40 µs/div, AC coupling).

Fig. 12 shows the response using the tri-mode controller under the load perturbation scheme in Fig. 8. Fig. 12 describes step 1 to step 3 in Section 2.4 when load current changes from 0.3 A to 0.45 A. $t_{tune1}$ and $t_{tune2}$ are both set to 40 µs to ensure sufficient transient response time according to the dynamic performance of the RST controller. $e_{th}$ is set to $\frac{\Delta V}{2^{N_{ADC}}}$. According to Fig. 12, the tri-mode controller exhibits better dynamic response (153 µs and 200 µs, respectively) than the stand-alone PID controller; however, although the tri-mode controller takes a longer response time than the stand-alone RST controller. Maximum output voltage ripple is 1.8 mV. Power consumption of the tri-mode controller is anticipated to be lower than the stand-alone RST controller or the full-speed stand-alone PID controller; this issue is discussed in the next section.

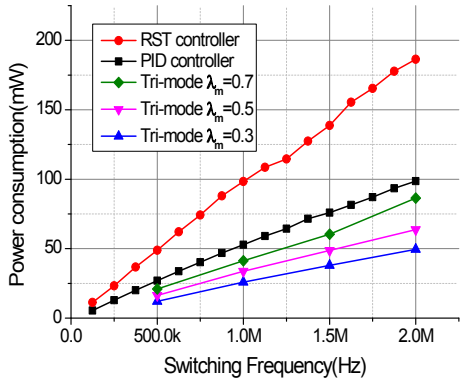


Fig. 13. Power consumption of proposed tri-mode controller compared with stand-alone PID and RST controllers under SMPS switching frequency.

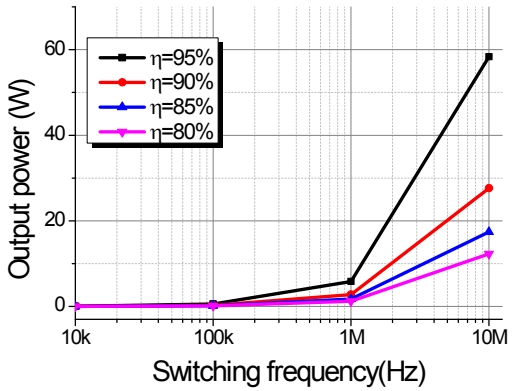


Fig. 14. Anticipated output power versus switching frequency of a buck converter; the tri-mode controller controls the buck converter with switching frequency from 10 kHz to 10 MHz.

### *B. Power Consumption Analysis of Proposed Controller*

The aforementioned test illustrates the acceptable static and dynamic performances of the proposed tri-mode controller with the idle-tone free DPWM. Power consumption is another important assessment parameter influencing overall converter efficiency. The same test-bench is used to perform an experiment illustrating actual power consumption. $t_{tune1}$ and $t_{tune2}$ are maintained at 40 µs. A parameter $\lambda_m$ represents the time ratio of non-stand-by operation mode, that is, the total time of transient mode and steady-state mode. Fig. 13 shows the experimental power consumption of the proposed tri-mode controller with time ratio $\lambda_m$ being 0.3, 0.5, and 0.7. The stand-alone PID controller and the RST controller are also shown for comparison purposes. We take $\lambda_m$=0.5 as an example, which is half the operation time before it falls in

stand-by mode. The power consumption of the tri-mode controller is only 64.5% of that of the PID controller and 34.2% of that of the RST controller at switching frequency of 2 MHz. That is, the power consumption is 32.15 mW/MHz with a supply voltage $V_{dd}$=3.3 V and output voltage $V_o$=1.5 V. $\lambda_m$=0.3 and $\lambda_m$=0.7 result in a power consumption of 24.56 mW/MHz and 42.83 mW/MHz, respectively.

If the power consumption of 24.56 mW/MHz corresponding to $\lambda_m$=0.3 is taken as an example, an SMPS output power range can be evaluated when a given efficiency is targeted. Output power is ideally given by

$$P_{out} = \frac{P_{loss}}{\frac{1}{\eta} - 1} \tag{7}$$

where $P_{out}$ is the estimated output power, $P_{loss}$ is the total amount of dissipated power consumption (including power loss from controllers, drivers, and power switches), and $\eta$ is the normalized power efficiency. According to the conclusion of [17], we assume that digital controller power loss does not account for more than 8% of the total power loss (i.e., $P_{loss}$=307 mW/MHz). Fig. 14 shows the estimated SMPS output power $P_{out}$ with respect to switching frequency and different global power efficiency targets ($\eta$=95%, 90%, 85%, and 80%).

## V. CONCLUSIONS

This study introduces a fully digital IC controller for a low-power, high-switching-frequency buck converter. This controller takes advantage of a proposed idle-tone free Σ–Δ DPWM and tri-mode compensator. The improved DPWM effectively reduces generating idle-tone. An offline parameter calculation guarantees that no hardware resources are required in ASIC. The proposed tri-mode controller addresses transient, steady-state, and stand-by modes by considering power consumption and dynamic performance. The experimental results verify the efficiency of this system-level power saving strategy. Power consumption is only 24.56 mW/MHz when the time ratio of non-stand-by operation mode is 0.3. The IC prototype is accurate and flexible, achieving high power efficiency for low-to-medium power applications.

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## REFERENCES

[1] H. Ahmad and B. Bakkaloglu, "A digitally controlled DC-DC buck converter using frequency domain ADCs," *Proc. IEEE APEC Conf.*, pp. 1871-1874, 2010.

[2] Y. Qiu, H. Liu, and X. Chen, "Digital average current-mode control of PWM DC-DC converters without current sensors," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 5, pp. 1670-1677, May 2010.

[3] F. Luo and D. Ma, "Design of digital tri-mode adaptive-output buck-boost power converter for power-efficient integrated systems," *IEEE Trans. Ind. Electron.*, Vol. 57, No 6, pp. 2151-2160, Jun. 2010.

[4] Y.-F. Liu, E. Meyer, and X. Liu, "Recent developments in digital control strategies for DC/DC switching power converters," *IEEE Trans. Power Electron.*, Vol. 24, No. 11, pp. 2567-2577, Nov. 2009.

[5] D. Fu, S. Wang, P. Kong, Fred C. Lee, and D. Huang, "Novel techniques to suppress the common mode EMI noise caused by transformer parasitic capacitances in DC-DC Converters," *IEEE Trans. Ind. Electron.,* Vol. 60, No. 11, pp. 4968-4977, Nov. 2013.

[6] B.-Y. Chen and Y.-S. Lai, "New digital-controlled technique for battery charger with constant current and voltage control without current feedback," *IEEE Trans. Ind. Electron.*, Vol. 59, No. 3, pp. 1545-1553, Mar. 2012.

[7] F. Gonzalez-Espin, E. Figueres, G. Garcera, R. Gonzalez-Medina, and M. Pascual, "Measurement of the loop gain frequency response of digitally controlled power converters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 8, pp. 2785-2796, Aug. 2010.

[8] Y. J. A. Alcazar, D. de Souza Oliveira, F. L. Tofoli, R. P. Torrico-Bascope, "DC-DC nonisolated boost converter based on the three-state switching cell and voltage multiplier cells," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 10, pp. 4438-4449 , Oct. 2013.

[9] Z. Lukic, N. Rahman, and A. Prodic, "Multibit Σ-Δ PWM digital controller IC for DC-DC converters operating at switching frequencies beyond 10 MHz," *IEEE Trans. Power Electron.*, Vol. 22, No. 5, pp. 1693-1707, Sep. 2007.

[10] J. Zhang and S. R. Sanders, "A digital multi-mode multi-phase IC controller for voltage regulator application," *Proc. IEEE APEC Conf.*, pp. 719-726, 2007.

[11] C.-A. Yeh and Y.-S. Lai, "Digital pulse width modulation technique for a synchronous buck DC/DC converter to reduce switching frequency," *IEEE Trans. Ind. Electron.*, Vol. 59, No. 1, pp. 550-561, Jan. 2012.

[12] E. Zurita-Bustamante, J. Linares-Flores, E. Guzman-Ramirez, and H. Sira-Ramirez, "A comparison between the GPI and PID controllers for the stabilization of a DC-DC buck converter: A field programmable gate array implementation," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 11, pp. 5251-5262, Nov. 2011.

[13] V. Mummadi, "Design of robust digital PID controller for H-Bridge soft-switching boost converter," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 7, pp. 2883-2897, Jul. 2011.

[14] X. Lin-Shi, F. Morel, B. Allard, D. Tournier, J.-M. Retif, and S. Guo, "A digital-controller parameter-tuning approach, application to a switch-mode power supply," *Proc. IEEE ISIE Symp*., pp. 3356-3361, 2007.

[15] S. Guo, X. Lin-Shi, B. Allard, B. Li, Y. Gao, and Y. Ruan, "High-resolution digital PWM controller for high-frequency low-power SMPS," *Proc. EPE Conf.*, pp. 1-9, 2009.

[16] B. Li, S. Guo, X. Lin-Shi, and B. Allard, "Design and implementation of the digital controller for boost converter based on FPGA," *Proc. IEEE ISIE Symp.*, pp. 1549-1554. 2011.

[17] D. Ma, J. Wang, and M. Song, "Adaptive on-chip power supply with robust one-cycle control technique," *IEEE Trans. VLSI Syst.* Vol. 16, No. 9, pp. 1240-1243, Sep. 2008.

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