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Dynamic Paralleling Behaviors of High Power Trench and Fieldstop IGBTs

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Abstract

This paper demonstrates the dynamic behaviors of paralleled high power IGBTs using trench and fieldstop technologies. Four IGBTs are paralleled and standard deviation is adopted to represent the imbalance. Experiments are conducted under three different operation conditions and at different temperatures ranging from -25°C to 125°C. The experimental results show that operation at very low and very high temperatures usually aggravates the switching behaviors. There is a trade-off between the balance and the losses at low temperatures. These results can help in the design of heat sinks in paralleling applications confronting very low temperatures.

Key words: Heat Sink, IGBT, Imbalance,Paralleling Application, Temperature

I. INTRODUCTION

Insulated gate bipolar transistors (IGBT) are gradually gaining popularity in power electronic systems such as wind turbines and solar power inverters, by combining the advantages of both MOSFET and bipolar junction transistors (BJT) [1]-[4]. They show performances from a few hundred watts to megawatts, with a voltage range from a few hundred to several thousand. However, in some conditions requiring high power and a large current, a single IGBT fails to satisfy the needs. The paralleled application of IGBTs is a better alternative for increasing the current range [5]-[6]. In such cases, the paralleled IGBTs should come from the same date and production patch.

In recent years a great deal of attention has been focused on static and dynamic paralleling behaviors. A lot of work has been done to investigate the factors that influence current sharing. The AC output resistance, saturation voltage ($V_{ce(sat)}$), diode forward voltage and gate-emitter voltage (V_{ge}) affect the static current balancing. The DC bus stray inductance, gate-emitter threshold voltage ($V_{ge(th)}$) and gate driver (including the gate loop inductance, gate loop resistance and switching delay time) affect the dynamic current balancing [7]. The junction temperature variance between the paralleling IGBTs, which affects both the static and dynamic current balancing, is mainly addressed. Xuesong Wang suggests that the current imbalance between paralleled IGBTs almost stays the same at a certain surrounding temperature if the relative temperature difference is unchanged, and the static current difference between the paralleled IGBTs increases with the rising relative temperature difference [8]. In addition, the driver matters. Ulrich suggests that the use of individual gate drivers is good for avoiding the coupling effects between the paralleled IGBTs and back to the control signal, while the use of common gate drivers substantially reduces the problems of the timing delay differences and gives solutions for using common mode chokes [9]. In general, a smaller temperature variance and a more symmetric current loop lead to more balanced dynamic and static current sharing [10], [11]. In order to improve the paralleling performance, Parick Hofer presents an active gate-controlled current balancing method to balance the static and dynamic behavior and then the temperature [12]. H. Dehbonei suggests that when IGBTs are applied in parallel, TSH (time sharing) should be used to reduce the stress on the switches while guaranteeing maximum performance in a system [13].

Based on this, the optimization of the layout symmetry and the heat sink is given priority, since it is cost-efficient and easy for engineers to implement. However, there is still a chance that the paralleling behaviors will become uncontrolled when paralleling applications are carried out in some extreme situations. For instance, the ambient temperature falling below O℃ (when the device is located at a high altitude) makes the

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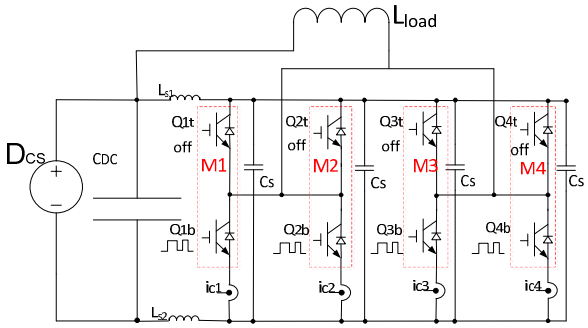


Fig. 1. The topology of the paralleling application.

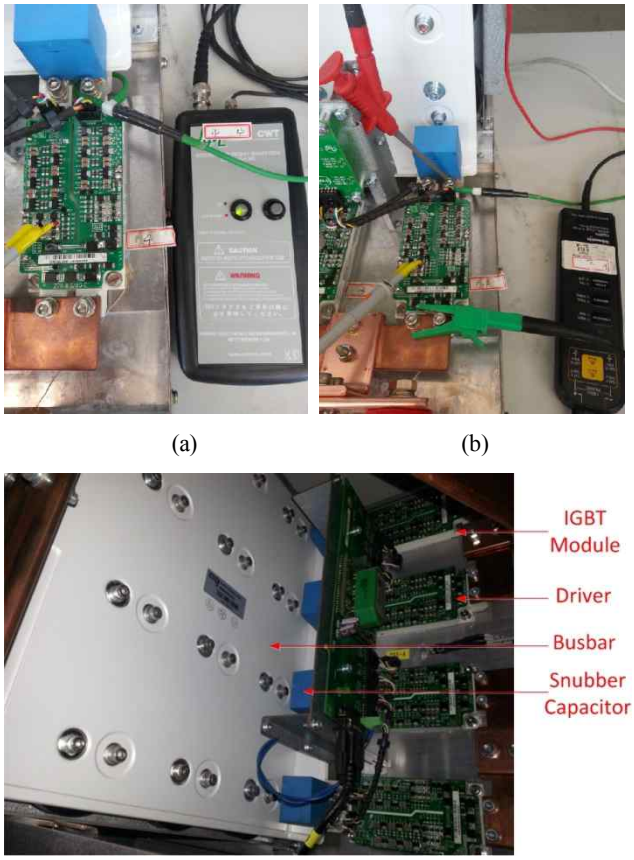
junction temperature of the paralleled IGBTs fall even with self-heating. The low temperature may affect the paralleling behaviors. As a result, predesigned application which only considers decreasing the relative temperature variance in the normal junction temperature may no longer be applicable. On the other hand, the studies mentioned above are all based on punch through (PT) and non-punch through (NPT) IGBTs. They seldom deal with trench and fieldstop IGBTs. Therefore, the behaviors of the paralleling application of trench and fieldstop IGBTs should be investigated.

This paper, aims at discussing the influences of relatively extreme temperatures on paralleling behaviors. It is organized as follows. Part one provides background information. Part two focuses on the setup of the paralleling application of high power IGBTs, and part three presents experiment results. Part four discusses and analyzes these results, and the final part gives some conclusions.

II. Setup of the Experiments

In order to investigate the relationship between the temperature and the behaviors of paralleled trench and fieldstop IGBTs, a topology with four modules is realized as depicted in Fig. 1. Fig. 2 shows the experimental setup.

The IGBT modules are Infineon FF600R12ME4 half bridge modules of 1200V/600A. All of them have identical data codes. The measurements are executed under the following three conditions: 357.5A per module, 820V DC bus voltage; 325A per module, 600V DC bus voltage; 35A per module, 820V DC bus voltage, which are named condition A, B and C, respectively. Condition A is set by the maximum output and maximum voltage for this type of IGBT used in a 500kW inverter. Condition B is set by the datasheet. Condition C is set by the maximum switching speed. Each of these conditions is tested at ambient temperatures of -25°C, 25°C and 125°C, in order to test the paralleling behaviors at very high and very low temperatures. To achieve the specific temperatures, four heaters (800W each) were embedded in a heat sink. Since the IGBT module is integrated with a negative temperature coefficient (NTC) resistor, the temperature in the IGBT can be monitored. In addition, the IGBT's copper base temperature is



(a) (b)

(c)

Fig. 2. The experimental platform. (a) Ic measurement. (b) Vce measurement. (c) The experimental platform.

TABLE I
Test Conditions

Condition	1st Pulse	2nd Pulse	Pulse Off Width
(A) 357.5A/820V	87.2us	10us	10us
(B) 325A/600V	108.4us	10us	10us
(C) 35A /820V	17.1us	10us	10us

monitored by a thermocouple. Before each test, the heater is heated for half an hour to make the NTC resistor temperatures the same. It can be reasonably assumed that the temperatures in the four IGBTs are identical. The test at -25°C is executed in a thermostatic chamber. Before testing, a minimum of half an hour is needed to assure that the temperatures of the IGBTs are the same.

Four modules (M_1, M_2, M_3 and M_4) are tested in this experiment. As in Fig. 1, i_{c1} measures the collector current of Q_{1b}; i_{c2} measures the collector current of Q_{2b}; i_{c3} measures the collector current of Q_{3b}; and i_{c4} measures the collector current of Q_{4b}. All four of these IGBTs belong to different discrete IGBT modules, just as Q_{1a} and Q_{1b} are in the same module. In

addition, the collector-emitter voltages of Q_{1b}, Q_{2b}, Q_{3b} and Q_{4b} are measured.

Tests at high temperatures are only executed at 125°C. Due to the research in [14], this can still reflect a real trend. Hence, this is believed to be sufficient for this paper to be fully illustrative and factual.

The double pulse test is used to extract the dynamic behaviors. Specifically, it is used to extract the turn-off paralleling behavior in the first pulse turn-off, and the turn-on paralleling behavior in the second pulse turn-on. The pulse width is shown in Table I to realize each output condition. While the bottom IGBTs are tested, the top IGBTs are turned off. According to information from Infineon technology, the test parameters and setup parameters are given in Appendix A and Appendix B, respectively.

III. Experimental Results

Since it is not just the current sharing being analyzed, the standard deviation (SD) approach, instead of the traditional current mismatch approach, is used to identify the imbalance for each of the test parameters during these tests. In each test, the average value for each of the tested module's parameters are calculated after measuring 3 times. Therefore, each module results in one average value, and the SD is derived from these four average values. A higher standard deviation means more imbalanced behaviors. In this paper, only the dynamic behaviors are investigated, since in high power applications this is more difficult to achieve.

A. Turn-on Behaviors of Paralleling IGBTs

The switching processes of an IGBT are the main source of EMI, in which the rate of change on the collector current (I_c) di/dt or the collector-emitter voltage (V_{ce}) du/dt is the most importance [15]. I_c (or V_{ce}) is used to assess the EMI characteristic. A steeper rise (or fall) in I_c (or V_{ce}) can cause a larger proportion of high frequency in the EMI spectrum. In addition, this is one of the key indexes demonstrating how the I_c (or V_{ce}) waveforms for each of the IGBTs differ from each other. Therefore, analyzing di/dt and du/dt is beneficial for the filter design, and assess the performance of the paralleled IGBTs.

Fig. 3 shows the standard deviation of the di/dt (SD di/dt) trend at different temperatures and operating conditions. It is worth noting that when the temperature is at a room temperature of 25°C, the SD di/dt reaches the bottom. However, when the temperature rises over 25°C or falls below 25°C, the SD di/dt rises. This indicates that when the temperature is too high or too low, the di/dt among these four IGBTs is less symmetric. In these situations the paralleling modules are exposed to EMI more easily. As a result, some IGBTs may suffer stricter di/dt changes. Fig. 3 also shows that a low temperature can cause a much greater imbalance in the di/dt

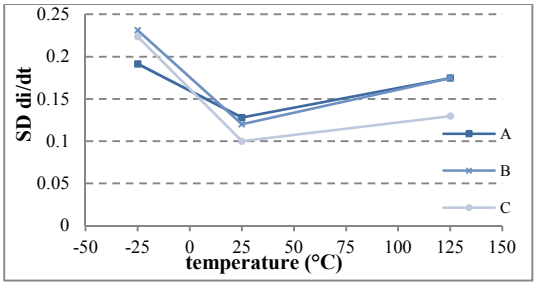
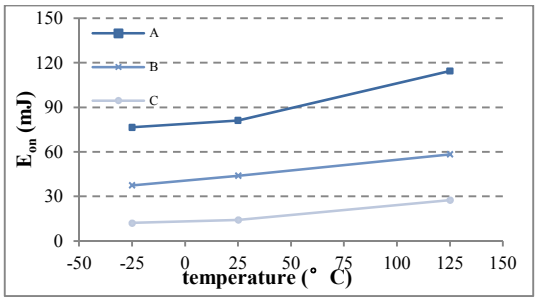
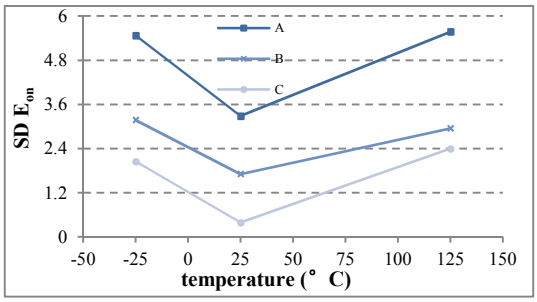


Fig. 3. Standard deviation of di/dt during turn-on.



(a)



(b)

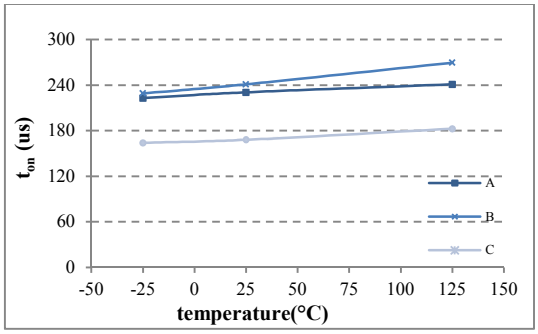
Fig. 4. Average Eon and standard deviation of E_{on} during turn-on. (a) Average value of E_{on}. (b) Standard deviation of E_{on}.

when compared to a high temperature, since the SD di/dt under each condition reaches the largest value at -25°C.

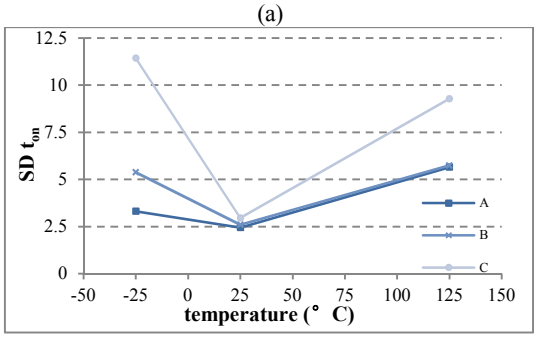
Fig. 4 shows the average turn on loss (E_{on}) and SD E_{on}. Fig. 4 (a) shows that there is a slight E_{on} increase at a low temperature, while there is a bigger E_{on} increase at over 25°C. Fig. 4 (b) shows that a higher output power level leads to a more imbalanced E_{on} distribution among the four paralleled IGBTs regardless of the temperature, since condition A is always higher than B, and B is always higher than C.

From Fig. 4 (b) it can also be seen that among all of the operation conditions it is at 25°C that the SD E_{on} presents the smallest value. When beyond or below that temperature, the SD E_{on} increases.

The positive temperature characteristic (PTC) of IGBTs enables them to be well paralleled when operating for a long time, which is mostly valid in static behavior [16]. Among the many influencing factors in dynamic behaviors, PTC is not that dominant. Once the temperature is very high or very low, the E_{on} imbalance changes the thermal sensitivity parameters and results in unstable operation or failure. The highest SD E_{on}



(a)



(b)

Fig. 5. Average value of t_{on} and standard deviation of t_{on} during turn-on. (a) Average value of t_{on}. (b) Standard deviation of t_{on}.

condition means that the paralleling IGBTs suffer from an uneven E_{on}, namely the junction temperature, which in turn aggravates the imbalanced behaviors. The probability of this occurring rises with the power level.

Fig. 5 shows the average t_{on} and SDT t_{on}. Fig. 5(a) shows that t_{on} rises with temperature. As shown in Fig. 5(b), the SD t_{on} presents a trend similar to E_{on}. The turn-on time, which is one of the major factors, determines the paralleling dynamic behaviors. Usually less turn-on time implies that the IGBT is the earliest to be turned on or the earliest to enter the conduction state. In the first situation, it takes the majority of the load current. This increases the probability of its failure due to the capacitor discharge [17]. In the second situation, this increases the probability of another IGBTs' failure due to higher turn-on losses. Still, the turn-on time among the paralleled IGBTs is likely the same at 25°C. At high or low temperatures, the turn-on time exhibits more imbalanced performance.

B. Turn-off Behaviors of Paralleling IGBTs

Fig. 6 shows the standard deviation of di/dt during turn- off. It basically follows the same trend as the SD di/dt during turn-on. When the temperature is too low, the SD di/dt demonstrates high values under all conditions. When it is at 25°C, the SD di/dt is about the smallest, which means that it has the most balanced di/dt performance.

Fig. 7(a) shows the average E_{off} and SD E_{off} with respect to temperature. There is only a slight increase of E_{off} from -25°C to 25°C under conditions A and B, followed by a higher

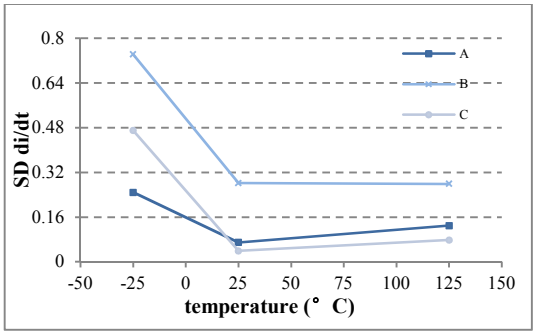
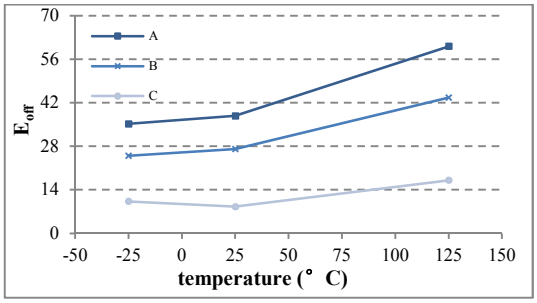
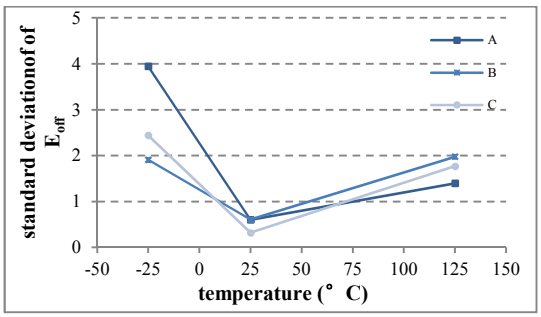


Fig. 6. Standard deviation of di/dt during turn-off.



(a)



(b)

Fig. 7. E_{off} and standard deviation of E_{off} during turn-off. (a) Average value of E_{off}. (b) Standard deviation of E_{off}.

increase from 25°C to 125°C, which is similar to E_{on}. In addition, it is obvious that at -25°C, the imbalance between each of the IGBT modules is at its greatest, since the SD E_{off} is at its highest in Fig. 7(b). In addition, the SD E_{off} rises linearly with temperatures beyond 25°C. It is worth mentioning that when working at temperatures higher than 25°C, the SD E_{off} does not show a big different due to different power levels. This means that temperature has a greater impact on the E_{off} imbalance than the output power level.

The maximum collector-emitter voltage ($V_{ce(max)}$) during turn-off should be avoided under all conditions. Fig.8 shows the SD $V_{ce(max)}$ with respect to temperature. This shows that high temperature is good for the balance and can decrease the probability of over voltage faults. The SD $V_{ce(max)}$ under condition B is larger than that under conditions A and C, of which the former performs at a bus voltage of 600V and the latter two perform at 820V. Therefore, the high voltage is good for the $V_{ce(max)}$ balance.

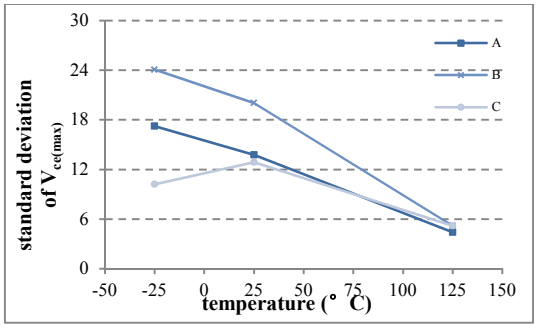
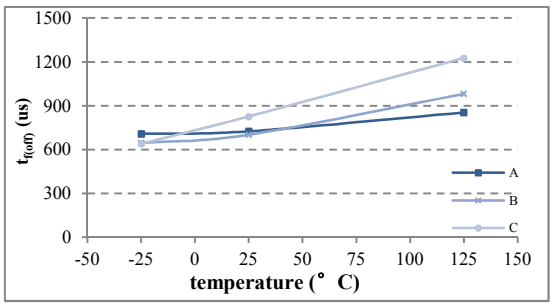
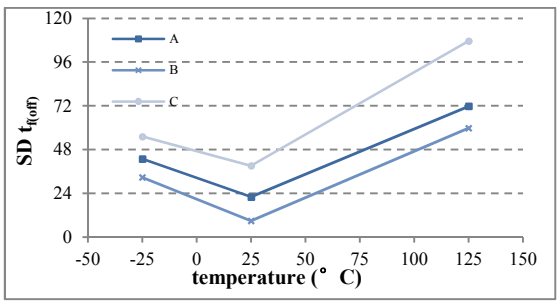


Fig. 8. Standard deviation of $V_{ce(max)}$ during turn-off.



(a)



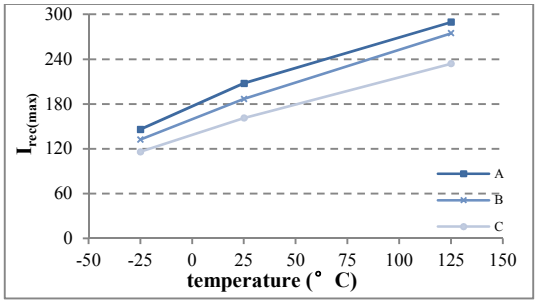
(b)

Fig. 9. Average value of $t_{f(off)}$ and standard deviation of $t_{f(off)}$ during turn-off . (a) Average value of $t_{f(off)}$. (b) Standard deviation of $t_{f(off)}$.

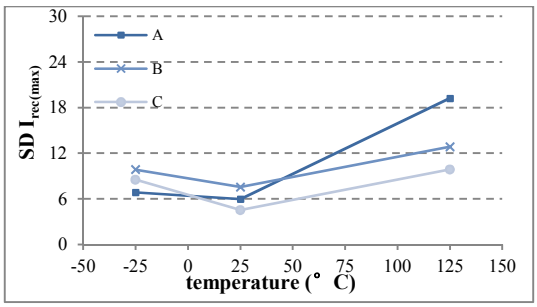
Fig. 9 shows the average $t_{f(off)}$ and SD $t_{f(off)}$ with respect to temperature. It can be seen from Fig. 9(a) that there is a bigger increase of $t_{f(off)}$ due to temperature than $t_{r(on)}$ (see Fig. 4(a)). This indicates that temperature has a larger impact on the turn-off. Fig. 9(b) shows that the SD $t_{f(off)}$ is at its smallest at 25°C. In addition, higher and lower temperatures result in a bigger SD $t_{f(off)}$. A low power output level leads to a bigger SD $t_{f(off)}$, which means a more imbalanced $t_{f(off)}$ performance. This is the same as the way that the line of condition C is higher than in conditions A and B in Fig. 9(b).

C. Reverse Recovery Behaviors

Fig. 10 shows the diode reverse recovery behavior. Fig. 10(a) indicates that the maximum reverse recovery current ($I_{rec(max)}$) increases linearly with the temperature. Fig. 10(b) shows that when the temperature is about 25°C, the SD $I_{rec(max)}$ is at its smallest, which means a more balanced reverse



(a)



(b)

Fig. 10. $I_{rec(max)}$ and standard deviation of $I_{rec(max)}$ in reverse recovery. (a) Average value of $I_{rec(max)}$. (b) Standard deviation of $I_{rec(max)}$.

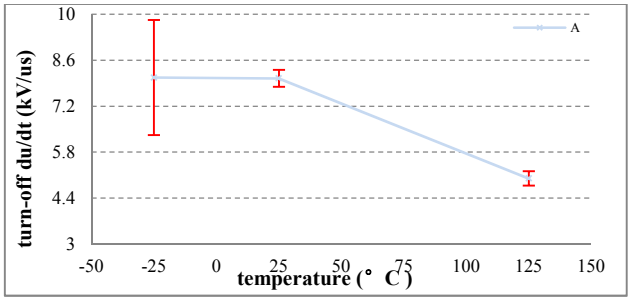
recovery current. However, a high temperature is worse for this balance than a low temperature. At 125°C the SD $I_{rec(max)}$ is bigger under each condition.

IV. Discussion and Analysis

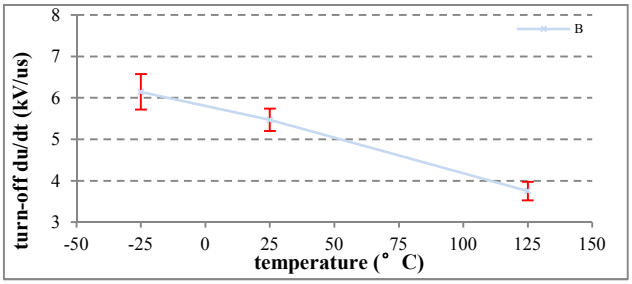
Xuesong Wang has demonstrated that when the discrepancy between the paralleling IGBTs decreases to zero, the ambient temperature change results in little imbalance among the paralleling IGBTs [8], provided that the other influencing factors are identical. Therefore, from the above measurement results, it can be reasonably assumed that some of the thermal sensitive parameters have changed at very high or very low temperatures. This later leads to a high standard deviation, which results in a high paralleling imbalance.

A. V_{ge}

It is apparent from section III that almost all of the standard deviations of these tested parameters increase with temperature when operated at over 25°C. This module (FF600R12ME4) uses Trench and Fieldstop technology. The internal MOS-channel loses its conductivity as soon as the gate falls below the Miller plateau and $V_{ge(th)}$. The load current can only be supported by the carriers remaining in the drift zone. At this point, there is no facility left to control the IGBT switching behavior. The IGBT will carry out the turn-off process with a self-limiting voltage gradient du/dt which is determined by the doping, geometry, load current and junction temperature [18]. Fig. 11 shows the turn-off du/dt under conditions A and B. The



(a)



(b)

Fig. 11. the relation of turn off du/dt to temperature and its standard deviation. (a) Condition A. (b) Condition B.

error bars in the pictures are the standard deviations. This shows that when the temperature becomes high, the du/dt among these four IGBTs fluctuates only within a small range, just as the error bar goes shorter. This indicates that even at high temperatures the du/dt among these IGBTs is well balance-performed. Because the du/dt is barely influenced, it can be deduced that temperature imposes great impact on $V_{ge(th)}$. This influences the time when V_{ge} falls to the Miller plateau, which is also the time V_{ce} starts to rise.

(1) is the relationship between V_{th} and temperature, based on the research of Bo Wang [19].

$$\frac{dV_{th}}{dT} = [\frac{\phi_{FB}}{T} - \frac{k}{q}(\frac{E_g}{2kT} + 1.5)](2 + \frac{\sqrt{2\varepsilon_0 \varepsilon_{si} q N_{Amax} 2\phi_{FB}}}{2\phi_{FB} C_{ox}}] \quad (1)$$

Where ϕ_{FB} is the surface potential, T is the junction temperature, k is the Boltzmann constant, q is the electron charge, E_g is the forbidden band, ε_0 is the dielectric constant for vacuum, ε_{si} is the dielectric constant for silicon, N_{Amax} is the surface concentration, and C_{ox} is the gate oxide capacitance.

It has been demonstrated that $V_{ge(th)}$ decreases with temperature in [20]. However, in paralleled applications, $V_{ge(th)}$ cannot be guaranteed to be identical when the temperature becomes high. According to (1), at high temperatures the PTC actually changes. In addition, the effect of thermo-electric coupling is very sensitive to increasing temperature. Especially a high currents, a very small change of current will cause the junction temperature to climb rapidly [19]. This results in positive feedback. Even paralleled IGBTs are current

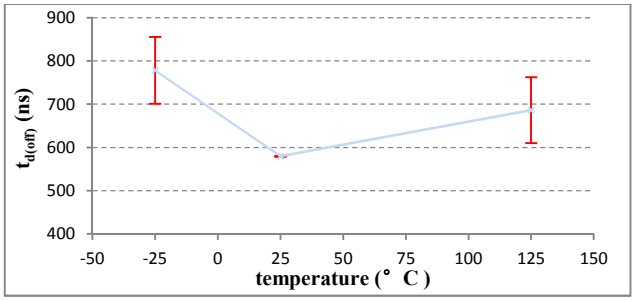


Fig. 12. The relation of $t_{d(off)}$ to temperature and its standard deviation.

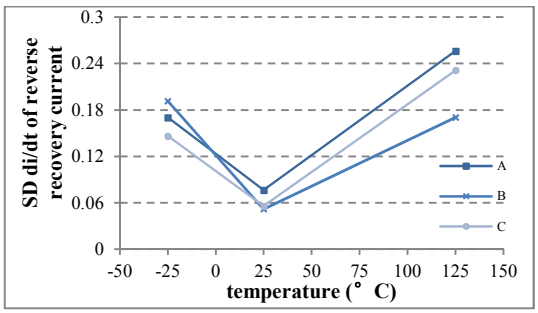


Fig. 13. The standard deviation of di/dt of the reverse recovery current.

symmetrical within a margin of error. Those with just a slightly higher current face much higher thermal runway and reduced $V_{ge(th)}$. This in turn makes the IGBTs turn off earlier and take more current. Fig. 12 demonstrates this by showing the $t_{d(off)}$. The error bar means the standard deviation. It can be seen that it is too high at 125°C. This indicates that $t_{d(off)}$ experiences a great change, which is the same as $V_{ge(th)}$.

According to [6], a different $V_{ge(th)}$ leads to an imbalanced turn on time (see Fig. 5), which results in a different current. As a result, the SD E_{on} is higher.

B. Reverse Recovery of the Diode

Bin Lu has demonstrated that temperature influences the turn-on behaviors of IGBTs by changing the reverse recovery behaviors of the diode [21].

Fig. 13 shows the SD di/dt of the reverse recovery current (SD $di/dt_{(rev)}$). It can be clearly seen that under very high and very low temperature conditions, the SD $di/dt_{(rev)}$ values are much bigger. The freewheeling currents with uneven changing rates from the diodes flow into the IGBTs, leading to different di/dt of the IGBTs. The SD $di/dt_{(rev)}$ values resemble those in Fig. 3, since they have a similar range and trend.

C. Low Temperature

[22]-[24] demonstrated that the velocity of carriers and their mobility increase with a reduction in temperature. This can result in a change in the turn-on (or turn-off) behaviors. The turn-on loss increases slightly when the temperature is

decreased. This is due to increases in the current rise time and voltage fall time. For turn-off, a lower temperature leads to a lower turn-off time, as a result of the decreasing current gain of the PNP bipolar part and the carrier lifetime. This also means that the turn-off loss decreases. However, as Fig. 7(a) shows, the turn-off loss in this study rises with a reduction in temperature. Thus, it can be assumed that some of the other features impose a greater impact at lower temperatures.

The negative temperature coefficient (NTC) characteristics appearing at low temperatures for IGBTs based on fieldstop technologies is one reason for the paralleling behaviors at low temperatures. Volke and Hornkamp have shown that because of the low doping concentration, the contact resistance between the p-layer and the backside metallization plays an increasing role at low temperatures. At temperatures below approximately 20°C this influence begins to dominate and the IGBTs start to show NTC behavior [17]. However, temperature can still magnify such little deviancies. A change of the loop inductance leads to a redistribution of the current during turn-on and turn-off, which finally aggravates the imbalance.

V. CONCLUSIONS

When Trench-Fieldstop IGBTs are paralleled, there is an obvious trend with respect to temperature. The best paralleling temperature can be determined for such trench and fieldstop IGBTs, and very low (or very high) temperatures may aggravate the paralleling behaviors. High temperatures amplify the deviances among the IGBTs, such as $V_{ge(th)}$. This in turn aggravates the imbalance by changing the switching time. However, low temperatures make IGBTs show the NTC feature, which also causes a bigger imbalance. There is a trade-off between the switching loss and the switching behavior imbalance at low temperatures. Lower temperatures usually mean less switching losses. However, it also enlarges the imbalance among the paralleling IGBTs. A higher temperature is beneficial for decreasing the probability of over voltage $V_{ce(max)}$ during turn-off. In addition, a high output power level leads to more balanced turn-on time and turn-off time among the paralleling IGBTs. When paralleling is necessary in applications confronting extreme climates, the chance of operating at a low junction temperature is high. The previous design may fail as the paralleling imbalance leads to the IGBT working out of the safety operation area (SOA). Such results can give guidance for optimizing the heat sink and overvoltage protection circuit of paralleling applications.

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APPENDIX

TABLE II

DEFINITION OF THE PARAMETERS

Test Parameter	Definition	Note
$T_{d(on)}$	From 10% V_{ge} to 10% I_c	Turn on delay time
$T_{r(on)}$	From 10% I_c to 90% I_c	Turn on rise time
T_{on}	$T_{d(on)} + T_{r(on)}$	Turn on time
E_{on}	From 10% I_c to 2% V_{ce}	Turn on loss
$T_{d(off)}$	From 90% V_{ge} to 90% I_c	Turn off delay time
$T_{f(off)}$	From 90% Ic to 10% I_c	Turn off fall time
T_{off}	$T_{d(off)} + T_{f(off)}$	Turn off time
E_{off}	From 10% V_{ce} to 2% I_c	Turn off loss

TABLE III

VALUES OF THE SETUP PARAMETERS

Setup Parameter	Value
C_{DC} (D_c Link Capacitor)	420uF
C_s (Snubber Capacitor)	1.5uF
L_s (Stray Inductance:L_{s1}, L_{s2})	about 35nH
L_{load} (Load inductance)	50uH

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