JPE 14-4-17

http://dx.doi.org/10.6113/JPE.2014.14.4.778
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

# One-Cycle Control Strategy with Active Damping for AC-DC Matrix Converter

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**Abstract**

This study presents an input filter resonance mitigation method for an AC–DC matrix converter. This method combines the advantages of the one-cycle control strategy and the active damping technique. Unnecessary sensors are removed, and system cost is reduced by employing the grid-side input currents as feedback to damp out LC resonance. A model that includes the proposed method and the input filter is established with consideration of the delay caused by the actual controller. A zero-pole map is employed to analyze model stability and to investigate virtual resistor parameter design principles. Based on a double closed-loop control scheme, the one-cycle control strategy does not require any complex modulation index control. Thus, this strategy can be more easily implemented than traditional space vector-based methods. Experimental results demonstrate the veracity of theoretical analysis and the feasibility of the proposed approach.

**Key words:** Active Damping, Matrix Converter, One-Cycle Control, Resonance Mitigation

## I. INTRODUCTION

The AC–DC matrix converter (AC–DC MC) is a novel and generalized power converter topology derived from a three-phase matrix converter (MC). AC–DC MC has the following significant advantages [1], [2]:

1) compact design and high reliability because of the absence of bulky energy storage components
2) generation of DC output voltage with arbitrary amplitude and polarity
3) sinusoidal input current with controllable input power factor
4) operation in all four torque-speed plane quadrants because of regenerative capability

These desirable characteristics make the AC–DC MC an ideal future solution for AC–DC power conversion applications.

An inductor–capacitor filter is always required at the input side of AC–DC MC. The filter capacitor reduces the high-frequency current harmonics caused by the switching operation and the inductive nature of the AC-line. The filter inductor suppresses the low-order harmonics from the power source. However, the LC filter, which has no energy storage, causes instability during operation and even results in severe system failure [3], [4]. The inherent resonance figure of the slightly damped LC filter mainly causes this issue. Resonance is easily excited by the harmonic pollution in the power source or the harmonic components in the input currents drawn by the AC–DC MC itself. The resonance problem has traditionally been considered at the design stage, in which the appropriate filter parameters are selected to tune the resonance frequency away from the potential harmonic frequency. However, this method limits performance because resonance frequency is related to source inductance, which usually varies with power source conditions. Adding a physical damping resistor into the filter to mitigate resonance is another classical, straightforward, and widely implemented method [5]. However, this resistor results in additional power loss, especially in high-power applications.

The active damping (AD) method improves input current quality and enhances system stability without changing the power converter topology or affecting its efficiency. The AD method simulates a fictitious damping resistor connected in

Manuscript received Aug. 26, 2013; accepted May 20, 2014
Recommended for publication by Associate Editor Kyo-Beum Lee.
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parallel with the filter capacitor. The harmonic current results are then forced through this resistor from the resonance flow to suppress the resonance. In [6]-[9], the authors used capacitor voltages as feedback to determine the harmonic current and successfully mitigate resonance in three-phase current source rectifiers (CSRs). In [10], the feedback signal changed to inductor current to remove additional capacitor voltage sensors. The classical space vector modulation (SVM) strategy controls the CSRs in most of these schemes. To synthesize the harmonic current, a new modulation index is obtained as an input current function that is normalized to output current. These procedures include complex space vector angle and modulation ratio calculations, which increase the software complexity. Therefore, developing an appropriate modulation and control strategy is key to the easy implementation of the AD method in practical applications.

A variety of pulse–width–modulation (PWM) switching techniques has been developed for AC–DC MC on the basis of two different approaches.

The first approach is the direct transfer function method proposed by Donald and Thomas [1]. This method requires the controller to perform cumbersome calculations per switching period to define all six elements in the transfer matrix. This method increases complexity while reducing practicability and reliability. Consequently, this method is preferred for theoretical analysis rather than real-time implementation.

The second approach is the SVM strategy [11], [12], which is similar to that used by CSRs. This method is a well-known and well-established modulation strategy because of its high performance, relative simplicity, and inherent capability to achieve full control of both output voltage and input power factor. Nevertheless, this method is inappropriate for the AD strategy as aforementioned.

Aside from linear techniques, modern control algorithms have recently been reported for the current and torque control of AC and DC machines by using MC or AC–DC MC; these control algorithms include predictive current control (PCC) [13], [14], predictive torque control [14], and sliding mode variable structure control [16]. In [13], a PCC method with active damping was proposed for MC to reduce software complexity because PCC control does not use modulation index variables. However, this method is highly sensitive to parameters and load variations. Moreover, the unfixed switching frequency makes the design of input and output filters difficult.

We introduce a new non-linear control strategy called one-cycle control (OCC) [17] into the AC–DC MC system. Compared with traditional modulation approaches, the OCC control strategy features fast dynamic response, excellent power source perturbation rejection, strong robustness, and automatic switching error correction. Similar to the PCC method, this strategy also discards explicit modulation index

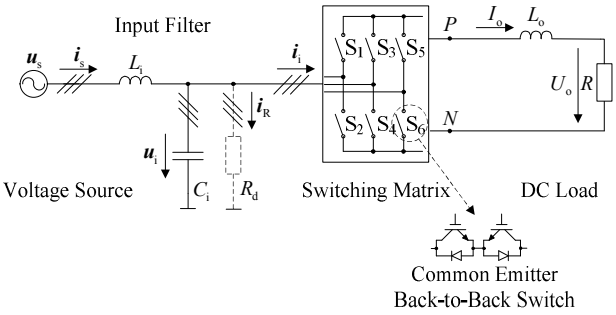



Fig. 1. Power topology of AC–DC MC.

control. These characteristics imply that the proposed control scheme exhibits a simple circuit, high performance, low cost, high stability, and easy implementation.

This paper is organized as follows: Section II investigates the inductor current feedback AD method and its stability with consideration of the time delay caused by the actual controller. Section III explains the modification to the OCC controller to include AD. Section IV discusses the damping resistance selection principles. Section V presents the experimental results. Section VI draws in the conclusions.

## II. Active Damping Approach for AC–DC MC

### *A. Active Damping Approach*

Fig. 1 shows the converter topology of AC–DC MC, which consists of a three-phase voltage source indicated as $\boldsymbol{u}_s$, a switching matrix composed of six bi-directional switches $S_1$ to $S_6$, an input LC filter, and an output inductive load. Assuming that the AD method is not included, the virtual resistive damper $R_d$ in Fig. 1 is temporarily neglected. The input filter is modeled as

$$\boldsymbol{u}_S = L_i \frac{d\boldsymbol{i}_S}{dt} + \boldsymbol{u}_i \tag{1}$$

$$\boldsymbol{i}_S = C_i \frac{d\boldsymbol{u}_i}{dt} + \boldsymbol{i}_i \tag{2}$$

where $L_i$ and $C_i$ represent the filter capacitor and filter inductor, respectively; $\boldsymbol{u}_s=[u_a\ u_b\ u_c]^T$ and $\boldsymbol{i}_s=[i_a\ i_b\ i_c]^T$ represent the grid-side voltage vector and current vector, respectively; and $\boldsymbol{u}_i=[u_{ia}\ u_{ib}\ u_{ic}]^T$ and $\boldsymbol{i}_i=[i_{ia}\ i_{ib}\ i_{ic}]^T$ represent the input-side voltage vector and current vector, respectively. If $\boldsymbol{u}_s$ and $\boldsymbol{i}_i$ are taken as input variables and $\boldsymbol{u}_i$ and $\boldsymbol{i}_s$ as output variables, then (1) and (2) can be transformed into the Laplace domain as

$$\boldsymbol{u}_i(s) = \frac{-sL_i}{s^2L_iC_i+1}\boldsymbol{i}_i(s) + \frac{1}{s^2L_iC_i+1}\boldsymbol{u}_S(s) \tag{3}$$

$$\boldsymbol{i}_S(s) = \frac{1}{s^2L_iC_i+1}\boldsymbol{i}_i(s) + \frac{sC_i}{s^2L_iC_i+1}\boldsymbol{u}_S(s) \tag{4}$$

From (3) and (4), the LC filter may amplify the harmonic components in the voltage source $\boldsymbol{u}_s$ or in the input current $\boldsymbol{i}_i$, which results in severe oscillations in $\boldsymbol{u}_i$ and $\boldsymbol{i}_s$ when the LC filter is tuned to one of the harmonics.

The AD approach emulates a virtual damping resistor $R_d$ in parallel with the filter capacitor $C_i$, as shown in Fig. 1. When $R_d$ is considered, Equation (2) should be modified as

$$\boldsymbol{i}_s = C_i \frac{d\boldsymbol{u}_i}{dt} + \boldsymbol{i}_i + \boldsymbol{i}_R \tag{5}$$

The damping resistance $R_d$ does not physically exist in practical circuits. Therefore, the converter extracts the $R_d$ current indicated by $\boldsymbol{i}_R$ in (5). $R_d$ is proportional to the capacitor voltage.

$$\boldsymbol{i}_R = \frac{1}{R_d} \cdot \boldsymbol{u}_i \tag{6}$$

Active damping aims to mitigate the system harmonics rather than the fundamental component. Thus, only harmonic capacitor voltage should be considered when calculating the damping current $\boldsymbol{i}_R$. Therefore, input voltage is transformed into the *dq* reference frame. In this frame, the fundamental component of the capacitor voltage vector $\boldsymbol{u}_i^{dq} = [\, u_i^d \quad u_i^q \,]^T$ is the DC component, which can be easily deleted by a digital DC-blocker [18] or a high-pass filter [19]. Remaining AC components correspond to all harmonics present in $\boldsymbol{u}_i^{dq}$.

$$\boldsymbol{u}_{ih}^{dq}(s) = h_f(s) \cdot \boldsymbol{u}_i^{dq}(s) \tag{7}$$

where

$$h_f(s) = \frac{s2T_s}{sT_s(1+a) + 2(1-a)} \tag{8}$$

is the digital DC-blocker transfer function in the Laplace domain, $a$ is the parameter, and $T_s$ is the sampling period.

Once the input voltage harmonics in Laplace domain $\boldsymbol{u}_{ih}^{dq}(s)$ have been obtained, harmonic damping currents $\boldsymbol{i}_{Rh}^{dq}(s)$ are determined by combining (6) and (7), as indicated by

$$\boldsymbol{i}_{Rh}^{dq}(s) = \frac{1}{R_d} \cdot h_f(s) \cdot \boldsymbol{u}_{ih}^{dq}(s) \tag{9}$$

From (9), three voltage sensors have to be set up in the practical circuit to feedback the instantaneous value of input voltage $\boldsymbol{u}_i$. These sensors are redundant because other algorithms do not use input voltage information.

Two sets of sensors are essential for AC–DC MC input side: one is grid-side current sensor $\boldsymbol{i}_s$, used for over-current protection, and the other is grid-side voltage sensor $\boldsymbol{u}_s$, used for over-voltage protection and voltage-based commutation. So as to reduce the system cost and enhance the reliability, $\boldsymbol{u}_s$ and $\boldsymbol{i}_s$ are utilized to estimate input voltage $\boldsymbol{u}_i$.

According to (1), we can write

$$\boldsymbol{u}_i = \boldsymbol{u}_s - L_i \frac{d\boldsymbol{i}_s}{dt} \tag{10}$$

Substituting (10) into (9), we obtain

$$\begin{aligned} \boldsymbol{i}_{Rh}^{dq}(s) = {} & \frac{1}{R_d} \cdot h_f(s) \cdot \boldsymbol{u}_s^{dq}(s) \\ & - \frac{L_i}{R_d} \cdot h_f(s) \cdot h_d(s) \cdot \boldsymbol{i}_s^{dq}(s) \\ & + \frac{\omega_i L_i}{R_d} \cdot h_f(s) \cdot \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix} \cdot \boldsymbol{i}_s^{dq}(s) \end{aligned} \tag{11}$$

where $\omega_i$ is the power source angular frequency, and

$$h_d(s) = \frac{1}{T_s} \cdot \frac{2s}{s + 2/T_s} \tag{12}$$

is the digital derivation transfer function.

From (11), the current throughout of $R_d$ is determined as a linear combination of three individual fractions.

The resulting output of the first fraction is proportional to the power source harmonics. The practical source voltages are always slightly harmonic-polluted, thus causing a few AC components in $u_s^d$ and $u_s^q$ to pass the digital DC-blocker. However, the magnitudes of these components are small in the low-frequency stage, such that their influence on $\boldsymbol{i}_s^{dq}(s)$ is negligible.

The damping current gain $1/R_d$, filter inductor $L_i$, digital DC-blocker dynamic, digital deviation dynamic, and grid-side current in *dq* reference frame comprise the second part of (11). After digital deviation, the remaining part of $\boldsymbol{i}_s^{dq}(s)$ contains only AC components. The effect of the DC-blocker on these signals is negligible. Therefore, the transfer function of this fraction is simplified to

$$G_2(s) = \frac{L_i h_d(s)}{R_d} \tag{13}$$

where the digital DC-blocker dynamic is omitted.

The third fraction contains cross-coupling terms related to the AC signals in $\boldsymbol{i}_s^{dq}(s)$. The gain margin of this fraction is smaller compared with the second fraction.

The second fraction is dominant in (11) in the final results. Therefore, the other two fractions were ignored to reduce calculation difficulty. The resulting simplified algorithm scheme is shown in Fig. 2.

### *B. Stability Analysis of the Proposed Active Damping Method*

In practical implementation, the controller realized by a digital signal processor (DSP) needs a finite calculation time for signal sampling, damping current $\boldsymbol{i}_{Rh}^{dq}$ calculation, and modulation strategy implementation. These processes cause time delay, which reduces the gain and phase margins, deteriorates the performance, and affects control loop stability. The total control and modulation delay is approximated from the effective switching frequency. Time delay is equivalent to one switching period for the OCC

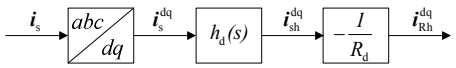



Fig. 2. Algorithm scheme of the AD strategy.

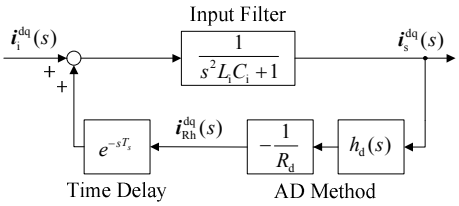



Fig. 3. Model of the AD closed-loop control system.

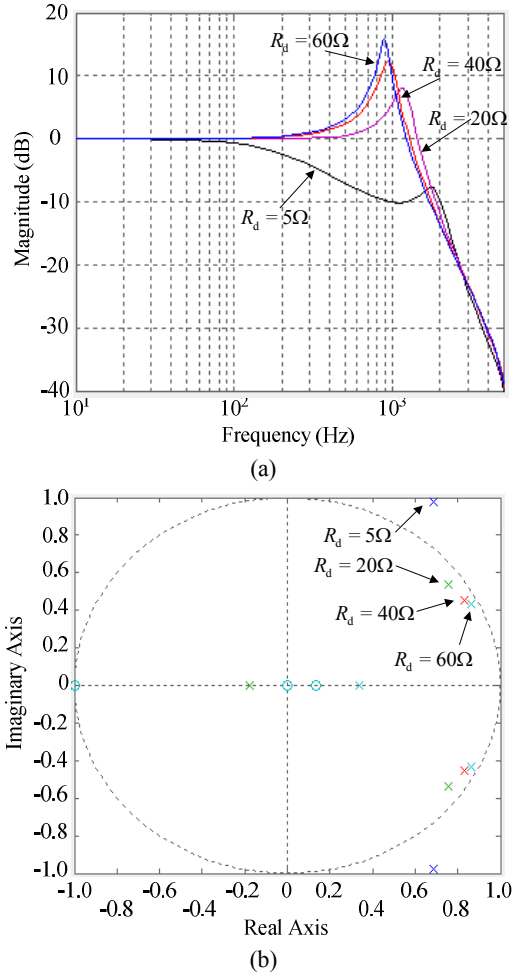



Fig. 4. Stability analysis with different $R_d$ values: (a) Bode map and (b) zero-pole map.

control technique used. Half of the time is used for analog–digital sampling, whereas the other half is used to execute the AD method and OCC algorithm.

The small-signal model of the closed-loop AD system is approximated by using filter impedance, the dynamic of the AD method, and total time delay, as shown in Fig. 3.

The Bode and zero-pole maps of the closed-loop control system are plotted in Fig. 4 with different AD resistance $R_d$ values. For example, a filter resonance frequency of 805 Hz ($L_i$=3mH, $C_i$=13uF) and a switching frequency of 12 kHz is used.

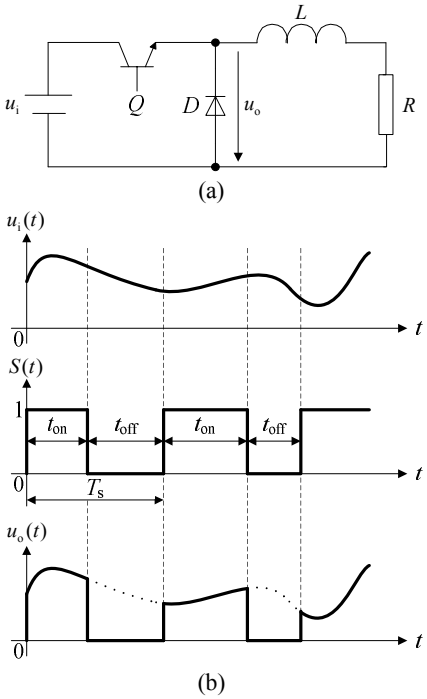



Fig. 5. Operational principle of the OCC control strategy: (a) topology of a simplified DC–DC chopper and (b) waveforms of input voltage, switching function, and output voltage.

Fig. 4(a) shows that the crest in the frequency response curve becomes flat when AD resistance decreases. Therefore, a small resistance value equates to a desirable effect in mitigating resonance and reducing filter sensitivity to resonance frequency. However, the AD loop gain margin is inversely proportional to damping resistance. When damping resistance is smaller than the minimum value, the gain margin becomes extremely high and the system becomes unstable. The minimum damping resistance value for filter parameters used in this study (i.e., $L_i$=3 mH and $C_i$=13 μF) is 12 Ω.

## III. One-Cycle Control Strategy for AC–DC MC

### *A. Principle of One-cycle Control Strategy*

The OCC control strategy aims to adjust the duty ratio of the switching device and force the controlled variable to follow the control reference during one switching cycle. The topology of a simplified DC–DC chopper illustrated in Fig. 5a explains the basic operational principle of the OCC controller [12], [17].

In Fig. 5, $u_i(t)$ and $u_o(t)$ represent the input and output voltages of the DC–DC chopper. Let us assume that switching device $Q$ is turned on during time interval $t_{on}$ and turned off during time interval $t_{off}$, where $t_{on}+t_{off}=T_s$. Switching function $S(t)$ is as follows:

$$S(t)=\begin{cases}1, & 0<t<t_{on}\\ 0, & t_{on}<t<T_s\end{cases} \tag{14}$$

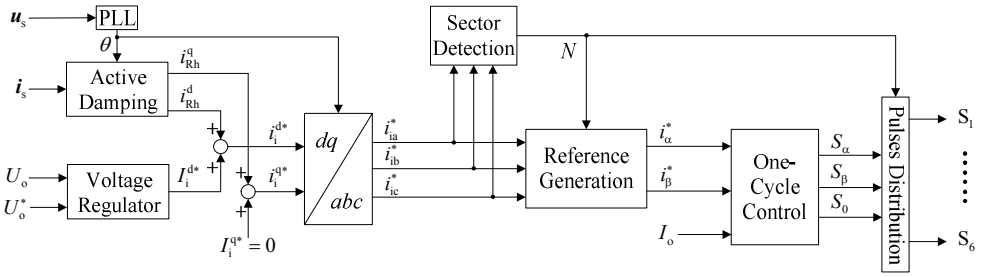



Fig. 6. Control scheme of OCC strategy for AC–DC MC with AD.

If the forward voltage drop of switching device $Q$ is neglected and the switching frequency $f_S = 1/T_S$ is assumed to be higher than input voltage $u_i(t)$, then the resulting output voltage $u_o(t)$ is a PWM pulse sequence with the same frequency and duty ratio as the switching function $S(t)$ and the same envelop as input voltage $u_i(t)$. This condition is illustrated in Fig. 5b. Thus, the average value of $u_o(t)$ in one switching period can be obtained by

$$\bar{u}_o(t) = \frac{1}{T_S}\int_0^{T_S} u_o(t)dt = \frac{1}{T_S}\int_0^{t_{on}} u_i(t)dt \quad (15)$$

Non-linear modulation is applied to switching device $Q$ to force the integration of $u_o(t)$ in one switching period is equal to the integration of analog control reference $u_o^*(t)$ in one switching period

$$\int_0^{T_S} u_o(t)dt = \int_0^{T_S} u_o^*(t)dt \approx T_S u_o^*(t) \quad (16)$$

Substituting (15) into (14), we obtain

$$\bar{u}_o(t) = \frac{1}{T_S}\int_0^{T_S} u_o^*(t)dt = u_o^*(t) \quad (17)$$

This technique to modulate and control switching device $Q$ according to (16) is the one-cycle control strategy. From (17), we conclude that the influence of input voltage $u_i(t)$ on output $u_o(t)$ is fully rejected and $u_o(t)$ is instantaneously controlled within one switching cycle. In other words, the OCC technique turns the original non-linear switch device into a linear transferring path.

### *B. Proposed One-cycle Control Strategy with Active Damping for AC–DC MC*

Two control objectives are considered for the AC–DC MC: (1) voltage control on the output side of the converter and (2) unity displacement power factor operation on the input side of the converter. Based on the assumption that grid-side voltage $\boldsymbol{u}_s$ is purely sinusoidal and neglects power loss in switching devices and transmission lines, the following active power balance equation must be satisfied:

$$u_i^d i_i^d = \frac{U_o^2}{R} \quad (18)$$

From (18), output voltage $U_o$ is related to input $d$-axis current $i_i^d$ because grid-side $d$-axis voltage $u_i^d$ is a constant value (in this case). Thus, the first control objective is realized by adjusting $i_i^d$ and the second control objective is obtained by minimizing input $q$-axis current $i_i^q$.

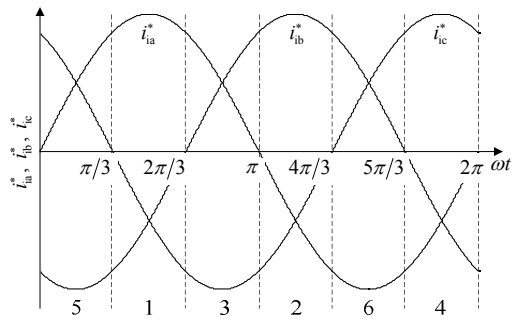



Fig. 7. Demanded phase currents and corresponding sectors.

The resulting control scheme is illustrated in Fig. 6. A PI controller realizes voltage regulation. The output is the main reference of input $d$-axis current $I_i^{d*}$, while the main reference of input $q$-axis current $I_i^{q*}$ is 0 because of the demanded unity input power factor. The AD method is included in the proposed scheme through adding damping current $\boldsymbol{i}_{Rh}^{dq}$ to $I_i^{d*}$ and $I_i^{q*}$. Thus, the new input current reference is expressed as:

$$\boldsymbol{i}_i^{dq*} = \boldsymbol{I}_i^{dq*} + \boldsymbol{i}_{Rh}^{dq} \quad (19)$$

The demanded phase currents in $abc$ coordinates are obtained by applying this transformation equation:

$$\begin{bmatrix} i_{ia}^* \\ i_{ib}^* \\ i_{ic}^* \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix}\cdot\begin{bmatrix} i_i^{d*} \\ i_i^{q*} \end{bmatrix} \quad (20)$$

According to the zero-crossing point of each demanded phase current, each input current cycle is evenly divided into six sectors to realize OCC control (Fig. 7).

Sector number $N$ is determined by:

$$N = sign(i_{ic}^*) * 4 + sign(i_{ib}^*) * 2 + sign(i_{ia}^*) \quad (21)$$

where

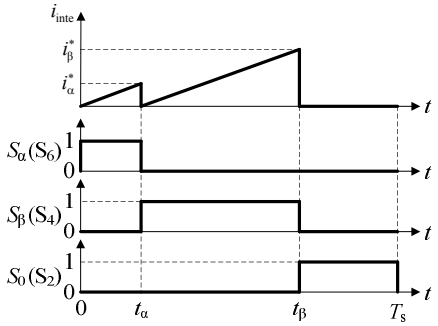



Fig. 8. Switching sequence and integrator waveform in sector I.

$$sign(x)=\begin{cases}1, & x>0\\ 0, & x\le 0\end{cases} \tag{22}$$

The input phase, whose current direction is opposite the other two phases, is the dominant phase in each sector. The other two input phases are auxiliary phases; the products of the absolute values of their corresponding demanded phase currents and switching period $T_s$ are current references indicated by $i_\alpha^*$ and $i_\beta^*$ in Fig. 6. The OCC controller instantaneously compares the current references with the integrated output current to determine duty ratios. Resulting switching signals $S_\alpha$, $S_\beta$, and $S_0$ are distributed to proper bi-directional switches in accordance with the sector number.

Without loss of generality, assuming demanded input currents are in sector 1, DC output polarity is positive and output inductor is large enough to guarantee continuous and constant output current. In this example, the dominant phase is input phase *a* and current references $i_\alpha^*$ and $i_\beta^*$ are $T_s\left|i_{ic}^*\right|$ and $T_s\left|i_{ib}^*\right|$, respectively. The bi-directional switch $S_1$ is kept on in the entire region to provide a path for the output current flowing from the power source to the DC load. Switches $S_3$ and $S_5$ are kept off to avoid input short circuit; and $S_2$, $S_4$, and $S_6$ in the lower bridge arm are turned on successively at following a switching frequency sequence (Fig. 8).

1) At the beginning of each switching period, $S_6$ is switched on, whereas $S_2$ and $S_4$ are switched off to enable the output current $I_o$ to flow back to input phase *c*. The resulting equivalent circuit is shown in Fig. 9(a). The OCC controller integrates the output current and compares the result of $i_{inte}$ to the current reference $i_\alpha^*$ which is $T_s\left|i_{ic}^*\right|$ in this example, until the two values equal each other at time instance $t_\alpha$.

2) $S_4$ is switched on, whereas $S_6$ is switched off to commutate the load current from input phase *c* to input phase *b*, as shown in Fig. 9(b). The integrator is reset to zero at the same time and repeat the first integration procedure with current reference changed to $i_\beta^*$. Consequently, integration result $i_{inte}$ reaches current reference $i_\beta^*$ at time instance $t_\beta$.

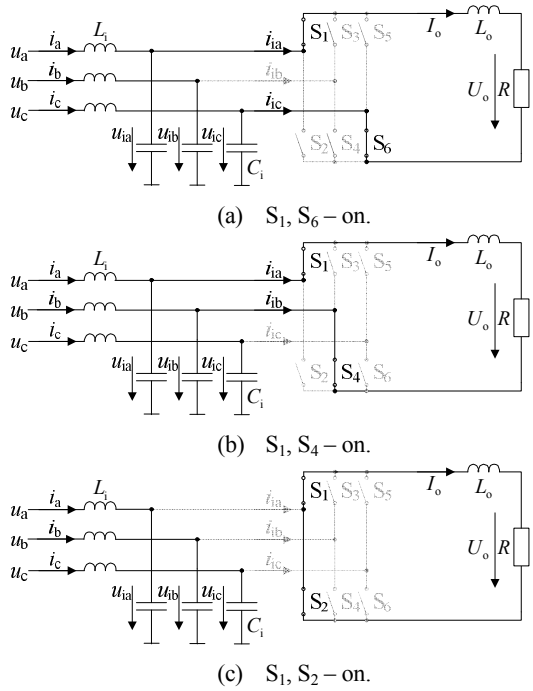



Fig. 9. Equivalent circuit of AC–DC MC in sector I.

3) Finally, only $S_2$ is switched on in the lower bridge arm. The yielding equivalent circuit is illustrated in Fig. 9(c). Doing so totally disconnects the input and output sides, such that no power is transmitted from the source to the DC load. All three input currents, as well as the integrator, remains at zero from $t_\beta$ to the end of the switching cycle. $S_1$ and $S_2$ provide a freewheeling path for the output current to avoid a detrimental open circuit in the inductive load.

Hence, the average values of the input currents $i_{ib}$ and $i_{ic}$ in one switching cycle are respectively given by (23) and (24).

$$\bar{i}_{ib}=\frac{1}{T_s}\int_0^{T_s} i_{ib}dt=-\frac{1}{T_s}\int_{t_\alpha}^{t_\beta} I_o dt=-\frac{i_\beta^*}{T_s}=i_{ib}^* \tag{23}$$

$$\bar{i}_{ic}=\frac{1}{T_s}\int_0^{T_s} i_{ic}dt=-\frac{1}{T_s}\int_0^{t_\alpha} I_o dt=-\frac{i_\alpha^*}{T_s}=i_{ic}^* \tag{24}$$

Based on the assumption that input three-phase system is well balanced, the third input current $i_{ia}$ can be obtained by

$$\bar{i}_{ia}=0-\bar{i}_{ib}-\bar{i}_{ic}=0-i_{ib}^*-i_{ic}^*=i_{ia}^* \tag{25}$$

From (23) to (25), input currents are controlled for reference tracking. Therefore, output voltage is effectively regulated, input power factor is unified, and the AD method is realized without any complex modulation index control. Moreover, only input currents with small absolute values are switched at high frequency; switches connected to the input phase with maximum current absolute value are kept on and off in the entire sector. Consequently, switching losses are greatly reduced.

Similarly, deriving current references and the switching signal distribution principle at the positive output voltage in other sectors can be derived in the same manner as shown in Table I.

TABLE I

CURRENT REFERENCES AND THE SWITCHING SIGNAL DISTRIBUTION PRINCIPLE OF THE OCC CONTROL STRATEGY WHEN OUTPUT VOLTAGE IS POSITIVE

| Sector | Current references | | Control sequence and output logic | | | | |
|---|---|---|---|---|---|---|---|
| | $i_\alpha^*$ | $i_\beta^*$ | ON | OFF | $S_\alpha$ | $S_\beta$ | $S_0$ |
| 1 | $T_s\lvert i_{ic}^*\rvert$ | $T_s\lvert i_{ib}^*\rvert$ | $S_1$ | $S_3$, $S_5$ | $S_6$ | $S_4$ | $S_2$ |
| 2 | $T_s\lvert i_{ia}^*\rvert$ | $T_s\lvert i_{ic}^*\rvert$ | $S_3$ | $S_1$, $S_5$ | $S_2$ | $S_6$ | $S_4$ |
| 3 | $T_s\lvert i_{ib}^*\rvert$ | $T_s\lvert i_{ia}^*\rvert$ | $S_6$ | $S_2$, $S_4$ | $S_3$ | $S_1$ | $S_5$ |
| 4 | $T_s\lvert i_{ib}^*\rvert$ | $T_s\lvert i_{ia}^*\rvert$ | $S_5$ | $S_1$, $S_3$ | $S_4$ | $S_2$ | $S_6$ |
| 5 | $T_s\lvert i_{ia}^*\rvert$ | $T_s\lvert i_{ic}^*\rvert$ | $S_4$ | $S_2$, $S_6$ | $S_1$ | $S_5$ | $S_3$ |
| 6 | $T_s\lvert i_{ic}^*\rvert$ | $T_s\lvert i_{ib}^*\rvert$ | $S_2$ | $S_4$, $S_6$ | $S_5$ | $S_3$ | $S_1$ |

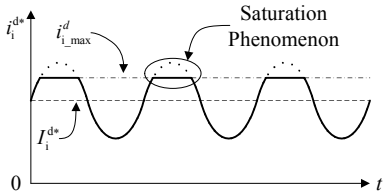



Fig. 10. Effect of the saturation phenomenon.

## IV. SELECTION OF ACTIVE DAMPING RESISTANCE

A small value of AD resistance $R_d$ minimizes resonance peak as long as it is larger than the minimum value required for stability. However, limitations of the demanded phase currents also constrain $R_d$ choice. When output current approaches zero, large damping current $\boldsymbol{i}_{Rh}^{dq}$ results from a small $R_d$ causes the demanded phase current $\boldsymbol{i}_i^*$ to exceed the maximum output current realizable value. In this situation, the required damping current is no longer realizable because of demanded phase current saturation. The saturation phenomenon also occurs when AC–DC MC produces maximum output voltage $U_{o\_max}$. Fig. 10 shows an example of the saturation phenomenon, in which $i_{i\_max}^d$ is the maximum input current in the *d*-axis and can be obtained as

$$i_{i\_max}^d = \frac{U_{o\_max}^2}{R \cdot u_i^d} \tag{26}$$

Normally, damping current $\boldsymbol{i}_{Rh}^{dq}$ contains only AC components and does not have any average value in the *d*- or *q*-axis. Thus, introducing the AD method does not influence input active and reactive power. However, the damping current obtains a negative bias in the *d*-axis under the aforementioned saturation conditions (Fig. 9). This deteriorates the input current waveform and causes undesirable interaction with the output voltage because of the distorted damping current.

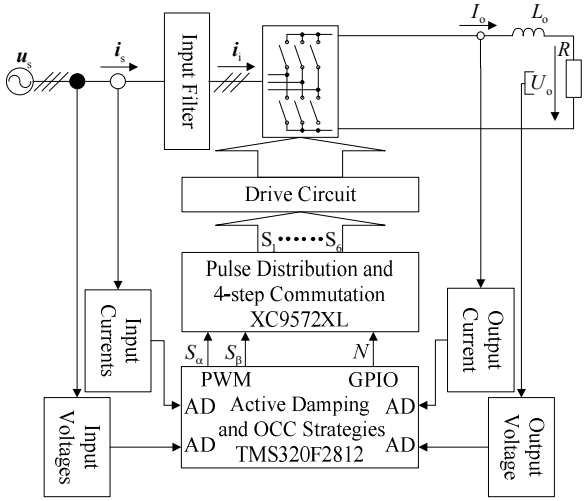



Fig. 11. Experimental configuration.

Damping resistance greater than the minimum value required for stability should be considered to avoid the saturation phenomenon and allow for reasonable gain and phase margins. For the system in this study, $L_i$=3 mH, $C_i$=13 μF, and resonance frequency is 805 Hz; the recommended AD resistance is 25 Ω.

## V. EXPERIMENTAL VERIFICATION

Fig. 11 shows the configuration of an experimental prototype built for hardware verification. The implementation setup consists of a control broad containing Texas Instruments TMS320F2812 DSP and a Xilinx XC9572XL complex programmable logic device (CPLD), an analog broad containing voltage and current sensors, and a power circuit realized by insulated gate bipolar transistors (IGBT).

The power supply phase voltage is 60 V/50 Hz; output load is $R$=25 Ω; input filter parameters are $L_i$=3 mH, and $C_i$=13 μF; output inductor is 5 mH; switching frequency is 12 kHz;

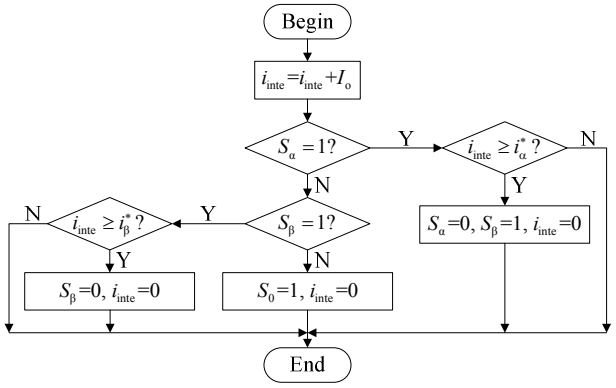



Fig. 12. ISR program flow chart of timer 2.

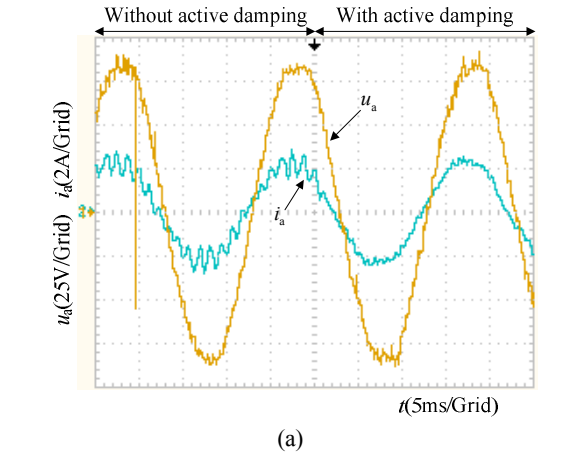



Fig. 13. Experimental waveform of grid-side input current and its FFT: (a) grid-side phase current and voltage; (b) FFT of $i_a$ without the AD method; and (c) FFT of $i_a$ with the AD method.

demanded output voltage $U_o^*$ is 80 V, and damping resistance is 25 Ω.

The DSP carries out the proposed control strategy by timer 1 and timer 2 in the event manager A module. Timing periods

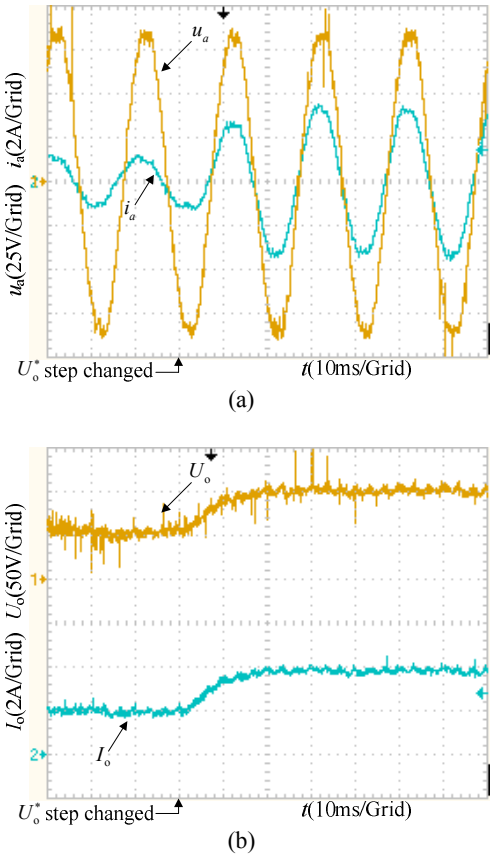
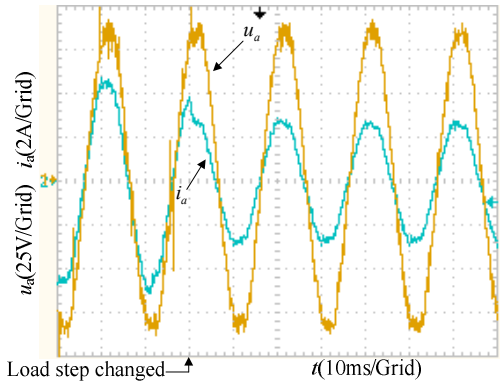


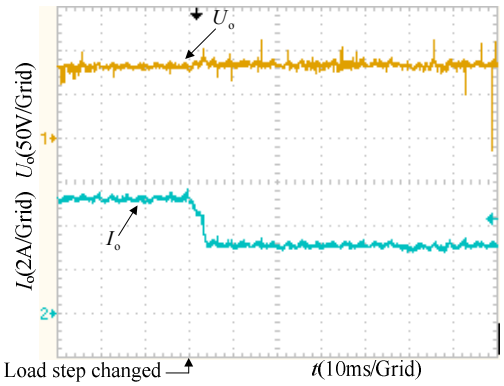

Fig. 14. Experimental results when demanded output voltage $U_o^*$ changes from 50V to 100V: (a) grid-side phase current and voltage and (b) output current and voltage.

of the two timers are set to 1/12000s and 1/120000s, respectively. The interrupt service routine (ISR) of timer 1 is programmed to calculate demanded phase current $\boldsymbol{i}_i^*$ according to measurements of practical input and output voltages and currents, as well as to determine the sector number and current references $i_\alpha^*$ and $i_\beta^*$. Timer 2 samples and integrates the output current to realize the OCC control of the input current. Fig. 12 shows a program flow chart for this process. The obtained sector number $N$ and switching signals $S_\alpha$, $S_\beta$, and $S_0$ are outputted to CPLD for pulse distribution. CPLD also carries out the 4-step commutation strategy [21]. The experimental results are shown in Fig. 13 to Fig. 15.

The system experimental results with and without AD control are given in Fig. 13. When AD control is disabled, the grid-side current is highly distorted because of the input filter resonance frequency. Fig. 13(b) shows that the waveform contains 15$^{th}$ and 17$^{th}$ harmonics with magnitudes as high as 10% and 17% of the fundamental. When AD control is activated, the grid-side current improves. This condition is reflected in the resulting sinusoidal waveform and its FFT spectrum, where oscillation is significantly suppressed and the THD value is reduced from 18.75% to 5.23%.




(a)




(b)

Fig. 15. Experimental results when load resistor changes from 15 Ω to 25 Ω: (a) grid-side phase current and voltage and (b) output current and voltage.

Fig. 14 and Fig. 15 provide the dynamic response of the OCC-controlled AC–DC matrix converter that always includes the AD method.

Fig. 14 shows that load resistance remains at 25 Ω and demanded output voltage $U_o^*$ changes from 50 V to 100 V. Error between the reference and actual output voltage causes the demanded input phase current $\boldsymbol{i}_i^*$ to change. Practical input currents can track their references in one switching cycle with the OCC control. Therefore, the dynamic performance of AC–DC MC relies mainly on the PI controller-based output voltage regulator. The experimental results show that output voltage reaches a new stable state in approximately 0.03 s.

Fig. 15 shows load resistance sharply changing from 15 Ω to 25 Ω, whereas output voltage reference keeps constant. Load changes accurately and immediately cause practical output voltage changes because of the AC–DC MC current source instinct; this disturbance is similar when demanded output voltage is changed. Fig. 15 also shows that grid-side and output currents reach their stable values smoothly in less than 0.01 s, whereas output voltage remains constant without any large oscillations in the transient process.

## VI. Conclusions

Our research proposes a novel control scheme for AC–DC MC by taking advantage of the one-cycle control strategy and the AD technique to mitigate input filter resonance. We developed the principle of the AD method and discussed the guidelines for selecting the damping resistance value. The AD method suppresses LC resonances caused by the power source or by the converter itself. Therefore, grid-side current waveform quality is significantly improved. The OCC control strategy significantly simplifies AD method implementation because of its flexibility and the absence of complex and explicit modulation index control in the proposed scheme. Our experimental results verify these advantages, strengthening the attractiveness of AC–DC MC for future power converter applications.

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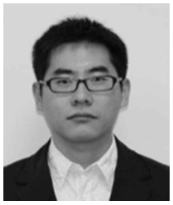

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