

Adaptive DC-link Voltage Control for Shunt Active Power Filter

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Abstract

This study analyzes the mathematical relationship between DC-link voltage and system parameters for shunt active power filters (APFs). Analysis and mathematical deduction are used to determine the required minimum DC-link voltage for APF. A novel adaptive DC-link voltage controller for the three-phase four-wire shunt APF is then proposed. In this controller, the DC-link voltage reference value will be maintained at the required minimum voltage level. Therefore, power consumption and switching loss will effectively decrease. The DC-link voltage can also adaptively yield different DC-link voltage levels based on different harmonic currents and grid voltage levels and thus avoid the effects of harmonic current and grid voltage fluctuation on compensation performance. Finally, representative simulation and experimental results in a three-phase four-wire center-split shunt APF are presented to verify the validity and effectiveness of the minimum DC-link voltage design and the proposed adaptive DC-link voltage controller.

Keywords: Active power filter, Adaptive DC-link voltage controller, Compensation performance, Minimum DC-link voltage

I. INTRODUCTION

The rapid development of power electronics technology over the past decades resulted in the wide installation of power electronic devices. A large number of harmonic currents were injected into the grid; these currents consequently degraded power quality and negatively affected power systems [1]. As a result, harmonic control has become a widely studied issue [2]. Active power filters (APFs) can detect and compensate system harmonics and reactive power in real time, thus reducing the harmonic effect on the grid and ensuring efficient operation [3]. Compared with passive filters, APFs exhibit superior dynamic response, real-time capability, and controllability, which make these filters ideal for compensating harmonics and improving power quality [4].

To ensure the proper operation of APFs, DC-link voltage must be stabilized at a sufficiently high level, which ensures that the APF production of compensating current strictly adheres to control requirements to achieve the desired compensation effect [5]. However, high DC-link voltage requires large capacity to withstand capacitor voltage. This

requirement significantly increases power consumption. Moreover, high DC-link voltage increases switching loss and switching noise [6], [7]. Therefore, the design of DC-link voltage value is an important task that requires detailed quantitative analysis and specification.

Only a few studies have investigated the APF control algorithm with DC-link voltage control [8]-[10], and discussion on the mathematical deduction of the minimum DC-link voltage for APF is limited. In [11], the effect of DC-link voltage on APF compensation characteristic was examined by focusing on the 5th negative and 7th positive harmonic sequences. The lowest required DC-link voltage is presented for the linear modulation range. However, focusing only on the 5th and 7th harmonics is insufficient, and the method used to determine a DC-link voltage was extremely complex to implement. In [12], the influence of DC-link voltage on APF the performance was analyzed, and a specification of the DC-link voltage rated value was presented. However, the Fourier transform analysis of harmonic current to obtain the expression used in this research only focused on a specified harmonic. Thus, various harmonics in practical applications may present a potential problem. In [13]-[15], a minimum DC-link voltage design for a power quality compensator and three-phase four-wire APFs with and without a neutral inductor were proposed. However, the influence of DC-link voltages,

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which were larger than the minimum value, on system performance was not investigated. Based on the analysis in [13]-[15], an adaptive DC-link voltage controller in which the DC-link voltage can be adaptively changed according to different reactive power compensations was deduced and proposed for the LC coupling hybrid APF with and without a neutral inductor [16], [17]. However, the inherent influence between the reactive power compensation and the DC-link voltage control was not discussed, and the proposed adaptive DC-link voltage control algorithm did not consider the harmonic current.

An adaptive DC-link voltage control algorithm for the three-phase four-wire center-split shunt APF remains lacking. In practical applications, grid voltage level varies under certain conditions, such that a large fluctuation may occur. The existing literature is deficient in that no mathematical deduction considered the APF DC-link voltage, the load harmonic current, and grid voltage level, and most shunt APF topologies operate at a fixed DC-link voltage level [5]-[12] [18]-[21]. In such case, changes in load may affect the performance of APFs with a fixed DC-link voltage. Moreover, APF compensation performance may not be guaranteed when the load harmonic current and grid voltage level fluctuate. Power consumption and switching loss are directly proportional to DC-link voltage [22], which suggests that APF will incur a large power consumption and high switching loss if high DC-link voltage is used, and vice versa. Therefore, if the DC-link voltage can be adaptively changed according to the variation of harmonic current and grid voltage level, the APF can operate under different minimum required DC-link voltage level s, such that compensation performance can be guarantee with low power consumption and switching loss.

The remainder of this paper is organized as follows: Section II presents a three-phase four-wire center-split shunt APF and its corresponding single-phase equivalent circuit model. Section III takes this model as a basis to analyze the relationship between DC-link voltage and system parameters, such that the required minimum DC-link voltage for APF can be deduced. Section IV presents the adaptive DC-link voltage controller for three-phase four-wire shunt APFs. Sections V and VI discuss the simulation and experimental verification of the minimum DC-link voltage deduction and the proposed adaptive DC-link voltage controller, respectively. Finally, Section VII concludes.

II. THREE-PHASE FOUR-WIRE CENTER-SPLIT SHUNT APF AND ITS SINGLE-PHASE CIRCUIT MODEL

The circuit of the three-phase four-wire center-split shunt APF is shown in Fig. 1. u_{sx} is the grid voltage, and u_{cx} is the inverter voltage. i_{sx} , i_{Lx} , and i_{cx} are the grid, load, and compensating currents for each phase, respectively, where

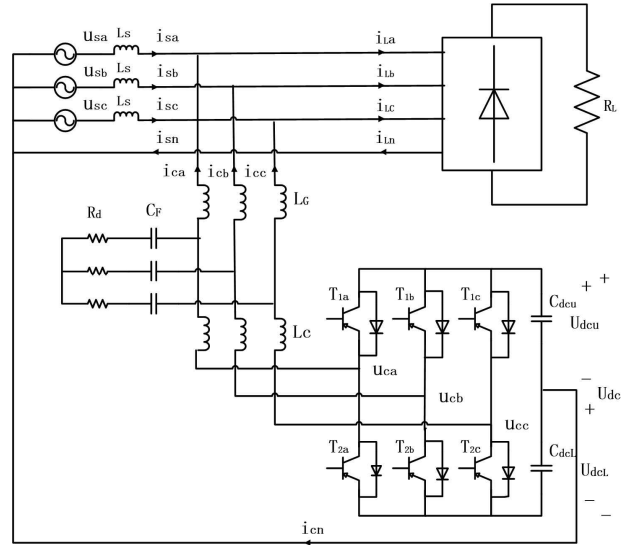


Fig. 1. Circuit of the three-phase four-wire center-split shunt APF.

subscript x denotes phases a , b , c , and n . C_{dc} and U_{dc} are the DC-link capacitor and DC-link voltages, respectively, and the upper and lower DC-link capacitor voltages are $U_{dcU} = U_{dcL} = 0.5 U_{dc}$. L_s is the grid inductor and is normally neglected because of its relatively low value. The non-linear load is composed of a three-phase full-bridge rectifier and a resistance R_L , which serves as a harmonic-producing load. The LCL filter that consists of L_c , L_g , and C_f is used to filter out the harmonics at switching frequency. R_d is used to suppress the resonance peak of the LCL filter at resonance frequency and to maintain system stability.

The single-phase equivalent circuit model from the three-phase four-wire center-split shunt APF circuit configuration is shown in Fig. 2. u_s is the grid voltage, u_c is the inverter voltage, u_L is the inductor voltage, and i_c is the compensating current. An LCL filter behaves in a manner similar to an inductor at a low-frequency range below 2.5 kHz, and the common APF output current requirement depends on the 50th harmonic; thus, only the frequency range below 2.5 kHz have to be considered in control system design [23]. As a result, the LCL filter can reasonably be simplified as an inductor in the low-frequency range. The inductance value of this filter is determined by $L = L_c + L_g$, whereas R is the equivalent resistance of the inductor.

III. MINIMUM DC-LINK VOLTAGE DEDUCTION FOR THE THREE-PHASE FOUR-WIRE SHUNT APF

According to Kirchhoff's voltage law, the following voltage equation can be obtained by employing the single-phase equivalent circuit in Fig. 2:

$$\begin{aligned} u_c &= u_s + u_L \\ &= u_s + R \cdot i_c + L \cdot \frac{di_c}{dt} \end{aligned} \quad (1)$$

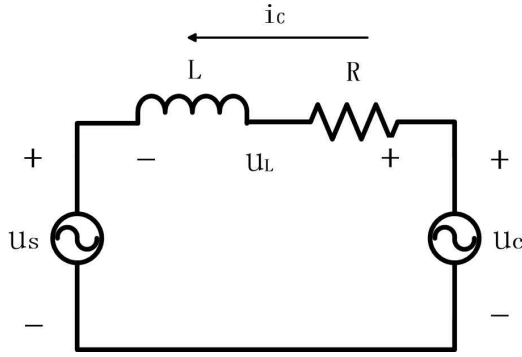


Fig. 2. APF single-phase equivalent circuit model.

To facilitate a detailed analysis, the grid and inverter voltages are defined as

$$u_s = \sqrt{2}U_{sn} \cos(\omega t + \theta_1) \quad (2)$$

$$u_c = U_{c1} \cos(\omega t + \varphi_1) + \sum_{n=2}^{\infty} U_{cn} \cos(n\omega t + \varphi_n) \quad (3)$$

where U_{sn} is the effective value of the grid voltage; U_{c1} and U_{cn} are the effective values of the fundamental and n^{th} components of the inverter voltage, respectively; ω is the fundamental angular frequency; and θ and φ represent the initial phase angles of each component.

Assuming that the non-linear load current i_L is composed of the load fundamental current i_{L1} and the load harmonic current i_{Lh} , we derive

$$\begin{aligned} i_L &= i_{L1} + i_{Lh} \\ &= I_{L1} \cos(\omega t + \theta_1) + \sum_{n=2}^{\infty} I_{Ln} \cos(n\omega t + \theta_n) \end{aligned} \quad (4)$$

where I_{L1} and I_{Lh} are the effective values of the fundamental and n^{th} harmonic currents, respectively.

Assuming that the APF output current i_C is composed of the fundamental component i_{C1} and the harmonic component i_{Ch} , we derive

$$\begin{aligned} i_C &= i_{C1} + i_{Ch} \\ &= I_{C1} \cos(\omega t + \theta_1) + \sum_{n=2}^{\infty} I_{Cn} \cos(n\omega t + \theta_n) \end{aligned} \quad (5)$$

The fundamental current I_{C1} , which maintains the DC-link voltage and system power loss, is very small ($I_{C1} \approx 0$) under a steady-state situation, such that the fundamental component of the APF output current i_{C1} can be simply neglected under a steady state ($i_{C1} = 0$) [16]. To compensate the load harmonics, the effect of the non-linear loads on power grid is eliminated by ensuring that the compensating harmonic current generated by APF is equal to the harmonic component of load current. Therefore, the APF output current i_C can be rewritten as

$$i_C = i_{Ch} = i_{Lh} = \sum_{n=2}^{\infty} I_{Ln} \cos(n\omega t + \theta_n) \quad (6)$$

Substituting (2), (3), and (6) into (1), the voltage equation

becomes

$$\begin{aligned} &U_{c1} \cos(\omega t + \varphi_1) + \sum_{n=2}^{\infty} U_{cn} \cos(n\omega t + \varphi_n) \\ &= \sqrt{2}U_{sn} \cos(\omega t + \theta_1) + R \cdot \sum_{n=2}^{\infty} I_{Ln} \cos(n\omega t + \theta_n) \\ &\quad + L \cdot \frac{d\{\sum_{n=2}^{\infty} I_{Ln} \cos(n\omega t + \theta_n)\}}{dt} \end{aligned} \quad (7)$$

According to Euler's formula, the grid voltage, inverter voltage, and compensating current can be expressed as

$$\begin{cases} \sqrt{2}U_{sn} \cos(\omega t + \theta_1) = \sqrt{2}U_{sn} \operatorname{Re}[e^{j(\omega t + \theta_1)}] \\ U_{c1} \cos(\omega t + \varphi_1) = U_{c1} \operatorname{Re}[e^{j(\omega t + \varphi_1)}] \\ \sum_{n=2}^{\infty} U_{cn} \cos(n\omega t + \varphi_n) = \sum_{n=2}^{\infty} U_{cn} \operatorname{Re}[e^{j(n\omega t + \varphi_n)}] \\ \sum_{n=2}^{\infty} I_{Ln} \cos(n\omega t + \theta_n) = \sum_{n=2}^{\infty} I_{Ln} \operatorname{Re}[e^{j(n\omega t + \theta_n)}] \end{cases} \quad (8)$$

where $\operatorname{Re}[*]$ is the operation symbol for extracting the real part of plural.

Substituting (8) into (7), the voltage equation becomes

$$\begin{aligned} &U_{c1} \operatorname{Re}[e^{j(\omega t + \varphi_1)}] + \sum_{n=2}^{\infty} U_{cn} \operatorname{Re}[e^{j(n\omega t + \varphi_n)}] \\ &= \sqrt{2}U_{sn} \operatorname{Re}[e^{j(\omega t + \theta_1)}] + R \cdot \sum_{n=2}^{\infty} I_{Ln} \operatorname{Re}[e^{j(n\omega t + \theta_n)}] \\ &\quad + L \cdot \sum_{n=2}^{\infty} I_{Ln} \operatorname{Re}[jn\omega e^{j(n\omega t + \theta_n)}] \end{aligned} \quad (9)$$

In (9), the corresponding parts on both sides of the equation are the same frequency sinusoidal vector. Thus, Equation (10) can be derived when the real part extracting operation symbol Re is removed from either side of Equation (9).

$$\begin{aligned} &U_{c1} e^{j(\omega t + \varphi_1)} + \sum_{n=2}^{\infty} U_{cn} e^{j(n\omega t + \varphi_n)} \\ &= \sqrt{2}U_{sn} e^{j(\omega t + \theta_1)} + R \cdot \sum_{n=2}^{\infty} I_{Ln} e^{j(n\omega t + \theta_n)} + L \cdot \sum_{n=2}^{\infty} I_{Ln} jn\omega e^{j(n\omega t + \theta_n)} \end{aligned} \quad (10)$$

In (10), the real and imaginary parts on both sides of the equation are equal. Thus, the following equations can be obtained:

$$\begin{cases} U_{c1} = \sqrt{2}U_{sn} \\ \sum_{n=2}^{\infty} U_{cn} = R \cdot \sum_{n=2}^{\infty} I_{Ln} + \omega L \cdot \sum_{n=2}^{\infty} n I_{Ln} \end{cases} \quad (11)$$

The mold length of the inverter output voltage vector is defined as

$$U_c = \| U_{c1} e^{j(\omega t + \varphi_1)} + \sum_{n=2}^{\infty} U_{cn} e^{j(n\omega t + \varphi_n)} \| \quad (12)$$

According to (11) and (12), the maximal mold length of the inverter voltage vector can be expressed as

$$U_{c_max} = U_{c1} + \sum_{n=2}^{\infty} U_{cn} \quad (13)$$

$$= \sqrt{2}U_{sn} + R \cdot \sum_{n=2}^{\infty} I_{Ln} + \omega L \cdot \sum_{n=2}^{\infty} n I_{Ln}$$

To provide sufficient DC-link voltage to compensate the load harmonic current, the relationship between the DC-link voltage and the maximal value of inverter voltage mold is given by

$$U_{c_max} = \frac{m}{2} U_{dc} \quad (14)$$

where m denotes the modulation index.

APF must be capable of producing a voltage that exceeds the maximal value of the inverter voltage vector mold to compensate the harmonic current produced by the nonlinear load completely. Substituting (13) into (14), the minimum DC-link voltage for the single-phase equivalent circuit model is obtained as

$$U_{dc_min} = \frac{2}{m} U_{c_max} \quad (15)$$

$$= \frac{2}{m} (\sqrt{2}U_{sn} + R \cdot \sum_{n=2}^{\infty} I_{Ln} + \omega L \cdot \sum_{n=2}^{\infty} n I_{Ln})$$

Some conclusions can be inferred from (15). First, with different grid voltage levels, coupling inductor values, equivalent resistances of the inductor, modulation indexes, and harmonic current contents, the APF requires different minimum DC-link voltage levels for operation. In addition, the value of the output inductor and its equivalent resistor affect the pulse-width modulation inverter output voltage component and the required minimum DC-link voltage, which should be considered in designing the output LCL filter. The modulation index is also an important factor to determine the minimum DC-link voltage level. Thus, the required DC-link voltage when using the Space Vector Pulse Width Modulation (SVPWM) modulation method ($m = 1.1547$) [24] is lower than that when using the triangular PWM method ($m = 1$).

The current harmonics in each phase can be independently compensated in the three-phase four-wire APF [25]. Thus, the final required minimum DC-link voltage for the three-phase four-wire center-split APF will be the maximum among the calculated minimum values of each phase, as expressed in (15). Thus, the deduced minimum DC-link voltage expression can be used for both balanced and unbalanced loads.

$$U_{dc} = \max(U_{dca_min}, U_{dcb_min}, U_{dcc_min}) \quad (16)$$

IV. MINIMUM DC-LINK VOLTAGE DEDUCTION FOR THE THREE-PHASE FOUR-WIRE SHUNT APF

Equation (15) can be rewritten as

$$\frac{m}{2} U_{dc_min} - \sqrt{2}U_{sn} = R \cdot \sum_{n=2}^{\infty} I_{Ln} + \omega L \cdot \sum_{n=2}^{\infty} n I_{Ln} \quad (17)$$

The right side of (17) can be written as

$$\Delta U = R \cdot \sum_{n=2}^{\infty} I_{Ln} + \omega L \cdot \sum_{n=2}^{\infty} n I_{Ln} \quad (18)$$

In (18), ΔU can be considered as the load harmonic contents that have to be compensated, as determined by the harmonic current. ΔU will increase when the harmonic current increases but decrease when the harmonic current decreases. In practical applications, the harmonic current frequently varies. Thus, the required minimum DC-link voltage will change with harmonic current variation. However, the APF topologies operate at a fixed DC-link voltage level in most existing studies [5]–[12]. According to the minimum DC-link voltage deduction, when the harmonic current decreases, a low DC-link voltage can facilitate normal APF function, which indicates that a fixed DC-link voltage results in additional power consumption and switch loss. Moreover, when the harmonic current increases, the DC-link requires a higher voltage level to ensure normal operation. In other words, a fixed DC-link voltage may result in an insufficient DC-link voltage that affects the normal operation and compensation effect of APF.

Based on (17) and (18), the left side of (17) can be written as

$$\Delta U = \frac{m}{2} U_{dc_min} - \sqrt{2}U_{sn} \quad (19)$$

Equation (19) shows that ΔU can also be considered as the capability of APF to output a harmonic compensating current. Therefore, when the current modulation method in which the modulation index m is fixed has been determined, both DC-link voltage and grid voltage level affect the APF output compensating current capability and consequently influence APF compensation performance. Increasing the DC-link voltage can increase ΔU and thus improve APF compensation capability. Conversely, decreasing the DC-link voltage will reduce ΔU and thus diminish APF compensation capability. Similarly, decreasing the grid voltage level increases ΔU larger and thus improves APF compensation performance, whereas increasing the grid voltage level decreases ΔU and thus deteriorates APF compensation performance.

In the literature, APF topologies operate at a fixed DC-link voltage level [5]–[12]. However, in industrial applications, the grid voltage level is not constant. Such level may vary under certain circumstances and may even exhibit large fluctuations. Thus, APF is generally designed to function normally under the condition of grid voltage level fluctuation within $\pm 10\%$. When the grid voltage level drops, low DC-link voltage can still achieve comparable compensation capability. That is, fixed DC-link voltage results in additional power consumption. Furthermore, when the grid voltage level increases, the capability of the APF output compensating current will decrease at a fixed DC-link voltage. Assuming that the effective value of the grid voltage is $U_{sn} = 220$ V, the modulation index is $m = 1.1547$, and the LCL output filter

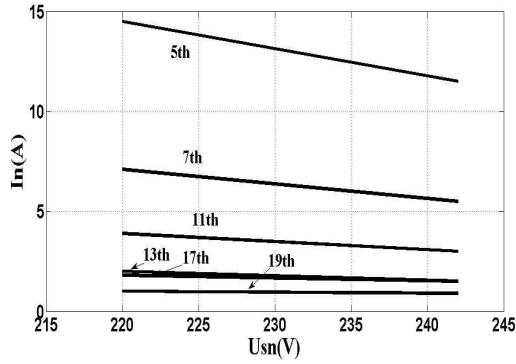


Fig. 3. Capability of APF compensating current change with various grid voltage levels.

inductance is $L = 0.45$ mH [23]. These system parameters are listed in Table I of Section V. The increase in APF output compensating current with increasing grid voltage level is shown in Fig. 3. When the APF is operated under normal condition $U_{sn} = 220$ V, the peak value of the APF output 5th harmonic compensating current is $i_{5th} = 14.5$ A. When the effective values of the grid voltage increase to $U_{sn} = 225, 231, 236$, and 242 V, the values of the APF output 5th harmonic compensating current decrease to $i_{5th} = 13.8, 13.1, 12.3$, and 11.5 A at a percentage decline of approximately 4.83%, 9.66%, 15.17%, and 20.69%, respectively. Furthermore, the peak value of the APF output 7th harmonic compensating current is $i_{7th} = 7.25$ A when $U_{sn} = 220$ V. When the effective values of the grid voltage increase to $U_{sn} = 225, 231, 236$, and 242 V, the values of the APF output 7th harmonic compensating current decrease to $i_{7th} = 6.87, 6.5, 6.01$, and 5.5 A at a percentage decline of approximately 5.24%, 10.34%, 17.11%, and 23.14%, respectively. A similar phenomenon occurs in other order harmonic compensating currents. In this situation, the APF output compensating current capability decreases. Consequently, compensation performance may not be guaranteed.

To solve the abovementioned problems, an adaptive DC-link voltage controller for the three-phase four-wire shunt APF is proposed in this section. This controller consists of three main blocks: determination of minimum DC-link voltage, adaptive reference DC-link voltage level, and DC-link voltage feedback PI controller blocks. The proposed adaptive DC-link voltage control block diagram for the three-phase four-wire shunt APF is shown in Fig. 4.

A. Determination of Minimum DC-link Voltage

The required minimum DC-link voltage U_{dc-min} for APF can initially be calculated according to the deduction in Section III. Based on the grid voltage level, coupling inductor value, modulation index, and harmonic current contents, the required minimum DC-link voltage value for APF is set from (1) to (16). When the minimum DC-link voltage value is affected by other factors, such as the change in the inductance

and resistance values at different temperatures during operation. When these factors are considered, a voltage margin U_{dc-mar} , which is shown in Equation (20), would be added to the minimum DC-link voltage level to avoid an insufficient DC-link voltage level even when the parameters of the output inductance filter and its equivalent resistance exhibit a 20% variation. This condition enhances the reliability of the block and absolutely guarantees the normal operation of APF.

$$U_{dc-mar} = 20\% \cdot R \cdot \sum_{n=2}^{\infty} I_{Ln} + 20\% \cdot \omega L \cdot \sum_{n=2}^{\infty} n \cdot I_{Ln} \quad (20)$$

To implement the adaptive DC-link voltage control function, $U_{dc-ref} = U_{dc-min} + U_{dc-mar}$ can be simply treated as the initial reference DC-link voltage.

B. Adaptive DC-link Voltage Reference Level

Based on Equation (18), the reference DC-link voltage can be written as

$$U_{dc-ref} = \frac{2}{m} (\Delta U + \sqrt{2} U_{sn}) \quad (21)$$

Equation (21) shows that the reference DC-link voltage U_{dc-ref} is determined by ΔU and U_{sn} . An adaptive controller can be designed to adjust the DC-link voltage reference value when the harmonic current and grid voltage level fluctuate.

Given that ΔU changes with harmonic current variation, determining different values requires the minimum DC-link voltage level. The adaptive DC-link voltage controller will adjust the DC-link voltage value when the harmonic current content changes, thus maintaining the DC-link voltage at the required minimum DC-link voltage and avoiding a case in which DC-link voltage is insufficient.

However, the required minimum DC-link voltage may frequently change as the load harmonic current varies, which randomly occurs. In this situation, the frequent change causes a rapid DC-link voltage fluctuation, which deteriorates APF operational performance. To mitigate this problem, the initial reference DC-link voltage will not be reset until a significant change in load is detected, such that the reference DC-link voltage can be maintained as a constant value within a specific range.

The controller will adaptively yield different DC-link voltage reference levels not only when the harmonic current changes, but also when the grid voltage level changes. The APF output harmonic current capability after applying the adaptive controller is shown in Fig. 5. Compared with that in Fig. 3 without the adaptive controller, the peak value of the APF output 5th harmonic compensating current is still maintained at approximately $i_{5th} = 14.4$ A, although the effective value of the grid voltage increases to $U_{sn} = 225, 231, 236$, and 242 V. In addition, the APF output 7th, 11th, 13th, 17th, and 19th harmonic compensating currents are also maintained at approximately $i_{7th} = 7.25$ A, $i_{11th} = 4$ A, $i_{13th} = 2$

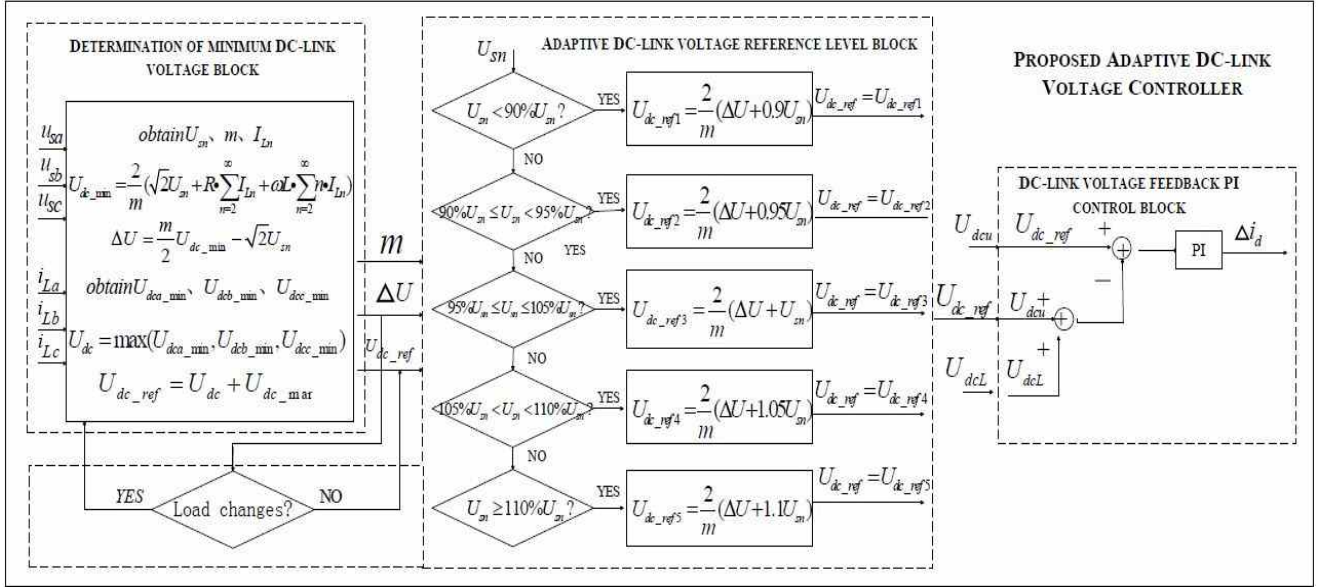


Fig. 4. Proposed adaptive DC-link voltage control block diagram for the three-phase four-wire shunt APF.

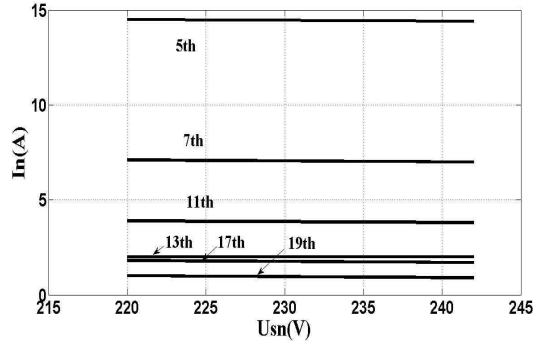


Fig. 5. Capability for APF compensating current change with various grid voltages when the adaptive voltage controller is applied.

A, $i_{17th} = 1.75$ A, and $i_{19th} = 1$ A, respectively. This result shows that when the adaptive voltage controller is applied, the APF output compensating capability is unaffected by grid voltage level fluctuation.

Nevertheless, the DC-link reference voltage may frequently change as the grid voltage varies occasionally. To mitigate this problem, the final reference DC-link voltage is classified into certain levels for selection. This classification depends on the different ranges of grid voltage level, as shown in Fig. 4, such that the reference DC-link voltage can be maintained as a constant value within a specific range [26]. In this way, the problem with DC-link voltage reference value fluctuation under adaptive voltage control method can be addressed. Finally, when the modulation index m and ΔU determined by harmonic current are fixed, the DC-link voltage reference value will be automatically adjusted with the variation of grid voltage level. The DC-link voltage reference value range is shown in Fig. 6.

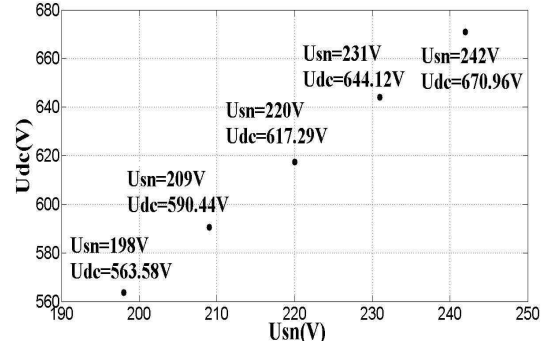


Fig. 6. DC-link voltage reference value range when using the adaptive voltage controller.

The switching loss of the switching device can be classified as turn-on and turn-off losses. Equation (22) gives the total turn-on and turn-off power losses [22], where U_{dc} , I_{CM} , I_{CN} , t_{RN} , t_{FN} , and f_{SW} are the DC-link voltage, maximum collector current, rated collector current, rated rise time, rated fall time, and switching frequency, respectively. Thus, a higher APF DC-link voltage results in a higher the switching loss, and vice versa [15] [22]. If the DC-link voltage adaptively yields at the minimum DC-link voltage level according to different harmonic currents and grid voltage levels, the APF performance, power consumption, and switching loss will be optimized.

$$P_{loss} = U_{dc} I_{CM} f_{SW} \left(\frac{1}{8} t_{RN} \frac{I_{CM}}{I_{CN}} + t_{FN} \left(\frac{1}{3\pi} + \frac{1}{24} \frac{I_{CM}}{I_{CN}} \right) \right) \quad (22)$$

C. DC-link Voltage Feedback PI Controller

The APF can effectively control the DC-link voltage by feedbacking the DC-link voltage error signal as a positive

fundamental active current component. The PI controller is applied to the DC-link voltage control loop. The DC-link capacitor can obtain energy and maintain a constant value through appropriate control. The difference between the DC-link reference voltage and the actual DC-link voltage is regulated by a PI regular. After regulation, the signal is added to the instantaneous positive fundamental active current component. Therefore, the reference current signal contains a fundamental active current, which indicates that the compensating current contains a fundamental active current component. This condition ensures the energy exchange between the DC and AC sides of APF and maintains the DC-link voltage at a reference level.

Through this adaptive controller, the DC-link voltage reference value will be initially set in the required minimum value, which may reduce power consumption and switching loss on the premise that APF operates normally. Another contribution of this controller is that once the harmonic current and grid voltage level change, the DC-link voltage reference value will be adaptively adjusted. The DC-link voltage reference value will first change according to the change in harmonic current. Then, the DC-link voltage reference value will increase as the grid voltage level increases to ensure efficient APF compensation performance. The DC-link voltage reference value will also decrease when the grid voltage level decreases, thereby reducing power consumption and switching loss. Thus, the optimal control of the DC-link voltage is achieved.

V. SIMULATION AND EXPERIMENTAL VERIFICATION OF MINIMUM DC-LINK VOLTAGE DEDUCTION

Simulations and experiments are performed on the three-phase four-wire shunt APF to verify the performance of the proposed controller. Simulation studies are conducted in MATLAB. A three-phase four-wire center-split shunt APF prototype is also implemented in the laboratory to verify the simulation results (Fig. 7). The simulated and experimental system parameters are listed in Table I. The PI controller is applied to the current control loop, and SVPWM modulation is applied to generate control signals in switches. In this section, the minimum DC-link voltage deduction is initially verified by simulations and experiments.

Without APF, the source currents contain a large amount of harmonics, and the total harmonic distortions (THDs) of the simulation and experimental load current are 24.39% and 25.13%, respectively. Therefore, the source currents are serious distortions. The values of every order harmonic current are listed in Table II. Even-order harmonics are generally largely offset in the three-phase system and can thus be ignored in the calculation process. Given that the load harmonic current beyond the 40th order is small the required minimum DC-link voltage calculation will consider only up to the 40th harmonic order for simplicity.



Fig. 7. Three-phase four-wire center-split shunt APF prototype.

TABLE I

SYSTEM PARAMETERS

Grid Voltage	U_{sn}	220 V
Grid Frequency	f	50 Hz
Switching Frequency	f_s	9.6 kHz
Inductor Filter	L	0.45 mH
Equivalent Resistance	R	0.2 Ω
DC-link Capacitance	$C_{dcu} C_{dcL}$	20000 μ F
Load Resistance	R_L	15 Ω
Modulation Index	m	1.1547

TABLE II

HARMONIC CURRENTS

Harmonic Order	Simulation	Experiment
5th	8.54 A	8.58 A
7th	4.01 A	4.29 A
11th	3.38 A	3.43 A
13th	2.23 A	2.43 A
17th	2.09 A	2.14 A
19th	1.63 A	1.71 A
23rd	1.19 A	1.35 A
25th	1.03 A	1.11 A
29th	0.95 A	1.02 A
31st	0.83 A	0.86 A
35th	0.59 A	0.71 A
37th	0.33 A	0.49 A

Based on the abovementioned deduction and related system parameters, the required minimum DC-link voltage for the APF can be calculated by using Equations (1) to (15). The required minimum DC-link voltages are $U_{dc-ref} = 626.39$ V in simulation and $U_{dc-ref} = 628.38$ V in the experiment.

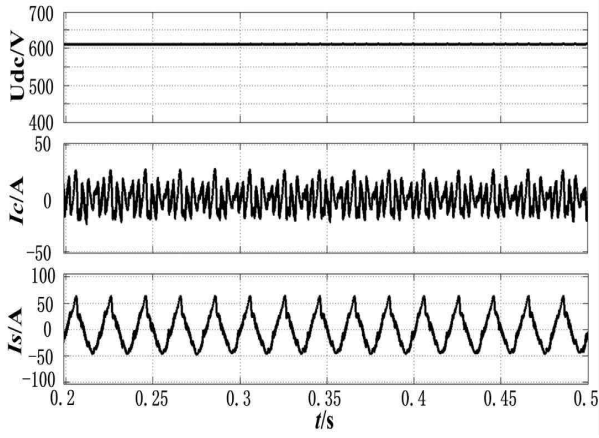


Fig. 8. Simulation DC-link voltage, as well as compensating and source currents when $U_{dc}=610V$.

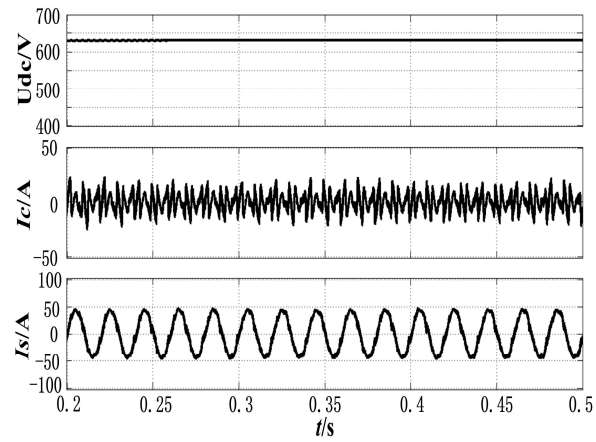


Fig. 9. Simulation DC-link voltage, as well as compensating and source currents when $U_{dc}=630V$.

In simulation, when the DC-link voltage is 610 V, which is lower than the required minimum value of 626.39 V. The THD of the source current after compensation is 13.34%, which does not satisfy the international standard (THD < 8% for IEEE519-1992 [27]). The simulated compensating and source currents when the DC-link voltage $U_{dc} = 610$ V are shown in Fig. 8.

When the DC-link voltage increases to $U_{dc} = 630$ V, which is higher than the required minimum value of 626.39 V, the APF can operate at both inverter and rectifier modes to achieve efficient compensation performance with THD = 6.48%, which meets international standards [27]. The compensating and source currents when the DC-link voltage $U_{dc} = 630$ V are shown in Fig. 9. The harmonics of the load current are significantly compensated. Meanwhile, the source current distortion is almost eliminated, whereas the source current is nearly sinusoidal.

Similar results are also obtained in experiments. When the DC-link voltage is 610 V, which is lower than the required minimum value of 628.38 V, the THD of the source current after compensation is 14.80%. The THD value does not satisfy

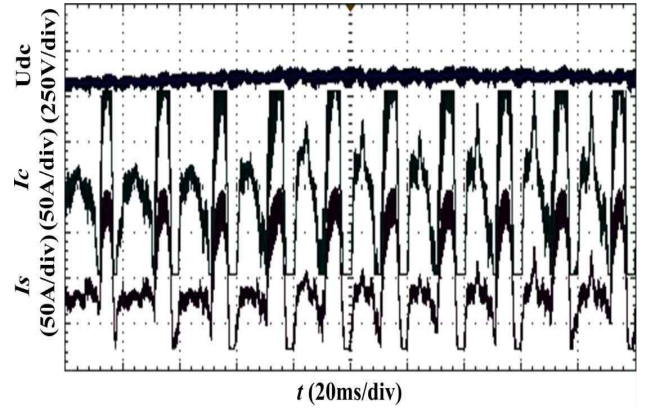


Fig. 10. Experimental DC-link voltage, as well as compensating and source currents when $U_{dc}=590V$.

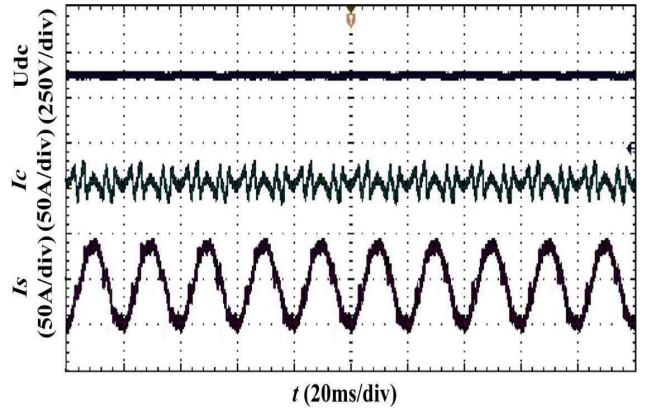


Fig. 11. Experimental DC-link voltage, as well as compensating and source currents when $U_{dc}=630V$.

the international standard because the APF is still operating at an insufficient DC-link voltage level. Moreover, when the reference voltage is further decreased to 590 V, the compensating current is seriously distorted, which distorts the supply current. The THD of the source current soars to 45.16%, a value that is even worse than that without compensation. Fig. 10 shows the experimental compensating and source currents after compensation when the DC-link voltage is $U_{dc} = 590$ V. The DC-link voltage is unstable and uncontrollable. In this case, APF is operating at a poor state, which will negatively affect the power grid, the load, and the APF itself.

When the DC-link voltage increases to $U_{dc} = 630$ V, which is higher than the required minimum value of 628.38 V, the APF achieves an efficient compensation effect with THD = 7.23%, which satisfies international standards [27]. Fig. 11 shows the experimental compensating and source currents after compensation when the DC-link voltage is $U_{dc} = 630$ V.

When the DC-link voltages are increased to $U_{dc} = 650, 670, 690, 710,$ and 730 V, the THDs of the simulated source current are 6.23%, 6.08%, 5.87%, 5.81%, and 5.72%, respectively, whereas the THDs of the experimental source current are 7.11%, 6.92%, 6.77%, 6.58%, and 6.52%, respectively. These THD values obviously meet international standards. Table III

TABLE III
COMPENSATION PERFORMANCES

		THD	
		Simulation	Experiment
Without APF		25.39%	26.13%
DC-link Voltage U_{dc}	590 V	43.70%	45.16%
	610 V	13.34%	14.80%
	630 V	6.48%	7.23%
	650 V	6.23%	7.11%
	670 V	6.08%	6.92%
	690 V	5.87%	6.77%
	710 V	5.81%	6.58%
	730 V	5.72%	6.52%

shows the simulation and experimental compensation results of APF with different DC-link voltages.

The results in Table III show that when the DC-link voltage is lower than the required minimum value, the APF is operating in the rectifier mode, and the variation in THD is large when the DC-link voltage is enhanced. As the DC-link voltage becomes closer to the required minimum value, the compensating performances improves. However, the compensation effect is not realized. Once the DC-link voltage is higher than the required minimum value, the APF can achieve superior compensation performance, in which the THD meets international standards and stabilizes. These simulation and experimental results verify the proposed APF minimum DC-link voltage deduction. Given the different grid voltage levels, coupling inductor values, and load current contents, the APF requires different minimum DC-link voltages for operation.

Based on the simulation and experimental results in Table III, the trade-off relationship between the THD and the DC-link voltage is shown in Fig. 12. When the DC-link voltage is higher than the required minimum value, increasing the value of the DC-link voltage alone cannot significantly improve the compensation effect. By contrast, power consumption and switching loss are directly proportional to the DC-link voltage [22], such that they may increase APF power consumption and loss. Compensation performance can be improved by adjusting the controller parameters or by applying better control algorithms (e.g., improved repetitive control [28], predictive control [29], and fuzzy control [30]), instead of increasing the DC-link voltage. Thus, APF power consumption and loss will not increase, and the APF can still operate in an ideal state, thus compensating the harmonic of load current and eliminating the harmonic pollution.

VI. SIMULATION AND EXPERIMENTAL VERIFICATION OF PROPOSED ADAPTIVE DC-LINK VOLTAGE CONTROLLER

The minimum DC-link voltage design block was verified in

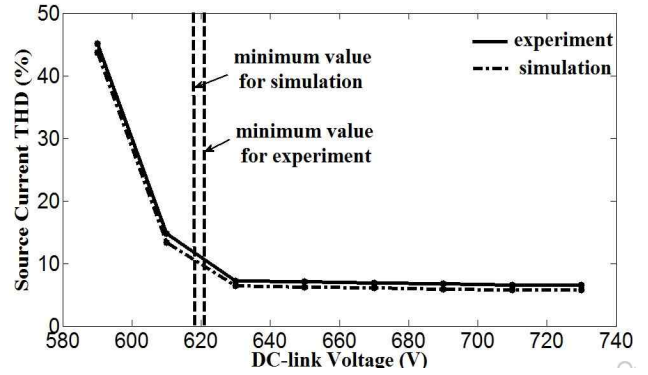


Fig. 12. Relationship between source current THD and DC-link voltage

Section V. In this section, the adaptive reference DC-link voltage level block will be verified by simulations and experiments. The system parameters listed in Table I are applied to maintain the consistency of the simulations and experiments.

The effect of the DC-link voltage controller when the harmonic currents change is analyzed. The fundamental and harmonic currents used to calculate THD do not correspondingly increase exponentially when harmonic currents change. Thus, the use of THD to compare APF performance before and after the harmonic currents change is inappropriate. Therefore, the single-order harmonic elimination rate $R\%$, which is shown in Equation (23), is used to analyze APF performance.

$$R\% = \frac{I_{\text{Before-compensation}} - I_{\text{After-compensation}}}{I_{\text{Before-compensation}}} \quad (23)$$

The harmonic currents of a load with a resistance $R_L = 15$ ohm are $i_{5th} = 8.58$ A, $i_{7th} = 4.29$ A, $i_{11th} = 3.43$ A, $i_{13th} = 2.45$ A, $i_{17th} = 2.14$ A, and $i_{19th} = 1.71$ A. After the compensation of APF with the minimum DC-link voltage $U_{dc-ref} = 630$ V, the harmonic currents are $i_{5th} = 0.26$ A, $i_{7th} = 0.21$ A, $i_{11th} = 0.58$ A, $i_{13th} = 0.25$ A, $i_{17th} = 0.52$ A, and $i_{19th} = 0.41$ A. According to the harmonic elimination rate calculation in (23), the harmonic current elimination rates of each order are 96.97%, 95.11%, 83.19%, 89.79%, 79.71%, and 76.11%.

When the load resistance changes to $R_L = 7.5$ ohm, the fundamental and harmonic currents increase. According to the abovementioned analysis and deduction, the APF-required minimum DC-link voltage increases. Without the adaptive DC-link voltage controller, the DC-link voltage remains at $U_{dc-ref} = 630$ V. The experiment waveform is shown in Fig. 13(a). The harmonic current elimination rates in every order harmonic are 96.14%, 95.01%, 85.82%, 85.89%, 78.63%, and 73.92%, as listed in Table IV. The harmonic current elimination rates for every order harmonic current are lower than the values before the load changes. This result indicates that APF compensation capability decreases with the fixed

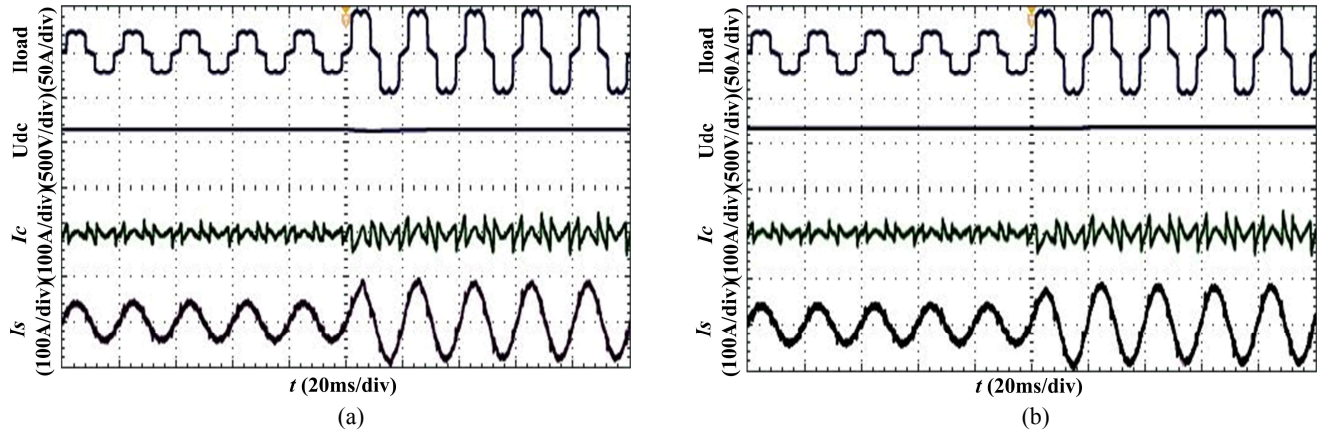


Fig. 13. Experiment waveform when the load changes. (a) Without adaptive voltage controller. (b) With adaptive voltage controller.

TABLE IV

HARMONIC CURRENT COMPENSATION WITH AND WITHOUT ADAPTIVE DC-LINK VOLTAGE CONTROLLER WHEN LOAD CHANGES

U_{dc-ref}	$I_{Fundamental}$	Harmonic order	5 th	7 th	11 th	13 th	17 th	19 th
630 V	50.4 A	Before Compensation	8.57 A	4.29 A	3.43 A	2.45 A	2.14 A	1.71 A
	51.2 A	After Compensation	0.26 A	0.21 A	0.38 A	0.32 A	0.44 A	0.41 A
		Harmonic Eliminate Rate	96.97%	95.11%	88.76%	86.79%	79.71%	76.11%
APF without Adaptive DC-link Voltage Controller When Load Changes (With Fixed DC-Link Voltage)								
630 V	96.51 A	Before Compensation	17.14 A	8.57 A	6.84 A	4.89 A	4.26 A	3.41 A
	100.34 A	After Compensation	0.66 A	0.42 A	0.97 A	0.69 A	0.91 A	0.89 A
		Harmonic Eliminate Rate	96.14%	95.01%	85.82%	85.89%	78.63%	73.92%
APF with Adaptive DC-Link Voltage Controller When Load Changes (With Adaptive DC-Link Voltage)								
645 V	99.8 A	Before Compensation	17.14 A	8.57 A	6.84 A	4.89 A	4.26 A	3.41 A
	100.52 A	After Compensation	0.53 A	0.41 A	0.73 A	0.65 A	0.85 A	0.82 A
		Harmonic Eliminate Rate	96.92%	95.21%	89.32%	86.71%	80.13%	75.96%

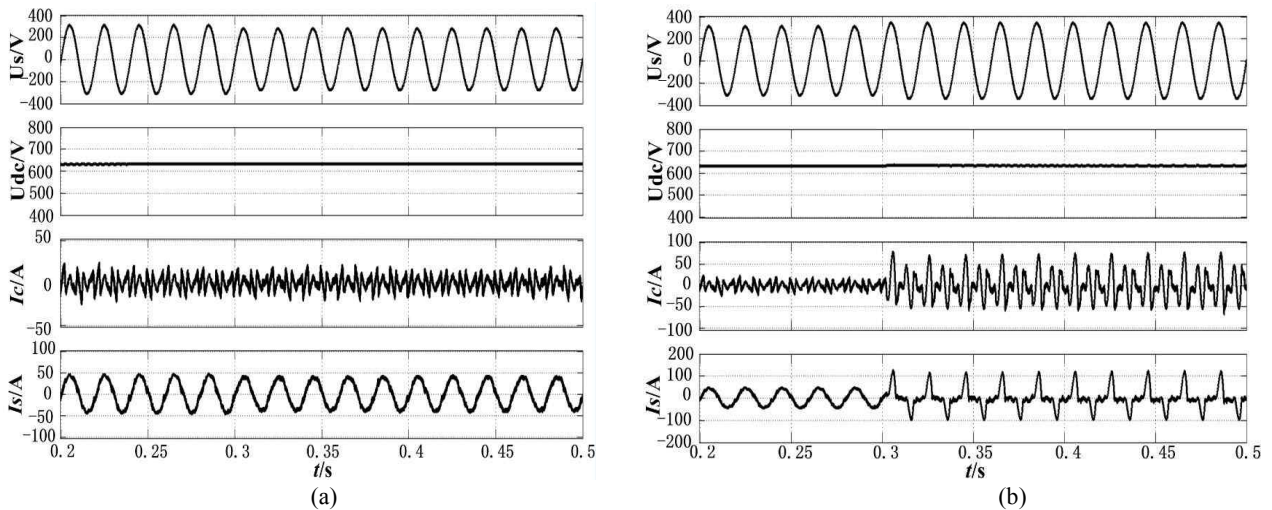


Fig. 14. Simulation waveform without adaptive voltage control when grid voltage level varies $\pm 10\%$, variation occurs at $t = 0.3s$. (a) Grid voltage level changes by -10% . (b) Grid voltage level changes by $+10\%$.

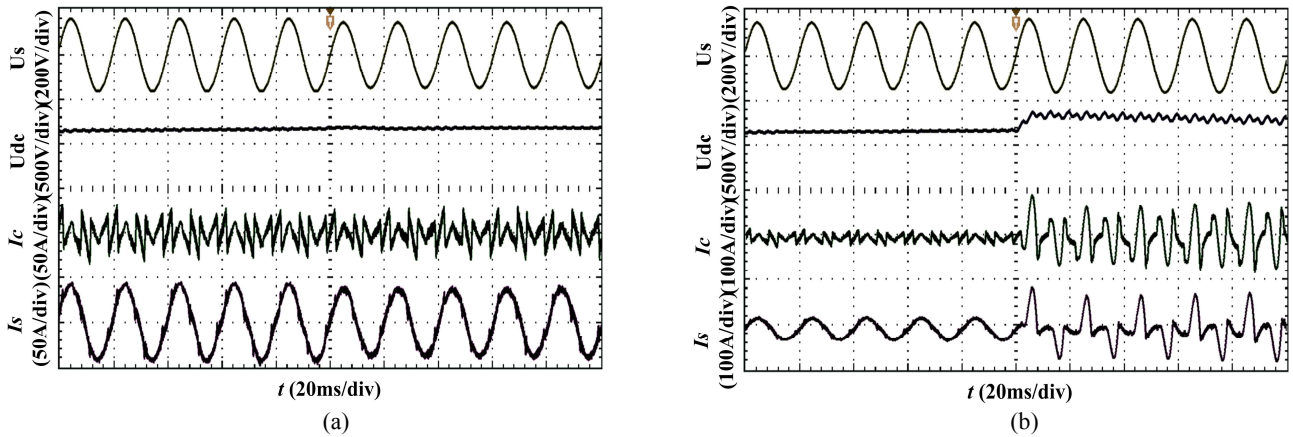


Fig. 15. Experiment waveform without adaptive voltage control when grid voltage level varies $\pm 10\%$. (a) Grid voltage level changes by -10% . (b) Grid voltage level changes by $+10\%$.

TABLE V

COMPENSATION PERFORMANCE WITHOUT ADAPTIVE VOLTAGE CONTROLLER WHEN GRID VOLTAGE LEVEL CHANGES

U_{sn}	U_{dc} (Fixed)	$I_{fundamental}$	THD (Simulation)	$I_{fundamental}$	THD (Experiment)
198 V (90% U_{sn})	630 V	40.21 A	6.29%	40.61 A	7.24%
220 V (U_{sn})	630 V	44.16 A	6.48%	44.58 A	7.33%
242 V (110% U_{sn})	630 V	49.97 A	seriously distorted	50.36 A	seriously distorted

DC-link voltage when harmonic current increases.

Once the adaptive voltage controller is applied, the DC-link voltage value will be adaptively adjusted with harmonic current changes. According to the deduction, the DC-link voltage increases to a new required minimum voltage value of $U_{dc-ref} = 645$ V. The experiment waveform is shown in Fig. 13 (b). The harmonic elimination rates are listed in Table IV. When the DC-link voltage increases to its new minimum voltage with the adaptive controller, the harmonic current elimination rates are 96.92%, 95.21%, 89.32%, 86.71%, 80.13%, and 75.96%, which are almost consistent with the values before the load changes. Thus, the adaptive voltage controller can maintain the DC-link voltage at the required minimum value with the variation of harmonic current, thus avoiding the insufficient DC-link voltage situation and ensuring the harmonic compensation capability of APF.

Thereafter, the effect of the DC-link voltage controller when the grid voltage level changes is analyzed. The condition without the adaptive reference DC-link voltage level block is studied. Based on the verified minimum DC-link voltage design block, the initial minimum DC-link voltage is set at $U_{dc} = 630$ V, which ensures the ideal operation of APF with minimal power consumption and switching loss status. With the fixed DC-link voltage level, Fig. 14 presents the change in compensating and source currents when the grid voltage level changes at $t = 0.3$ s by -10% and 10% in the simulation. Correspondingly, the experimental results when the grid voltage level varies are shown in Fig. 15. Table V outlines the compensation performance. The simulation and experimental

results reflect the effect of the changes in grid voltage level on compensation performance. When the DC-link voltage is fixed, the THD of the source current after compensation will only slightly decrease with a 10% decrease in grid voltage level. Furthermore, when the grid voltage level increases by 10%, the compensating and source currents become seriously distorted because of the insufficient output capability of the fixed DC-link voltage. Meanwhile, the DC-link voltage oscillates and thus becomes unstable and uncontrollable. Hence, the compensation performance cannot be guaranteed, and the system runs under a poor state.

Once the adaptive voltage control block is applied, the DC-link voltage reference value will be adaptively adjusted with the variation of grid voltage level. The simulation and experimental results are shown in Figs. 16 and 17, respectively. The compensation performance with the adaptive controller is presented in Table VI.

The figures show that when the grid voltage level decreases by 10% from 220 V to 198 V, the DC-link voltage level adaptively decreases to a lower value of 580 V, and the THD is unchanged. Meanwhile, DC-link voltage becomes significantly lower than the fixed voltage of 630 V without the adaptive voltage control block. That is, a low DC-link voltage can still realize compensation. Power consumption and switching loss can be effectively decreased compared with the case with fixed DC-link voltage. Given that power consumption and switching loss are directly proportional to the DC-link voltage [22], low DC-link voltage can save on power consumption and reduce switching loss. Moreover, when the

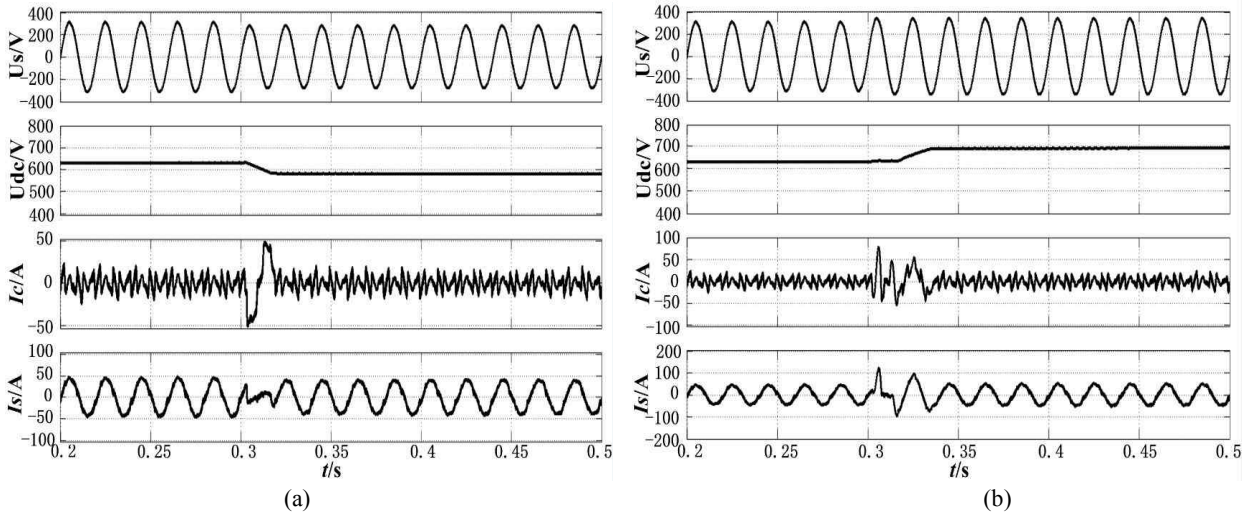


Fig. 16. Simulation waveform with adaptive voltage control when grid voltage level varies $\pm 10\%$, variation happens in $t = 0.3s$. (a) Grid voltage level changes -10% . (b) Grid voltage level changes $+10\%$.

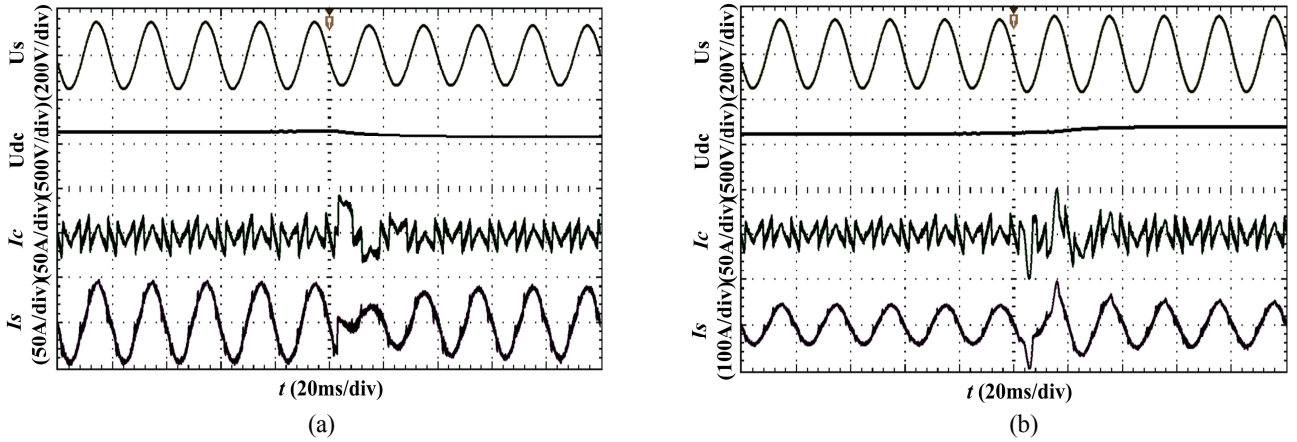


Fig. 17. Experiment waveform with adaptive voltage control when grid voltage level varies $\pm 10\%$. (a) Grid voltage level changes by -10% ; (b) Grid voltage level changes by $+10\%$.

TABLE VI
COMPENSATION PERFORMANCE WITH ADAPTIVE VOLTAGE CONTROLLER WHEN GRID VOLTAGE LEVEL CHANGES

U_{sn}	U_{dc} (Adaptive)	$I_{fundamental}$	THD (Simulation)	$I_{fundamental}$	THD (Experiment)
198 V (90% U_{sn})	580 V	39.92 A	6.61%	40.22 A	7.51%
220 V (U_{sn})	630 V	44.16 A	6.48%	44.58 A	7.33%
242 V (110% U_{sn})	680 V	48.57 A	6.37%	49.10 A	7.21%

grid voltage level increases by 10% from 220 V to 242 V, the DC-link voltage level adaptively increases to a higher value of 680 V, and the THD basically remains unchanged. Compared with that in the case without the adaptive voltage block, this increase may avoid the output compensating current distortion caused by the insufficient output capability of APF when the grid voltage level increases, thus ensuring the operation of the APF and its satisfactory compensation performance.

VII. CONCLUSIONS

This study proposed an adaptive DC-link voltage controlled in the three-phase four-wire shunt APF. The required minimum DC-link voltage for APF was deduced, and its minimum DC-link voltage design block was built to implement the adaptive DC-link voltage controller. The simulation and experimental results proved that once the DC-link voltage exceeds the minimum value, increasing its value alone will not significantly improve the compensation effect but will increase

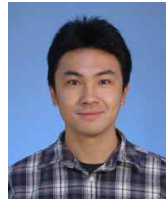
power consumption and switching loss. Thus, the DC-link voltage reference will be initially set to the required minimum value. Power consumption and switching loss can be effectively decreased on the premise that the APF operates normally.

The adaptive reference DC-link voltage control block with different harmonic currents and grid voltage levels was also built. The adaptive voltage control block can adaptively adjust the DC-link voltage reference value when the harmonic current and grid voltage level fluctuate to guarantee the operation of APF and maintain an ideal compensation performance, while reducing power consumption and switching loss compared with the traditional fixed DC-link voltage control. The viability and effectiveness of the required minimum DC-link voltage deduction and the proposed adaptive DC-link voltage control for the three-phase four-wire shunt APF were proven by both simulation and experimental results. Therefore, the proposed adaptive DC-link voltage controller is an optimal solution in practical applications.

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