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Interleaved ZVS DC/DC Converter with Balanced Input Capacitor Voltages for High-voltage Applications

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Abstract

A new DC/DC converter with zero voltage switching is proposed for applications with high input voltage and high load current. The proposed converter has two circuit modules that share load current and power rating. Interleaved pulse-width modulation (PWM) is adopted to generate switch control signals. Thus, ripple currents are reduced at the input and output sides. For high-voltage applications, each circuit module includes two half-bridge legs that are connected in series to reduce switch voltage rating to $V_{in}/2$. These legs are controlled with the use of asymmetric PWM. To reduce the current rating of rectifier diodes and share load current for high-load-current applications, two center-tapped rectifiers are adopted in each circuit module. The primary windings of two transformers are connected in series at the high voltage side to balance output inductor currents. Two series capacitors are adopted at the AC terminals of the two half-bridge legs to balance the two input capacitor voltages. The resonant behavior of the inductance and capacitance at the transition interval enable MOSFETs to be switched on under zero voltage switching. The circuit configuration, system characteristics, and design are discussed in detail. Experiments based on a laboratory prototype are conducted to verify the effectiveness of the proposed converter.

Keywords: Interleaved PWM, PWM converters, Switching mode power supplies

I. INTRODUCTION

High-voltage converters have been studied and proposed for railway electrical systems [1], ship electric power distribution systems [2], and three-level medium power converters [3]-[5]. Three-level or multilevel converters/inverters [3]-[5] with clamped diodes, capacitors, or series H-bridge circuits have been proposed to reduce the voltage rating of power devices. To achieve compact size, high power density, and high circuit efficiency in modern power products, power switches with high switching frequency and low voltage rating can be adopted in medium-power converters. Thus, three-level converters can use MOSFETs to limit the voltage stress of power switches to $V_{in}/2$. Compared with two-level converters, three-level converters have more circuit components and higher cost. However, power switches are operated in hard switching mode if converters have high switching frequency. This condition reduces circuit efficiency. Therefore, three-level converters with soft switching techniques [6]-[13] were developed to reduce the switching losses. Thus, all power switches can be switched on at zero current switching (ZCS) or zero voltage switching (ZVS) within the desired load range. The leakage inductance or external inductance of the transformer and the output capacitance of power switches are resonant at the transition interval. The drain-to-source voltage of MOSFETs can be decreased to zero voltage before MOSFETs are switched on. Therefore, if MOSFETs are switched on under ZVS, circuit efficiency is improved to achieve high switching frequency.

This study presents an interleaved soft switching DC/DC converter for high-voltage and medium-power applications. This converter is characterized by low switching loss, ZVS turn-on, and low voltage rating of MOSFETs. Two circuit modules are adopted, and the interleaved PWM scheme is used to share load current and reduce the ripple currents at input and output capacitors. Thus, the size of the input and output capacitors is reduced. In each circuit module, two

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input capacitors and two half-bridge converters are connected in series at the high voltage side to limit the voltage rating of MOSFETs to $V_{in}/2$. Therefore, power MOSFETs with 500 V voltage rating can be used in DC converters with 800 V input voltage. Two balance capacitors are connected in series between the AC sides of two half-bridge legs to balance two input split capacitor voltages automatically in each switching style. The primary windings of two transformers are connected in series to balance the secondary winding currents. Thus, power can be equally transferred to output load through two center-tapped rectifiers. Asymmetric PWM is adopted to generate the appropriate signals and regulate output voltage. MOSFETs can be switched on at ZVS within the desired load range on the basis of the resonant behavior of the MOSFET output capacitance and the transformer leakage inductance. The operation principle, circuit analysis, and design example of the proposed converter are discussed in detail. To verify the performance of the proposed converter, experiments are conducted with the use of a 1.8 kW prototype .

II. CIRCUIT CONFIGURATION

For a general single-phase AC/DC converter, the conventional half-bridge and full-bridge circuit topologies are adopted in the second stage DC/DC converter to regulate output voltage. The voltage stress of the power switches in these circuit topologies is set at DC input bus voltage V_{in}. Power MOSFETs with 600 V voltage stress are normally adopted for half-bridge and full-bridge converters and are used after single-phase power factor correction (PFC). For three-phase AC/DC converters with PFC function, 900 V voltage stress MOSFETs or 1200 V IGBTs are adopted in the second stage DC/DC converter. The two half-bridge converters shown in Fig. 1 are connected in series at the high voltage side to reduce the voltage rating of power switches to $V_{in}/2$. Meanwhile, these converters are connected in parallel at the low-voltage side to reduce the current rating of passive and active components. The main drawback of this circuit topology is that the two input split capacitor voltages can be unbalanced and thus result in unbalanced output inductor currents.

The circuit configuration of the proposed converter is shown in Fig. 2. The DC bus voltage after three-phase PFC is normally within the range of 750 V to 800 V. Two input split capacitor voltages V_{Cdc1} and V_{Cdc2} can be automatically balanced by the clamped capacitors C_{c1}–C_{c4}. The proposed DC/DC converter has two circuit modules that share the load current. The interleaved PWM with a 90-degree phase shift is adopted to generate the appropriate switching signals and regulate output voltage. Thus, the ripple currents at the input and output capacitors can be reduced. Each circuit module in the proposed converter has two half-bridge converters in series. For circuit module 1, the first half-bridge converter

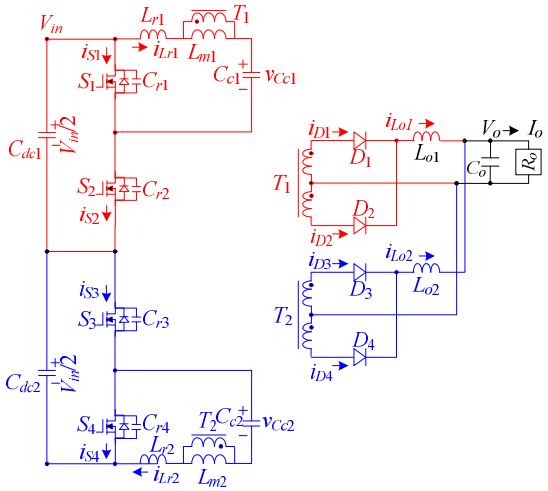

Fig. 1 Circuit configuration of two series half-bridge converter for high-input-voltage and high-current applications.

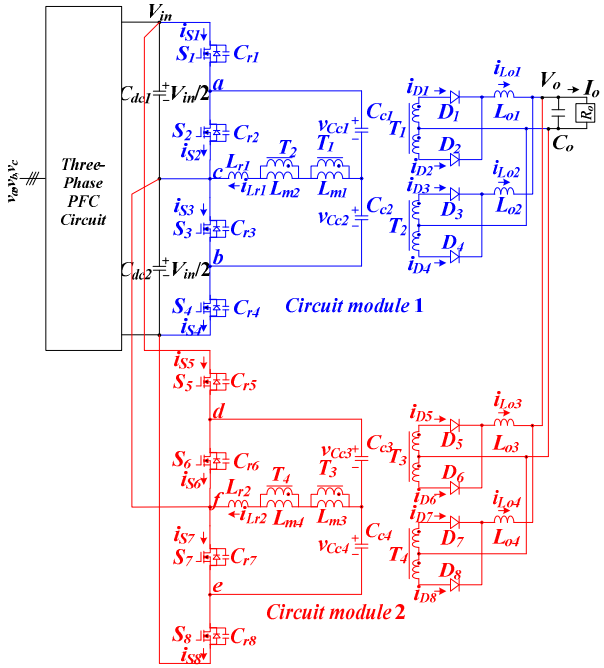

Fig. 2 Circuit configuration of the proposed interleaved ZVS converter.

includes C_{dc1}, S_1, S_2, L_{r1}, T_1, T_2, C_{r1}, C_{r2}, C_{c1}, D_1, D_2, L_{o1}, and C_o. The second half-bridge converter includes the components C_{dc2}, S_3, S_4, L_{r1}, T_1, T_2, C_{r3}, C_{r4}, C_{c2}, D_3, D_4, L_{o2}, and C_o. V_{in} and V_o are the input and output DC bus voltages, respectively. C_o is the output capacitance, and R_o is the load resistance. C_{c1}–C_{c4} are the DC blocking capacitances. C_{r1}–C_{r8} are the output capacitances of MOSFETs S_1–S_8, respectively. L_{r1} and L_{r2} are the resonant inductances, L_{m1}–L_{m4} are the magnetizing inductances and L_{o1}–L_{o4} are the output inductances of transformers T_1–T_4, respectively. D_1–D_8 are the rectifier diodes. The asymmetric PWM scheme is used to control MOSFETs S_1–S_8. S_1 and S_3 have the same PWM signals, whereas S_2 and S_4 have the same PWM waveforms.

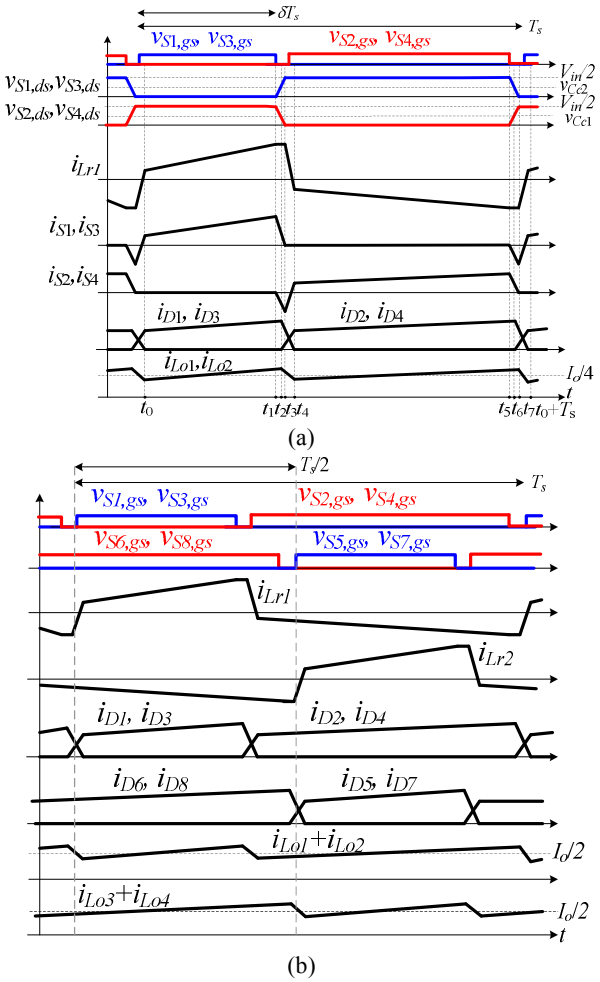

Fig. 3. Key waveforms in a switching cycle (a) circuit module 1 (b) the proposed converter.

However, S_1 and S_2 complement each other with dead time to enable the ZVS operation. The gate signals of S_5–S_8 are phase-shifted by one-fourth of the switching period with respect to the gate signals of S_1–S_4. Therefore, the inductor currents i_{Lr1} and i_{Lr2} are interleaved. C_{dc1} and C_{dc2} are input capacitors that split the input voltage (V_{Cdc1}=V_{Cdc2}=V_{in}/2). C_{c1} and C_{c2} are connected in series between AC terminals *a* and *b* to balance V_{Cdc1} and V_{Cdc2} automatically. For example, the voltage across C_{c1} and C_{c2} is equal to V_{Cdc1} if S_1 and S_3 are conducting while S_2 and S_4 are in the off-state. Meanwhile, the voltage across C_{c1} and C_{c2} is equal to V_{Cdc2} if S_1 and S_3 are in the off-state while S_2 and S_4 are conducting. Based on the on/off states of S_1–S_8, two split capacitor voltages V_{Cdc1}=V_{Cdc2}=V_{in}/2 and the voltage stress of S_1–S_8 are equal to V_{in}/2. In the proposed converter, the primary windings of transformers T_1 and T_2 are connected in series to balance i_{Lo1} and i_{Lo2} automatically. In the same manner, the output inductor currents i_{Lo3} and i_{Lo4} are also balanced. If power is delivered through two balanced circuit modules, then the current rating of each output inductor is equal to I_o/4.

III. Operation Principle

The main PWM waveforms of circuit module 1 in the proposed converter are given in Fig. 3(a). The duty cycle of S_1 and S_3 is δ, and that of S_2 and S_4 is 1-δ. The circuit modules are controlled by an interleaved PWM scheme. The gate signals of S_5–S_8 are phase-shifted by T_s/4 with respect to the gate signals of S_1–S_4, respectively. Fig. 3(b) shows the main waveforms of the proposed interleaved DC/DC converter. The following assumptions about the proposed converter are made to simplify the system analysis:

1) Transformers T_1–T_4 have the same magnetizing inductance L_m and turns ratio n;
2) Power switches S_1–S_8 and rectifier diodes D_1–D_8 are ideal;
3) Resonant capacitances C_{r1}=..=C_{r8}=C_r;
4) DC blocking capacitances C_{c1}=C_{c2}=C_{c3}=C_{c4}=C_c;
5) Input split capacitances C_{dc1}=C_{dc2};
6) Output inductances L_{o1}=L_{o2}=L_{o3}=L_{o4}=L_o; and
7) C_o is sufficiently large to be considered as constant output voltage V_o.

Circuit modules 1 and 2 exhibit the same behavior. Thus, only circuit module 1 is discussed to simplify the circuit analysis. Based on the on/off states of S_1–S_4 and D_1–D_4, eight operating modes exist in circuit module 1 during one switching cycle. Fig. 4 shows the equivalent circuits of eight operation modes in a switching cycle. S_1, S_3, and D_1–D_4 are already conducting before time t_0.

Mode 1 [t_0≤t<t_1]: At t_0, i_{D2}=i_{D4}=0. Given that L_{m1}=L_{m2}>>L_r, the magnetizing inductor voltages v_{Lm1} and v_{Lm2} are approximately v_{Cc2}/2 or (V_{in}/2-v_{Cc1})/2. The inductor currents i_{Lo1} and i_{Lo2} are increasing in this mode. Power is transferred from input voltage to output load in this time interval. At t_1, S_1 and S_3 are both off.

Mode 2 [t_1≤t<t_2]: At t_1, S_1 and S_3 are switched off. Given that i_{Lr}(t_1)>0, C_{r1} and C_{r3} are charged linearly, whereas C_{r2} and C_{r4} are discharged linearly. At t_2, v_{Cr2} and v_{Cr3} are equal to v_{Cc1} and v_{Cc2}, respectively.

Mode 3 [t_2≤t<t_3]: At t_2, v_{Cr2}=v_{Cc1} and v_{Cr3}=v_{Cc2}. The primary and secondary winding voltages of T_1 and T_2 are zero voltage, such that diodes D_1–D_4 are all conducting. In this mode, v_{Lo1}=v_{Lo2}=-V_o, i_{Lo1} and i_{Lo2} are decreased linearly, i_{D1} and i_{D3} decrease, i_{D2} and i_{D4} increase, C_{r1} and C_{r3} are continuously charged, whereas C_{r2} and C_{r4} are discharged. If the energy stored in L_{r1} is greater than that stored in C_{r1}–C_{r4}, then C_{r2} and C_{r4} can be discharged to zero voltage. At t_3, C_{r2} and C_{r4} are also discharged to zero voltage. The time interval in modes 2 and 3 are given by

$$\Delta t_{13} = t_3 - t_1 \approx \frac{2C_r V_{in}}{i_{Lr1}(t_1)} \quad (1)$$

The dead time t_d between S_1 and S_2 must be greater than the time interval Δt_{13} to achieve ZVS turn-on for S_2 and S_4.

Mode 4 [t_3≤t<t_4]: At t_3, v_{Cr2}=v_{Cr4}=0. Given that i_{Lr1}(t_3)>0, the

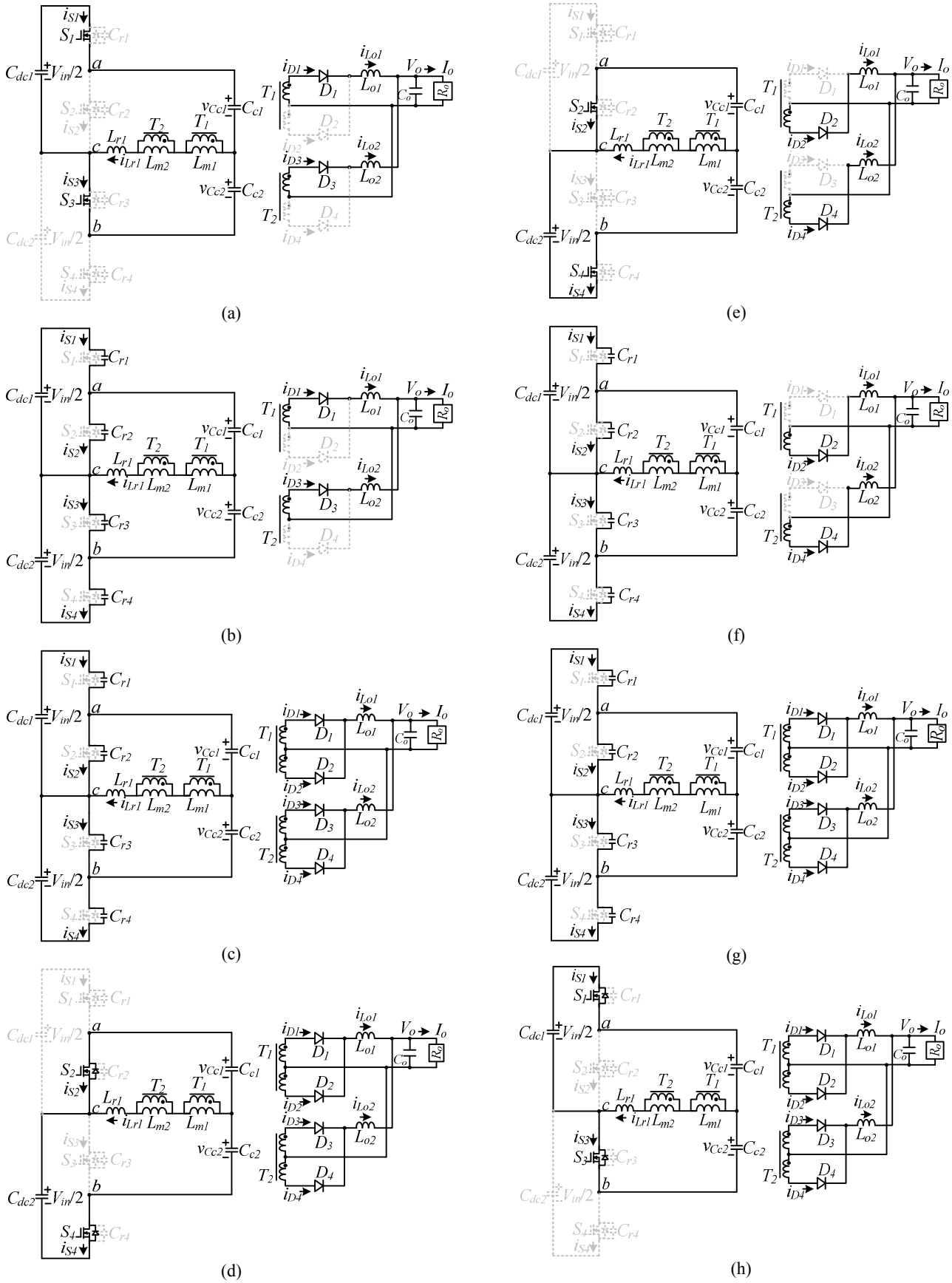

Fig. 4. Operation modes of circuit module 1 in a switching cycle. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8.

anti-parallel diodes of S_2 and S_4 are conducting. Therefore, S_2 and S_4 can be switched on at this moment to achieve ZVS. Given that D_1–D_4 are still in the commutation state, the inductor voltage v_{Lr1}=-(V_{in}/2-v_{Cc2})=-v_{Cc1}, and i_{Lr1} is decreasing. At t_4, i_{D1} and i_{D3} are decreasing to zero. The current variation of L_{r1} is $\Delta i_{Lr1} = I_o/(2n)$. The time interval in this mode is given by

$$\Delta t_{34} = t_4 - t_3 \approx \frac{L_r I_o}{2n(V_{in}/2 - v_{Cc2})} = \frac{L_r I_o}{2n v_{Cc1}} \quad (2)$$

Given that S_2, S_4, and D_1–D_4 are conducting, the duty loss in mode 4 is expressed as

$$\delta_{loss,4} = \frac{\Delta t_{34}}{T_s} \approx \frac{L_r I_o f_s}{2n v_{Cc1}} \quad (3)$$

Mode 5 [$t_4 \le t < t_5$]: At t_4, i_{D1}=i_{D3}=0. In this mode, the inductor current i_{Lr1} decreases. Given that the duty ratio of S_1 and S_3 is less than 0.5, the average voltages of C_{c1} and C_{c2} are smaller and larger than V_{in}/4, respectively. Currents i_{Lo1} and i_{Lo2} decrease with the slope of [v_{Cc1}/2n-V_o]/L_o. Power is transferred from input voltage to output load in this time interval. At time t_5, S_2 and S_4 are switched off.

Mode 6 [$t_5 \le t < t_6$]: At time t_5, power switches S_2 and S_4 are switched off. Given that $i_{Lr1}(t_5)$ is negative, C_{r2} and C_{r4} are charged, whereas C_{r1} and C_{r3} are discharged. At time t_6, v_{Cr2} and v_{Cr3} are equal to v_{Cc1} and v_{Cc2}, respectively.

Mode 7 [$t_6 \le t < t_7$]: At time t_6, v_{Cr2}=v_{Cc1} and v_{Cr3}=v_{Cc2}. The primary and secondary winding voltages of T_1 and T_2 are equal to zero voltage, such that D_1–D_4 are conducting, and v_{Lo1}=v_{Lo2}=-V_o. i_{Lo1} and i_{Lo2} decrease, i_{D1} and i_{D3} increase, whereas i_{D2} and i_{D4} decrease. C_{r1} and C_{r3} are continuously discharged, whereas C_{r2} and C_{r4} are charged linearly. If the energy stored in L_{r1} is greater than the energy stored in C_{r1}–C_{r4}, then C_{r1} and C_{r3} can be discharged to zero voltage. At time t_7, C_{r1} and C_{r3} are discharged to zero voltage. The time interval in modes 6 and 7 is given by

$$\Delta t_{57} = t_7 - t_5 \approx \frac{2C_r V_{in}}{i_{Lr1}(t_5)} \quad (4)$$

The dead time t_d between S_1 and S_2 must be greater than the time interval Δt_{57} to achieve ZVS turn-on for S_1 and S_3.

Mode 8 [$t_7 \le t < t_0 + T_s$]: At t_7, v_{Cr1}=v_{Cr3}=0. Given that $i_{Lr1}(t_7)$<0, the anti-parallel diodes of S_1 and S_3 are conducting. S_1 and S_3 can be switched on at this moment to achieve ZVS. Given that D_1–D_4 are all also conducting, the inductor voltage v_{Lr1}=(V_{in}/2-v_{Cc1})=v_{Cc2} and i_{Lr1} are increasing. At t_0+T_s, i_{D2}=i_{D4}=0. The current variation on L_{r1} is $\Delta i_{Lr} = I_o/(2n)$, and the time interval in this mode is expressed as

$$\Delta t_{70} = t_7 - t_0 \approx \frac{L_r I_o}{2n(V_{in}/2 - v_{Cc1})} = \frac{L_r I_o}{2n v_{Cc2}} \quad (5)$$

The duty loss in mode 8 is given by

$$\delta_{loss,8} = \frac{\Delta t_{70}}{T_s} \approx \frac{L_r I_o f_s}{2n v_{Cc2}} \quad (6)$$

The circuit operations of the proposed converter in a switching cycle are finally completed.

IV. Circuit Characteristics

Given that C_{r1}–C_{r8} << C_{c1}–C_{c4}, the charge and discharge times of C_{r1}–C_{r8} at turn-on and turn-off can be neglected. Only modes 1, 4, 5, and 8 are considered in circuit module 1 to derive the voltage conversion ratio of the proposed converter. From the volt-second balance on (L_{r1}, L_{m1}, and L_{m2}) and (L_{r2}, L_{m3}, and L_{m4}), the average capacitor voltages V_{Cc1}–V_{Cc4} are expressed as

$$V_{Cc1} = V_{Cc3} = \delta V_{in}/2 \text{ and } V_{Cc2} = V_{Cc4} = (1-\delta)V_{in}/2, \quad (7)$$

where δ is the duty cycle of S_1, S_3, S_5, and S_7. We apply the volt-second balance to L_{o1}–L_{o4} in steady state. The voltage conversion ratio of the proposed converter is derived from

$$\frac{V_o + V_f}{V_{in}} = \frac{-2\delta^2 + \delta(2 + \delta_{loss,8} - \delta_{loss,4}) - \delta_{loss,8}}{4n} \quad (8)$$

where V_f is the voltage drop on diodes D_1–D_8. Based on (3) and (6)–(8), the output voltage can be rewritten as

$$V_o = \frac{V_{in}}{2n}\left[\delta(1-\delta) - \frac{L_r I_o f_s}{n V_{in}}\right] - V_f \quad (9)$$

The average output inductor currents under steady state are expressed as I_{Lo1}=I_{Lo2}=I_{Lo3}=I_{Lo4}=I_o/4. The ripple currents on output inductors are given by

$$\Delta i_{Lo1} = \Delta i_{Lo2} = \Delta i_{Lo3} = \Delta i_{Lo4} \approx \frac{V_{in} T_s}{4nL_o}\left[\delta(1-\delta)(1-2\delta) + \frac{L_r I_o f_s (3\delta - 1)}{n V_{in}} - \frac{1}{1-\delta}\left(\frac{L_r I_o f_s}{n V_{in}}\right)^2\right] \quad (10)$$

Given that $i_{Cc1,av}$=$i_{Cc2,av}$=$i_{Cc3,av}$=$i_{Cc4,av}$=0, the average magnetizing currents I_{Lm1}-I_{Lm4} are approximately equal to (1-2δ)I_o/(4n). The ripple currents on inductances L_{m1}–L_{m4} can be expressed as

$$\Delta i_{Lm} = \frac{V_{Cc2}(\delta - \delta_{loss,8})T_s}{L_m} = \frac{\delta(1-\delta)V_{in}T_s - L_r I_o/n}{2L_m} \quad (11)$$

The maximum and minimum magnetizing currents of L_{m1}–L_{m4} are given by

$$i_{Lm,\max} = \frac{(1-2\delta)I_o}{4n} + \frac{\delta(1-\delta)V_{in}T_s - L_r I_o/n}{4L_m} \quad (12)$$

$$i_{Lm,\min} = \frac{(1-2\delta)I_o}{4n} - \frac{\delta(1-\delta)V_{in}T_s - L_r I_o/n}{4L_m} \quad (13)$$

The output inductances of L_{o1}-L_{o4} can be obtained as

$$L_o = \frac{[V_{Cc2}/n - V_o - V_f](\delta - \delta_{loss,8})T_s}{\Delta i_{Lo}} = \frac{\left[\frac{(1-\delta)^2 V_{in}}{2n} + \frac{L_r I_o f_s}{2n^2}\right]\left(\delta - \frac{L_r I_o f_s}{n V_{in}(1-\delta)}\right)T_s}{\Delta i_{Lo}} \quad (14)$$

The maximum and minimum output inductor currents are expressed as

$$i_{Lo,\max} = \frac{I_o}{4} + \left[\frac{(1-\delta)^2 V_{in}}{4n} + \frac{L_r I_o f_s}{4n^2}\right]\left(\delta - \frac{L_r I_o f_s}{n V_{in}(1-\delta)}\right)\frac{T_s}{L_o} \quad (15)$$

$$i_{Lo,\min}=\frac{I_o}{4}-[\frac{(1-\delta)^2V_{in}}{4n}+\frac{L_rI_of_s}{4n^2}](\delta-\frac{L_rI_of_s}{nV_{in}(1-\delta)})\frac{T_s}{L_o} \quad (16)$$

The average currents on rectifier diodes D_1–D_8 are expressed as $I_{D1}=I_{D3}=I_{D5}=I_{D7}=\delta I_o/4$ and $I_{D2}=I_{D4}=I_{D6}=I_{D8}=(1-\delta)I_o/4$. The voltage stress of D_1, D_3, D_5, and D_7 is $\delta V_{in}/n$ In the same manner, the voltage stress of rectifier diodes D_2, D_4, D_6, and D_8 is $(1-\delta)V_{in}/n$. The root-mean-square (*rms*) values of switching currents $i_{S1,rms}$–$i_{S4,rms}$ are approximately given by

$$i_{S1,rms}=i_{S3,rms}\approx\sqrt{(\frac{I_o}{8n})^2\frac{L_rI_of_s}{3nV_{in}(1-\delta)}+(\frac{(1-\delta)I_o}{4n})^2(\delta-\frac{L_rI_of_s}{nV_{in}(1-\delta)})} \quad (17)$$

$$i_{S2,rms}=i_{S4,rms}\approx\sqrt{(\frac{I_o}{8n})^2\frac{L_rI_of_s}{3n\delta V_{in}}+(\frac{\delta I_o}{4n})^2(1-\delta-\frac{L_rI_of_s}{n\delta V_{in}})} \quad (18)$$

The voltage stresses of S_1–S_4 are equal to $V_{in}/2$. At time t_1, the inductor current i_{Lr1} is approximated as

$$\begin{aligned}i_{Lr1}(t_1)&\approx i_{Lm1,\max}+\frac{i_{Lo1,\max}}{n}\\&\approx\frac{(1-2\delta)I_o}{4n}+\frac{\delta(1-\delta)V_{in}T_s-L_rI_o/n}{4L_m}+\frac{I_o}{4n}\\&+[\frac{(1-\delta)^2V_{in}}{4n^2}+\frac{L_rI_of_s}{4n^3}](\delta-\frac{L_rI_of_s}{nV_{in}(1-\delta)})\frac{T_s}{L_o}\end{aligned} \quad (19)$$

In the same manner, the inductor current i_{Lr1} at t_5 is approximated as

$$\begin{aligned}i_{Lr1}(t_5)&\approx\frac{(1-2\delta)I_o}{4n}-\frac{\delta(1-\delta)V_{in}T_s-L_rI_o/n}{4L_m}-\frac{I_o}{4n}\\&-[\frac{(1-\delta)(1-2\delta)V_{in}}{4n^2}+\frac{L_rI_of_s}{4n^3}](\delta-\frac{L_rI_of_s}{nV_{in}(1-\delta)})\frac{T_s}{L_o}\end{aligned} \quad (20)$$

If the energy stored in inductor L_{r1} at t_1 is greater than that in capacitors C_{r1}–C_{r4}, then C_{r2} and C_{r4} can be discharged to zero voltage. The ZVS condition of S_2 and S_4 is expressed as

$$L_{r1}\ge\frac{2C_r(V_{in}/2)^2}{i_{Lr1}^2(t_1)}=\frac{C_rV_{in}^2}{2i_{Lr1}^2(t_1)}. \quad (21)$$

If the energy stored in L_{r1} at t_5 is greater than that in capacitors C_{r1}–C_{r4}, then capacitors C_{r1} and C_{r3} can be discharged to zero voltage. The ZVS condition of S_1 and S_3 is given by

$$L_{r1}\ge\frac{C_rV_{in}^2}{2i_{Lr1}^2(t_5)} \quad (22)$$

In the same manner, the ZVS condition of S_5 and S_7 is given by

$$L_{r2}\ge\frac{C_rV_{in}^2}{2i_{Lr2}^2(t_5+T_s/2)}=\frac{C_rV_{in}^2}{2i_{Lr1}^2(t_5)} \quad (23)$$

The ZVS condition of S_6 and S_8 is shown in (24).

$$L_{r2}\ge\frac{C_rV_{in}^2}{2i_{Lr2}^2(t_1+T_s/2)}=\frac{C_rV_{in}^2}{2i_{Lr1}^2(t_1)} \quad (24)$$

From (21)–(24), the necessary inductances L_{r1} and L_{r1} to achieve ZVS turn-on of S_1–S_8 are derived as

$$L_{r1}=L_{r2}=L_r\ge\max\{\frac{C_rV_{in}^2}{2i_{Lr1}^2(t_1)},\ \frac{C_rV_{in}^2}{2i_{Lr1}^2(t_5)}\}. \quad (25)$$

V. Design Example and Experimental Results

The proposed converter design is presented in this section. A laboratory prototype with 1.8 *k*W rated power was built to test the proposed converter. The electrical specifications of the converter are V_{in}=750 V to 800 V, V_o=24 V, I_o=75 A, and f_s=100 kHz. The maximum duty cycle of S_1 is assumed as 0.45 at V_{in}=750 V and full load. The maximum duty cycle loss in modes 4 and 8 is assumed to be 15% under a full load with a duty cycle δ=0.5.

$$\delta_{loss,T}=\delta_{loss,4}+\delta_{loss,8}\approx\frac{4L_rI_{o,full}f_s}{nV_{in,\min}}\approx\frac{32P_{o,full}L_rf_s}{V_{in,\min}^2}<0.15 \quad (26)$$

Step 1: Resonant inductance

From (26), the resonant inductance of L_r can be derived as

$$L_{r1}=L_{r2}=L_r<\frac{V_{in,\min}^2\delta_{loss,T}}{32P_{o,full}f_s}\approx14.6\mu H \quad (27)$$

In the prototype circuit, the selected inductances are $L_{r1}=L_{r2}=14\mu H$.

Step 2: Turns ratio of T_1–T_4

If the voltage drop V_f on diodes D_1–D_8 is neglected, the turns ratio of T_1–T_4 is given by

$$\begin{aligned}n&=\frac{\delta_{\max}(1-\delta_{\max})V_{in,\min}+\sqrt{[\delta_{\max}(1-\delta_{\max})V_{in,\min}]^2-8V_oI_oL_rf_s}}{4V_o}\\&\approx3.18\end{aligned} \quad (28)$$

The TDK EER-40C magnetic cores with primary and secondary winding turns of n_p=45 turns and n_s=15 turns, respectively, are adopted for transformers T_1–T_4. The magnetizing inductance of T_1–T_4 is 350 μH.

Step 3: Power switches S_1-S_8

From (17) and (18), the *rms* currents and voltage stresses of S_1–S_8 are given by

$$\begin{aligned}&i_{S1,rms}=i_{S3,rms}=i_{S5,rms}=i_{S7,rms}\\&\approx\sqrt{(\frac{I_o}{8n})^2\frac{L_rI_of_s}{3nV_{in,\min}(1-\delta_{\max})}+(\frac{(1-\delta_{\max})I_o}{4n})^2(\delta-\frac{L_rI_of_s}{nV_{in,\min}(1-\delta_{\max})})}\\&\approx2.29A\end{aligned} \quad (29)$$

$$\begin{aligned}&i_{S2,rms}=i_{S4,rms}=i_{S6,rms}=i_{S8,rms}\\&\approx\sqrt{(\frac{I_o}{8n})^2\frac{L_rI_of_s}{3n\delta_{\max}V_{in,\min}}+(\frac{\delta_{\max}I_o}{4n})^2(1-\delta_{\max}-\frac{L_rI_of_s}{n\delta_{\max}V_{in,\min}})}\\&\approx2A\end{aligned} \quad (30)$$

$$V_{S1,stress}=.....=V_{S8,stress}=V_{in,\max}/2=400V \quad (31)$$

IRFP460 MOSFETs with V_{DS}=500 V, $I_{D,rms}$=20 A, $R_{DS,on}$=0.27 Ω, and C_{oss}=480 pF at 25 V are used for S_1–S_8.

Step 4: Power diodes D_1-D_8 and capacitances

The average currents and voltage stresses of D_1–D_8 are

expressed as

$$I_{D1} = I_{D3} = I_{D5} = I_{D7} \approx \delta_{\max} I_o / 4 \approx 8.4A \quad (32)$$

$$I_{D2} = I_{D4} = I_{D6} = I_{D8} \approx (1-\delta_{\min}) I_o / 4 \approx 10.8A \quad (33)$$

$$V_{D1,stress} = V_{D3,stress} = V_{D5,stress} = V_{D7,stress} \approx \frac{\delta_{\max} V_{in,\min}}{n} \approx 113V \quad (34)$$

$$V_{D2,stress} = V_{D4,stress} = V_{D6,stress} = V_{D8,stress} \approx \frac{(1-\delta_{\min}) V_{in,\max}}{n} \approx 154V \quad (35)$$

The KCU30A30 fast recovery diodes with V_{RRM}=300 V and I_F=30 A are used as the rectifier diodes D_1–D_8. The selected DC blocking capacitances and the output capacitance are C_{c1}=C_{c2}=C_{c3}=C_{c4}=0.2 μF, C_{dc1}=C_{dc2}=470 μF, and C_o=4400 μF.

Step 5: Output filter inductances L_{o1}–L_{o4}

The ripple current on L_{o1}-L_{o4} is set to 10% of the rated inductor current. From (10), L_{o1}–L_{o4} can be obtained from

$$L_o = \frac{V_{in,\max} T_s [\delta_{\min}(1-\delta_{\min})(1-2\delta_{\min}) + \frac{L_r I_o f_s (3\delta_{\min}-1)}{n V_{in,\max}} - \frac{(L_r I_o f_s)^2}{(1-\delta_{\min}) n^2 V_{in,\max}^2}]}{0.1 \times I_{Lo1} \times 4n} \approx 16\mu H \quad (36)$$

where L_{o1}–L_{o4} are set as 16 μH in the prototype circuit.

Step 6: ZVS conditions of S_1 and S_2

The output capacitance of IRFP460 MOSFETs is 480 pF at 25 V. The equivalent output capacitance C_r at V_{in}=800 V is given by

$$C_r \approx \frac{4}{3} C_{oss,25} \sqrt{\frac{25}{v_{S1,ds}}} = \frac{4}{3} \times 480 \times \sqrt{\frac{25}{400}} \approx 160\,pF \quad (37)$$

From (21) and (22), the minimum inductor current $i_{Lr1}(t_1)$ and $i_{Lr1}(t_5)$ to achieve ZVS turn-on for S_1–S_4 is obtained from

$$|i_{Lr1,\min}(t_1)| = |i_{Lr1,\min}(t_5)| \geq \sqrt{\frac{C_r V_{in,\max}^2}{2L_r}} = \sqrt{\frac{160 \times 10^{-12} \times 800^2}{2 \times 14 \times 10^{-6}}} \approx 1.9A \quad (38)$$

If the ripple currents on the primary and secondary sides in (19) and (20) can be neglected, the minimum load current to achieve ZVS turn-on for (S_1 and S_3) and (S_2 and S_4) are approximated in (39) and (40), respectively.

$$I_{o,\min,S_1,S_3,S_5,S_7} \approx \frac{2n|i_{Lr1,\min}(t_5)|}{\delta_{\max}} \approx 25A \quad (39)$$

$$I_{o,\min,S_2,S_4,S_6,S_8} \approx \frac{2n|i_{Lr1,\min}(t_1)|}{(1-\delta_{\min})} \approx 19.7A \quad (40)$$

From (39) and (40), S_1, S_3, S_5, and S_7 can be switched on under ZVS from 25 A load (approximately 33% load) to 75 A load (100% load). Meanwhile, S_2, S_4, S_6, and S_8 can be turned on under ZVS from 19.7 A load (approximately 26% load) to 75 A load (100% load).

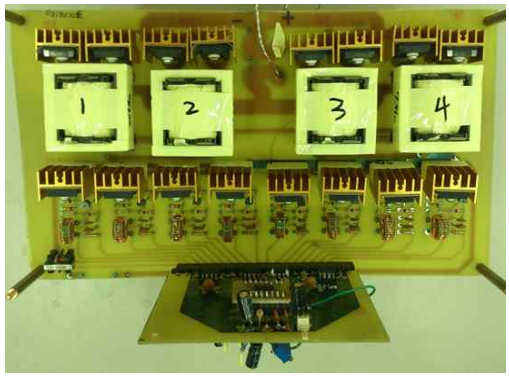

Fig. 5. Photograph of the experimental setup.

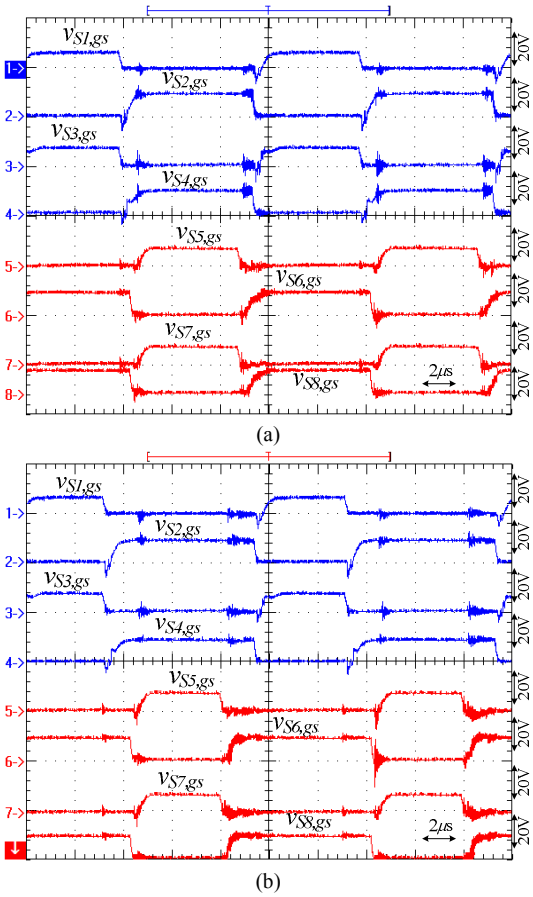

Fig. 6. Measured PWM waveforms of gate voltages at full load and (a) V_{in}=750V (b) V_{in}=800V.

Experiments based on a laboratory prototype, with the circuit parameters derived in the previous section, are presented in this section to verify the effectiveness of the proposed converter. A photograph of the experimental setup is shown in Fig. 5. Fig. 6 shows the measured PWM waveforms of S_1–S_8 at full load under different input voltages. The PWM signals of S_5–S_8 were phase-shifted by half of the switching cycle with respect to PWM signals of S_1–S_4, respectively. Fig. 7 gives the measured gate voltage, drain voltage, and drain current of switches S_1 and S_2 at V_{in}=800 V and 26%, 50%, and 100% load conditions. S_1 is switched on at hard switching under 26% load and at zero

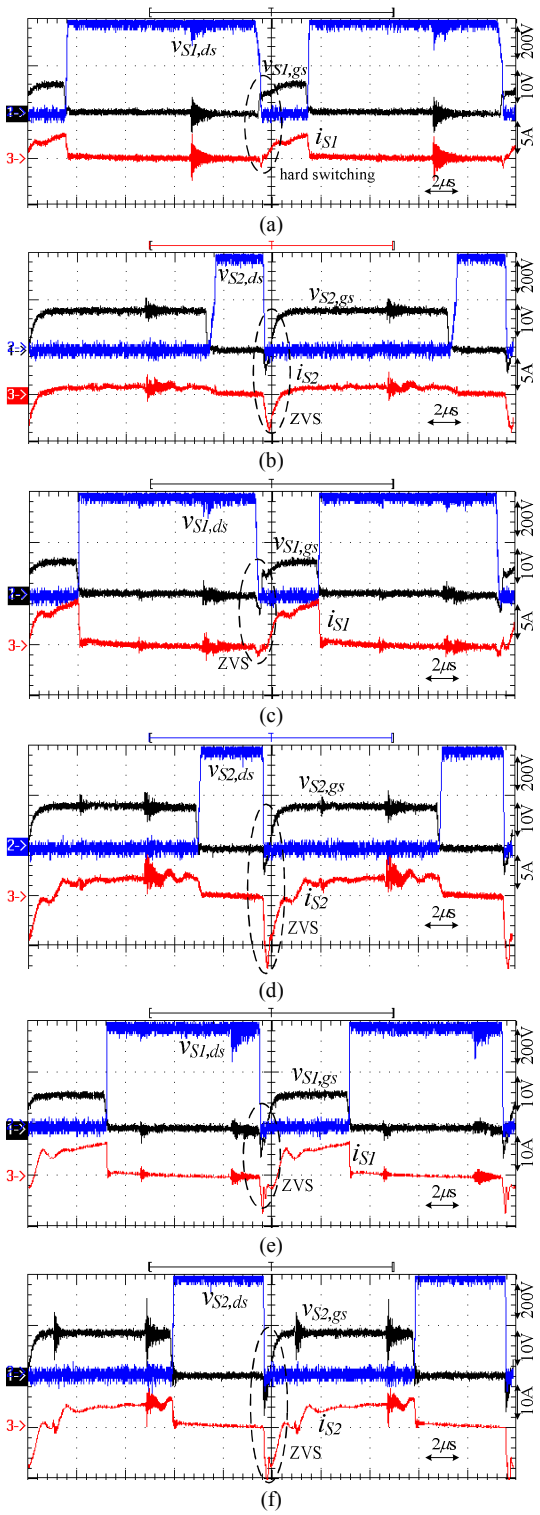

Fig. 7. Measured PWM waveforms of gate voltage, drain voltage, and drain current: (a) S_1 under 26% load, (b) S_2 under 26% load, (c) S_1 under 50% load, (d) S_2 under 50% load, (e) S_1 under 100% load, and (f) S_2 under 100% load.

voltage switching under 50% and 100% load condition. However, S_2 is switched on under ZVS from 26% load to full load. From the test results in Fig. 7, we can expect that S_4, S_6, and S_8 are also switched on under ZVS from 26% load to full load. Fig. 8 gives the measured voltage waveforms v_{Cdc1}, v_{Cdc2}, and $v_{Cc1}+v_{Cc2}$ at full load. Three capacitor voltages v_{Cdc1}, v_{Cdc2} and $v_{Cc1}+v_{Cc2}$ are balanced. Fig. 9 shows the measured waveforms of $v_{S1,gs}$, $v_{S5,gs}$, i_{Lr1}, and i_{Lr2} at full load. When S_1 is conducting, i_{Lr1} increases. Meanwhile, i_{Lr1} decreases if S_1 switched off. i_{Lr1} and i_{Lr2} are phase-shifted by half of a switching cycle. Fig. 10 gives the measured waveforms of i_{D1}, i_{D2}, i_{D5}, i_{D6}, and i_{Lo1}–i_{Lo4} at full load. Fig. 11 shows the output currents $i_{Lo1}+i_{Lo2}$ and $i_{Lo3}+i_{Lo4}$ of the two circuit modules at full load. The output currents of the two circuit modules balance each other. Fig. 12 shows the measured circuit efficiencies at different load conditions. Based on the load current and the voltage drop on rectifier diodes, the conduction losses on rectifier diodes, MOSFETs, and power semiconductors can be estimated to be approximately 5% to 6%, 1% to 2%, and 6% to 8% of the rated power, respectively. Other power losses are related to the core and copper losses on inductors and transformers, the necessary passive snubber across the rectifier diodes, and some switching losses, such as turn-off losses on MOSFETs and switching losses on rectifier diodes. The rectifier diodes can

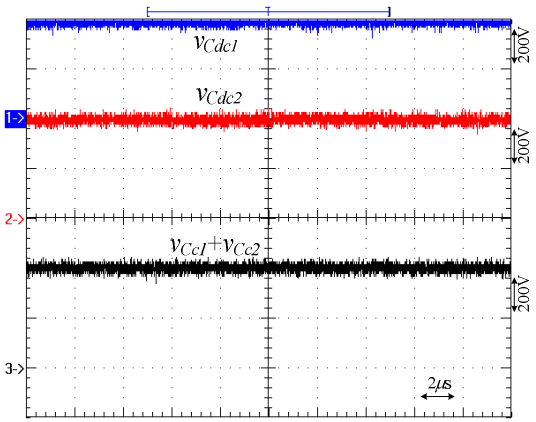

Fig. 8. Measured voltage waveforms v_{Cdc1}, v_{Cdc2} and $v_{Cc1}+v_{Cc2}$ at full load and 800 V input voltage.

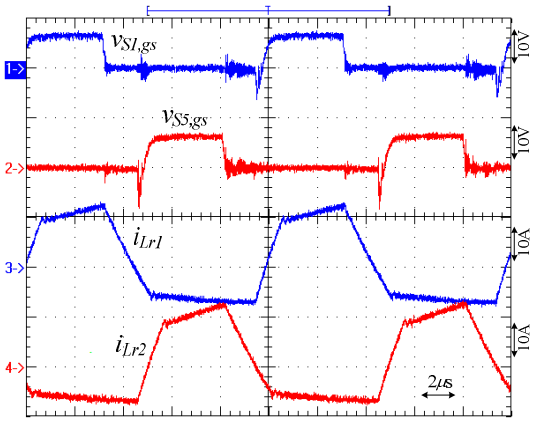

Fig. 9. Measured waveforms of $v_{S1,gs}$, $v_{S5,gs}$, i_{Lr1} and i_{Lr2} at full load.

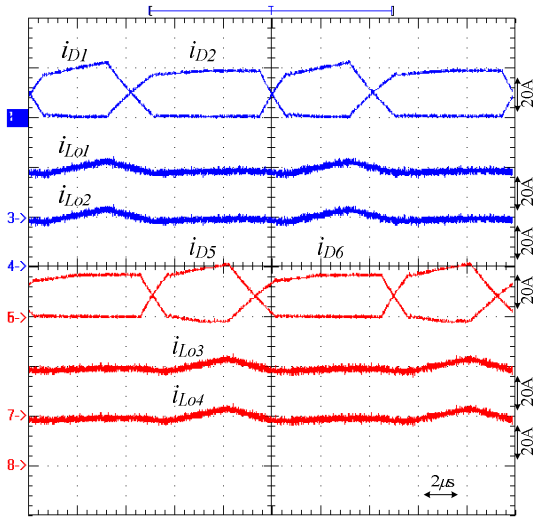

Fig. 10. Measured waveforms of i_{D1}, i_{D2}, i_{D5}, i_{D6} and i_{Lo1}-i_{Lo4} at 100% load.

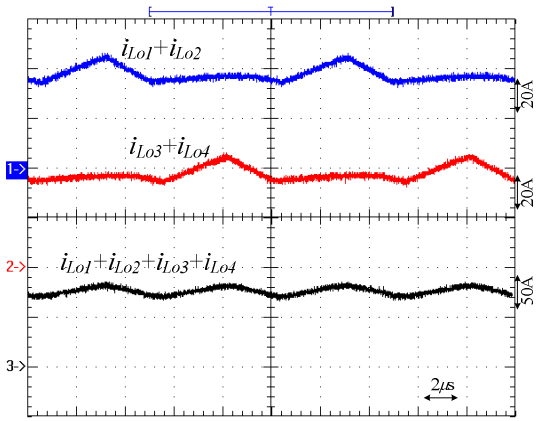

Fig. 11. Measured waveforms of $i_{Lo1}+i_{Lo2}$, $i_{Lo3}+i_{Lo4}$ and $i_{Lo1}+i_{Lo2}+i_{Lo3}+i_{Lo4}$ at 100% load.

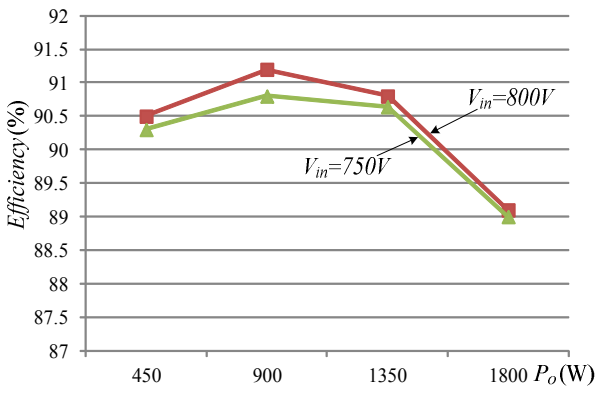

Fig. 12. Measured circuit efficiencies at different load conditions.

be replaced by synchronous rectifiers to increase circuit efficiency by approximately 2% to 4%. Low loss MOSFETs and cores can also be adopted to increase circuit efficiency.

VI. Conclusions

A new parallel DC/DC converter for applications with high input voltage and high load current is presented. The proposed converter is characterized by 1) ZVS turn-on for all switches from 33% load to 100% load, 2) V_{in}/2 voltage stress of power switches, and 3) low ripple currents at input and output sides when using the interleaved PWM scheme. Two half-bridge converters are connected in series to reduce the voltage stress of power switches at V_{in}/2. Thus, MOSFETs with 500 V voltage stress are used for 800 V input voltage applications. Two series capacitors connected at the AC terminals of two half-bridge converters are used to balance two input capacitor voltages automatically. A PWM scheme is used to generate PWM signals and regulate output voltage, such that power switches can be switched on under ZVS within the desired load range. System analysis, operation mode, circuit characteristics, and design of the proposed converter are discussed in detail. Finally, experiments with the 1.8 kW prototype are conducted to verify the effectiveness of the proposed converter.

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