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A Design of BJT-based ESD Protection Device combining SCR for High Voltage Power Clamps

Jin-Woo Jung and Yong-Seo Koo

***Abstract*—This paper presents a novel bipolar junction transistor (BJT) based electrostatic discharge (ESD) protection device. This protection device was designed for 20V power clamps and fabricated by a process with Bipolar-CMOS-DMOS (BCD) 0.18µm. The current-voltage characteristics of this protection device was verified by the transmission line pulse (TLP) system and the DC BV characteristic was verified by using a semiconductor parameter analyzer. From the experimental results, the proposed device has a trigger voltage of 29.1V, holding voltage of 22.4V and low on-resistance of approximately 1.6Ω. In addition, the test of ESD robustness showed that the ESD successfully passed through human body model (HBM) 8kV. In this paper, the operational mechanism of this protection device was investigated by structural analysis of the proposed device. In addition, the proposed device were obtained as stack structures and verified.**

***Index Terms*—Electrostatic discharge, bipolar junction transistor, silicon controlled rectifier**

I. INTRODUCTION

In recent years, with increasing demands for high voltage in modern electronic circuits such as automobile, power management, power distribution, and driver ICs, high voltage ICs have become widely used in today's IC products [1]. At the same time, electrostatic discharge (ESD) protection in these high voltage technologies has become much more difficult than in standard CMOS logic technologies [2].

High voltage MOSFETs are widely used in switching devices, output drivers, and in general ESD protection in high voltage ICs. However, MOSFETs or MOSFET based devices used as ESD protection devices are inherently weak with respect to ESD robustness and reliability. In particular, the well-known 'base push-out' effect [3] lead to current filamentation, which causes the ESD stress current to be sustained only by a portion of the device, where thermal failure occurs as a result [4, 5]. In addition, a MOSFET based ESD protection device consumes a relatively large silicon area and their relatively low holing voltage may cause a latch-up issue due static or may cause transients.

Either an NPN bipolar junction transistor (BJT) or a silicon controlled rectifier (SCR) ESD structures are generally used as high voltage clamp due to its high current driving capability. However, because of the nature of avalanche-injection conductivity modulation, both structures provide low holding voltages when implemented in high voltage processes [6].

In this paper, we introduce BJT based ESD protection device with robustness and low on-resistance characteristic for high voltage applications. We achieve the high robustness and low on-resistance by combining the BJT with SCR.

This paper is composed of four sections. Section II of this paper describes the cross-section of the proposed device and its operation under ESD surge environment. Section III presents the TLP measurement, breakdown voltage and robustness of the proposed device. Finally, section IV presents a summary and the conclusion.

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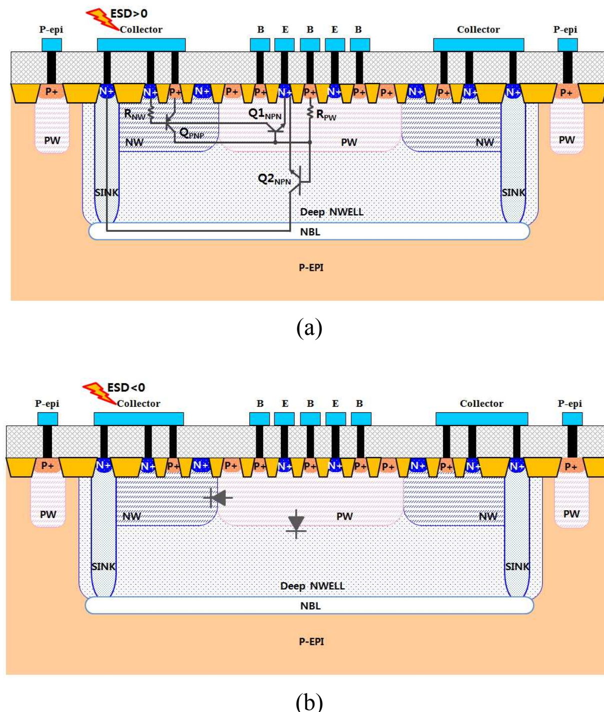
Department of Electronics and Electrical Engineering
Dankook University, Gyeonggi-do, Korea.
E-mail : yskoo@dankook.ac.kr

II. DEVICE DESCRIPTION

1. Device Structure

Figs. 1(a) and (b) show the cross-section of the proposed structure and the positive ESD and negative ESD paths. A simplified version of this device can be represented as an NPN BJT device including a silicon controlled rectifier (SCR). An N-well is added to basic BJT structure including the N-Sink and the N-buried layer (NBL) and a P-well, which forms the SCR structure. N+ region in the N-sink and the N+ and P+ regions in N-well are connected by the Collector, while the P+ and N+ regions in the P-well form the base and emitter, respectively. A poly resistor of approximately 5kΩ is connected between the base and the emitter, although it is not shown in the Figure. This device is able to adjust the breakdown voltage by changing the distance between the N-well and the P-well and the distance between the region of the well and the floating N+/P+ region. Therefore, the design parameters of this device are D1 (the distance between the N-well and the P-well) and D2 (the distance between the floating P+/N+ region and the well region).

In addition, the added floating N+/P+ diffusion regions for the structure of the internal SCR becomes the design parameter for adjusting the holding voltage. More detailed information will be explained later.



(a)

(b)

Fig. 1. Cross-section of the proposed device with BJT for (a) positive, (b) negative ESD surge.

2. Device Operation

ESD protection under positive ESD and negative ESD is shown in Fig. 1. The operation of this device is generally divided into SCR operation and BJT operation. In normal condition, because the breakdown voltage of this device is 24.5V, which is higher than the voltage of VDD, it does not work as an ESD protection device; therefore, the protection device does not interfere with the normal functions of the internal circuits.

If positive ESD inflows into a terminal of the collector, the electric potential of N-well and N-sink increase. If the elevated electric potential reaches the threshold, avalanche breakdown occurs. In this case, because the breakdown voltage of the N-well and the P-well is lower than those of the deep N-well and the P-well, avalanche breakdown occurs between the N-well and the P-well. This breakdown voltage determines that the breakdown voltage of proposed device. When an avalanche breakdown occurs between the N-well and the P-well, the created electrons flow into the floating N+ in the N-well, while the created holes flow into the base via the floating P+ in the P-well. Electrons and current pass through the N-well and turn on the parasitic NPN bipolar device. Thus, SCR becomes fully operational and the collector's voltage continues to increase, causing a breakdown between the deep N-well and the P-well; then the NPN bipolar device is turned ON. Finally, 2 parasitic bipolar transistors and 1 NPN bipolar in SCR operate in this device. Therefore, the proposed device has high current driving capability and low resistance, different from conventional bipolar devices.

However, if negative ESD current inflows into the terminal of the collector, a reversed bias is created between the N-well and the P-well. Therefore, the path of the parasitic diode current is created between P+ in the P-well and N+ in the N-well, by which the ESD current is discharged.

3. Analysis of the Incorporated SCR

Fig. 2 shows the cross section of SCR which is

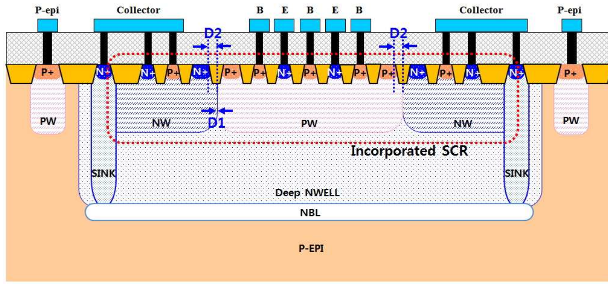


Fig. 2. Cross-section of incorporated SCR of the proposed device and design parameters.

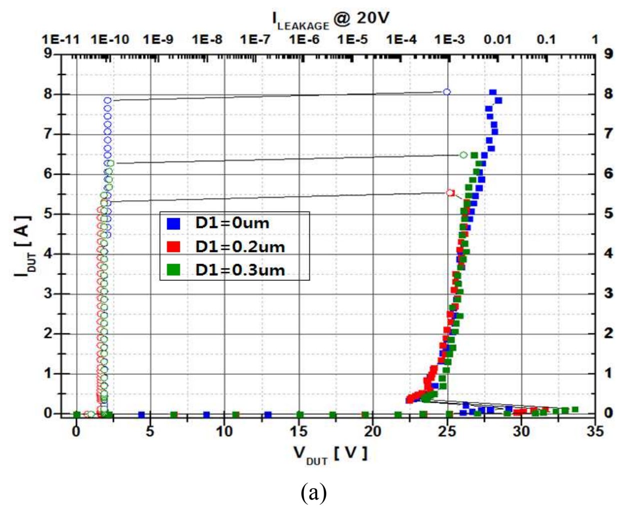
inserted into the proposed device. A general SCR forms the anode in the N+/P+ diffused region inside the N-well and the cathode in the N+/P+ diffused region inside the P-well. Unlike a general SCR, this SCR structure has N+ floating and P+ floating regions in the N-well and the P-well, respectively. These floating regions determine the breakdown voltage of the proposed device according to the distance from well and play a role in increasing the holding voltage of the internal SCR according to the length of the floating region. A highly doped floating region is located at the base of the parasitic bipolar, playing a role in reducing the current gains of the base transport factor, parasitic NPN bipolar and PNP bipolar. After avalanche breakdown occurs between the N-well and the P-well, holes flow into the P+ floating region, whose resistance is relatively lower than that of the P-well, and electrons also flow into the N+ region. Therefore, recombination is activated in the base region and the current gain of the parasitic bipolar is reduced. As a result, the holding voltage of SCR is increased.

III. EXPERIMENTAL RESULTS

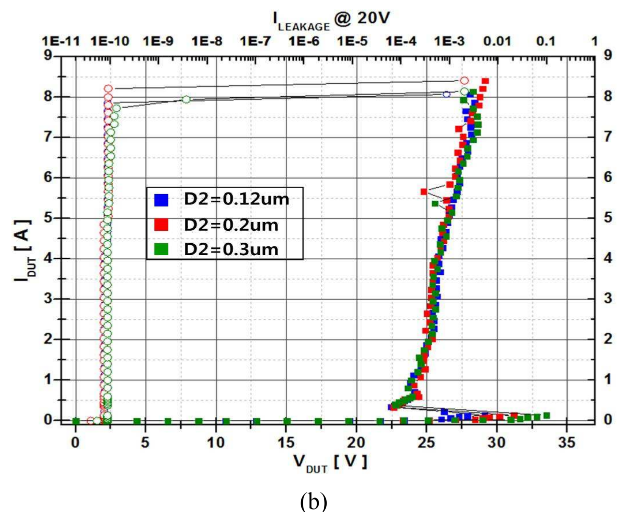
An experiment was conducted using the TLP system to verify the ESD protection performance of the proposed device. TLP measurement is widely used to analyze the electrical characteristics and fault-tolerance of ESD protection devices [7, 9]. The TLP result is typically presented as a current–voltage plot that indicates a parameter, such as the turn-on point (Vt1, It1) of the snapback protection structure. Other parameters, such as the on-resistance, can also be easily found on the TLP I-V curve [10]. This study used the TLP system of 10ns rise time and 100ns pulse width of Barth. Also, we carried out an experiment using an HBM/MM simulator (ESS-6008) and parameter analyzer (HP4156A) to measure the ESD protection robustness, DC breakdown voltage and leakage current of the proposed device. The width of the proposed device was 80 μm.

1. TLP Measurement

Fig. 3 shows TLP measurements for the design variables (D1 and D2) of the proposed device. Fig. 3(a) shows the I-V characteristics in which the design variable D1 has values of 0μm, 0.2μm and 0.3μm, respectively. As the design variable D1 increases from 0μm, to 0.2μm and to 0.3 μm, the trigger voltage increases up to 29.1V, 31.5V and 33.5V respectively. The design variable D1 represents the distance between the N-well and the P-



(a)



(b)

Fig. 3. I-V characteristics for the design variables of the proposed device (a) D1; (b) D2 parameters.

Table 1. Electrical characteristics of the proposed device with design variables

Design parameter		Trigger Voltage	Holding Voltage	Second Breakdown current
D1	0 μm	29.1V	22.4V	7.85A
	0.2 μm	31.5V	22.4V	5.32A
	0.3 μm	33.5V	23.4V	6.2A
D2	0.12 μm	29.1V	22.4V	7.85A
	0.2 μm	31.3V	22.6V	8.2A
	0.3 μm	33.8V	22.4V	7.7A

well. As this distance increases, the bigger the area of the deep N-well, which is under lower concentration than the N-well. Therefore, the width of the space charge region increases in the direction of the N-well and then the maximum electric field where avalanche breakdown occurs is reduced, which in turn causes the breakdown voltage to rise. A relation between the depletion layer and the maximum electric field is expressed by the following equation [11].

$$E_{\max} = \frac{-2(V_{bi} + V_R)}{W} \quad (1)$$

where V_{bi} indicates the potential barrier, V_R is the applied reverse bias, and W is the width of the space charge region. Assuming that the applied reverse bias is constant, the more the width of the space charge region increases, the less the E_{max} becomes.

2. DC Characteristics

We performed DC measurements to check the leakage current and the breakdown voltage of the proposed device. Fig. 4 shows the breakdown voltage and leakage current according to the value of the design variable D1.

As the design variable D1 increases from 0μm to 0.2μm and to 0.3μm, respectively, the breakdown voltage of the proposed device increases to 24.5V, 28V and 29V, respectively, which shows the same trend as rising trigger voltage. In addition, current less than 1-E8A flows before the breakdown occurs, which proves that there is no leakage current before the element is operated.

3. HBM/MM Test

Although the I-V characteristics acquired by TLP

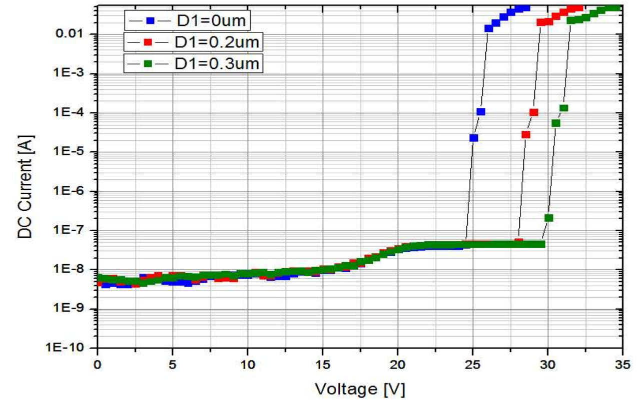


Fig. 4. DC characteristics depending on the value of the design variable D1 of the proposed device.

Table 2. ESD robustness depending on design variable for the proposed device

Design variables		Fault tolerance	
		HBM [kV]	MM [V]
D1	0 μm	8kV	800V
	0.2 μm	8kV	800V
	0.3 μm	8kV	800V
D2	0.12 μm	8kV	800V
	0.2 μm	8kV	800V
	0.3 μm	8kV	800V

measured is converted to HBM and MM value there might be differences between the results of the TLP measurements and those of HBM and MM. Therefore, we measured HBM and MM to check the fault-tolerance characteristic of the proposed device. Devices with basic design variables have fault-tolerance characteristics of HBM 8kV and MM 800V, which means these variables have higher fault tolerance characteristics exceeding HBM 2kV and MM 200V. Table 2 shows the result of the fault-tolerances of the proposed device for each design variable.

4. Stack Configuration

Stack configuration enhances the use of the proposed device. Fig. 5 shows the characteristics of the TLP I-V curve which indicates the s-stacked structure of the proposed device. This structure minimizes the isolation and interference between devices through the N-sink and the N+ buried layer, which are basic elements provided by the BCD process.

Therefore, an additional mask is not used. From the

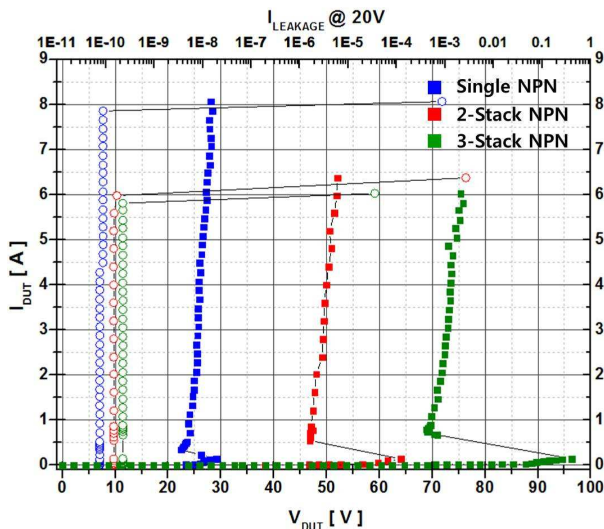


Fig. 5. I-V characteristic for stack configuration from the proposed device.

measurements, the 2-Stack NPN and the 3-Stack NPN show approximately 65V and 97V of the trigger voltage and approximately 46V and 68V of the holding voltage, respectively. It's possible to adjust the holding voltage by regulating the number of stacks and to design a high voltage ESD protection device with latch-up immunity. In addition, even a 3-stacked configuration for the proposed device shows high second breakdown current of approximately 6A. Therefore, the proposed device can be applied for high voltages of greater than 40V.

IV. Conclusions

This paper proposed a novel structure for a BJT – based, high voltage power clamp ESD protection device with high ESD robustness and low on-resistance. The proposed device was fabricated by the 0.18μm BCD process, and it showed enhanced current driving capability and approximately 1.6Ω of low resistance with the insertion of SCR into existing BJT structure. The proposed device was verified by TLP, HBM and MM measurements, and the results of the measurements showed 29.1V of trigger voltage and 23V of holding voltage. For the design variable D1 of 0μm, 0.2μm and 0.3μm, the trigger voltage increased to 29.1V, 31.5V and 33.5V, respectively, and the breakdown voltage increased to 24.5V, 28V and 29V, respectively. As the distance of D2 was gradually increased to 0.12μm, 0.2μm and 0.3μm, the trigger voltage increased to 29.1V, 31.3V and 33.8V, respectively. In addition, the proposed device showed high fault tolerances of HBM 8kV and MM 800V. Therefore, the device could be used for ESD protection at high voltages of greater than 40V.

The proposed ESD protection device is believed to be effective for high voltage power clamp because of its high ESD robustness, low on–resistance and holding voltage of greater than 20V, compared to conventional devices. This device may be applied to ICs requiring high reliability.

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References

[1] Huang, et al., "ESD protection design for advanced CMOS," Proc. SPIE, pp. 123-131, 2001.

[2] Huang, et al., "An SCR-Incorporated BJT Device for Robust ESD protection with High Latchup Immunity in High-Voltage Technology," IEEE Trans. Device and Material Reliability, vol. 12, No. 1, pp.113-123, 2012..

[3] Sze SM, "Physics of semiconductor device, 2nd ed. Newyork: Wiley, 1981.

[4] Wunsch DC, Bel RR. "Determination of threshold failure levels of semiconductor diodes and transistors due to pulsed voltage," IEEE Trans. Nucl Sci, pp.244-5, 1968.

[5] Dwyer VM, Fanklin Aj, Cambell DS,. "Thermal failure in semiconductor devices," Solid State Electronics, pp.553-560, 1990.

[6] Vashchenko, V.A., Sinkevitch, V.F., "Physical Limitaions of Semiconductor Devices, Springer, p.340, 2008.

[7] Fred G.. Kouper, "Design of SCR-based ESD Protection for Power Clamp using Deep-Submicron CMOS Technology," Microelectronics Jorunal, pp.

1007-1012, 2009.
[8] Fred G. Kouper, "The Design of high holding voltage SCR for whole-chip ESD protection," IEICE Electronics Express, pp. 1624-1630, 2008.
[9] MEDICI : Two-Dimensional Device Simulation Program, Synopsys Inc., 2007.
[10] E. Ground and M. Hernandez, "Obtaining TLP-like Information from an HBM simulator," EOS/ESD Symp., pp. 2A.3-1-2A.3-7, 2007.
[11] Donald A. Neamen, "Semiconductor Physics and Device : basic principle, 3rd ed.

Jin-Woo Jung received the MS degrees from the Department of electronic and electrical engineering at Dankook University in 2012. He is currently working toward the Ph.D. degree in Dankook University. His research interests include power semiconductor devices and electrostatic discharge (ESD) protection circuit design.

Yong-Seo Koo received the BS, MS, and PhD degrees in electronic engineering from Sogang University in 1981, 1983, and 1992, respectively. He joined the Department of Electronics and Electrical Engineering, Dankook University as a professor in 2009. His current research interests include power semiconductor devices, power management integrated circuits (PMIC) and electrostatic discharge (ESD) protection circuit design.