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Simplified PWM Strategy for Neutral-Point-Clamped (NPC) Three-Level Converter

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Abstract

A novel simplified pulse width modulation(PWM) strategy for neutral point clamped (NPC) three-level converter is proposed in this paper.The direct output voltage modulation is applied to reduce the calculation time. Based on this strategy, several optimized control methods are proposed. The neutral point potential balancing algorithm is discussed and a fine neutral point potential balancing scheme is introduced. Moreover, the minimum pulse width compensation and switching losses reduction can be easily achieved using this modulation strategy. This strategy also gains good results even with the unequal DC link capacitor. The modulation principle is studied in detail and the validity of this simplified PWM strategy is experimentally verified in this paper. The experiment results indicated that the proposed PWM strategy has excellent performance, and the neutral point potential can be balanced well with unequal DC link captaincies.

Key words: Minimum pulse width compensation, Neutral point potential balance, PWM, Switching losses reduction, Three-level converter

I. INTRODUCTION

The neutral-point-clamped (NPC) three-level converter [1] is the most preferred option in high power, medium voltage applications. Fig. 1 is the NPC three-level converter, which takes advantage of blocking one-half of the dc-link voltage and improved quality output voltages. However, the disadvantages of the NPC three-level converter are obvious, such as more power semiconductors, complicated PWM strategy, the possible drifting of neutral point (NP) potential [2], and uneven distribution of switching losses [3].

A number of studies have focused on three-level converter control strategies, among which carrier-based modulation (CBM) is the first and most widely used. However, this method has the drawbacks, such as limited modulation index (or the low DC bus voltage usage) and the difficulty to control the NP potential. As the research continues, zero sequence voltages are injected to all three-phase reference voltages to enlarge the liner modulation range and suppress the NP potential variation [4]-[7]. The NP potential can be balanced well with zero sequence voltage injection. However, the zero sequence voltages injected are not unique. Different zero sequence voltage can be injected to obtain different goals. The injection changes the switching states of three phases, and this change will be discussed in detail in this paper.

Nowadays, the space vector PWM (SVPWM) strategy becomes noticeable. The SVPWM scheme receives high DC bus utilization and low harmonic distortion in output voltage. Compared to CBM, the NP potential can also be easily balanced [8], [9]. However, the process requires a powerful microprocessor to accomplish the heavy calculation. In [10], a new SVPWM based on simplified diagram has been proposed. The space vector selection becomes simple and the calculation is reduced to a certain degree.

To obtain high quality output voltage, a study [11] investigated and proposed alternative switching sequences that used the pivot vector not only once, but also employed one of the other two vectors twice within the subcycle. Finally, two of the proposed sequences led to reduced THD at high modulation indices. However, these sequences induced high switching

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losses. In [12], a synchronized SVPWM algorithm was presented. Three-level converter eliminated subharmonics using this control algorithm for the over modulation region.

In the field of high power medium voltage applications, the junction temperature of the power semiconductors is most vital. High switching frequency leads to high junction temperature. Hence, numerous studies focus on how to reduce the switching losses by reducing the switching frequency. Many studies have been conducted on reducing switching losses for two-level converters, but reports on three-level NPC converters are scarce. In [13], an optimized discontinuous PWM method is presented to minimize the switching losses by varying the offset components.

The circuit-level decoupling concept was introduced into the NPC three-level converter control in [2]. A discontinuous PWM strategy based on [2] was proposed to reduce the switching losses. In [14], the predictive control was used in the NPC three-level converter control. A cost function, which includes terms of reference tracking, NP potential balancing, and switching losses reduction, is adopted for the control. This method consumes substantial calculation time, and the performance depends on whether the parameters in the model are precise or not.

In this paper, a simplified modulation strategy for NPC three-level converter is explored in detail. Generated from SVPWM, the proposed scheme is based on a new volt-second balance. The scheme avoids the complicated space vectors selection and simplifies the duration of calculation. The proposed PWM strategy can significantly reduce calculation time and the NP potential balancing can be easily implemented. Moreover, compensation of the minimum pulse width and reduction of switching losses are incorporated for the high power, high voltage applications. The proposed control strategy is verified by experiments.

In the traditional SVPWM and CBM strategies, the capacitor voltages are always treated the same when calculating the duration times even in an unbalanced NP potential state. However, this simplified PWM considers real output voltage of each phase terminals. This method is especially suitable for multi-level converter operating in transition state, such as capacitor voltages varying to some extent (as for the three-level converter, it means that the NP potential is not balanced). The converters under these situations have different features, and should be controlled with advanced PWM strategy. These topics are under study, and we have made some progress. However, these topics are beyond the scope of this paper and will be presented in the near future.

II. Principle of Simplified PWM Strategy

A. Principle of SVPWM for NPC Three-Level Converter

A typical NPC three-level converter is shown in Fig. 1.

Table I presents the switching states of each phase for the converter.

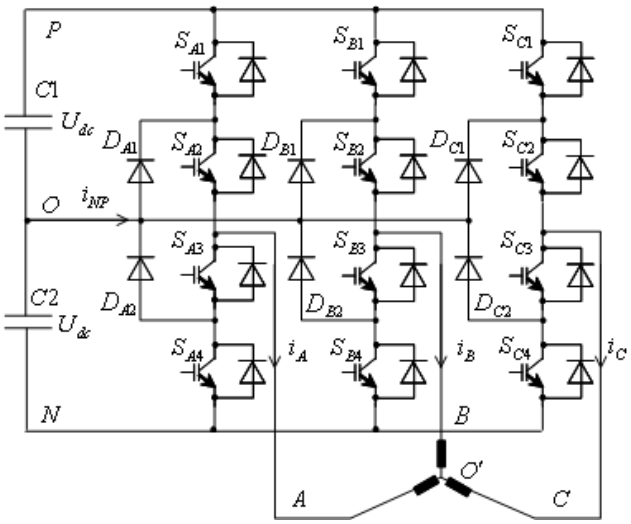


Fig. 1. Circuit of a NPC three-level converter.

TABLE I
Phase Switching States of Three-Level NPC Converter(X=A,B,C)

S1X	*S2X*	*S3X*	*S4X*	*Terminal Voltage*	*Switching State*
1	1	0	0	U_{dc}	P
0	1	1	0	0	O
0	0	1	1	$-U_{dc}$	N

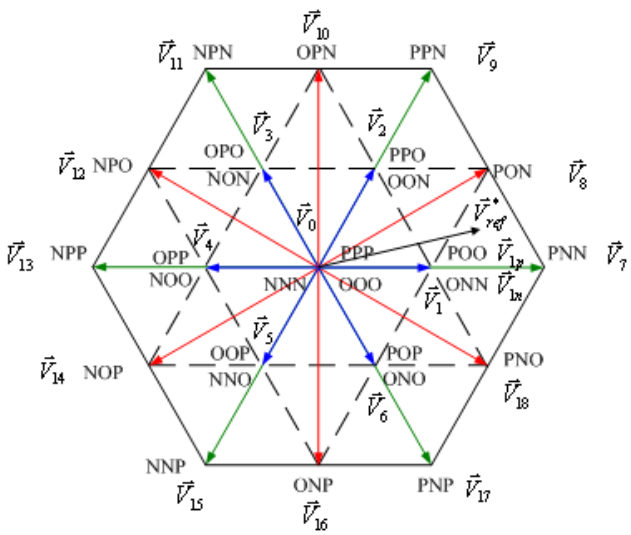
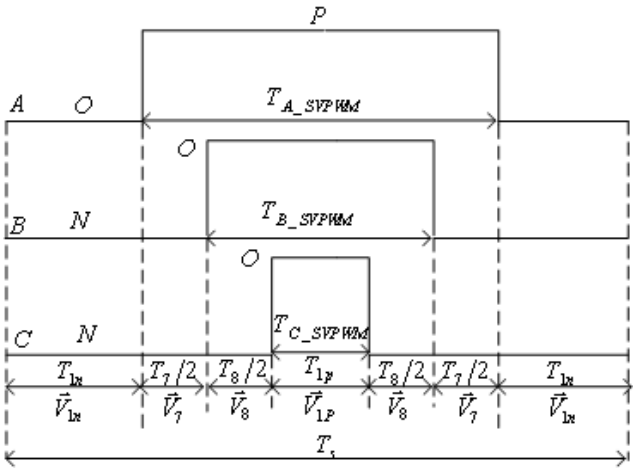


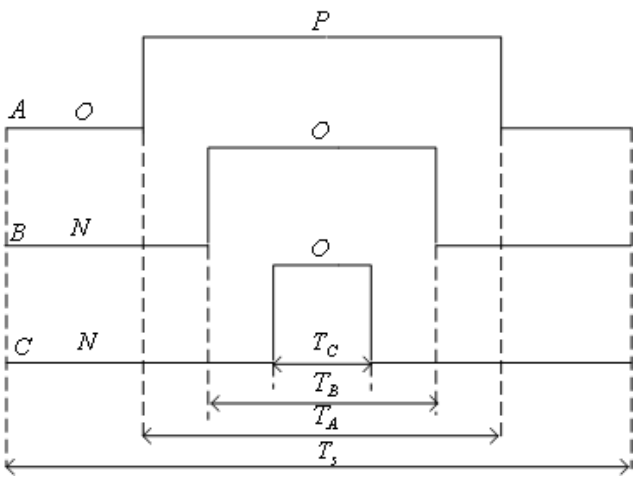
Fig. 2. Space vector diagram of NPC three-level converter.

The space vector diagram of a three-level converter with the definition of voltage space vector is illustrated in Fig.2.

For convenience, a reference voltage space vector $\vec{V}_{ref}^{*}$ is introduced (refer to Fig. 2).



(a)



(b)

Fig. 3. Diagram of switching sequences for NPC three-level converter.

The duration of each voltage space vector can be acquired by solving equation (1):

$$\begin{cases} \vec{V}_{ref}^{*} \cdot T_s = \vec{V}_{1p} \cdot T_{1p} + \vec{V}_7 \cdot T_7 + \vec{V}_8 \cdot T_8 + \vec{V}_{1n} \cdot T_{1n} \\ T_s = T_{1p} + T_7 + T_8 + T_{1n} \end{cases} \quad (1)$$

Equation (1) is the traditional phase volt-second balance rule of SVPWM. When we describe the balance rule in the three phase reference frame, Equation (1) can be rewritten as:

$$\begin{cases} u_{A\_ref}^{*} \cdot T_s = u_{AO'\_1p} \cdot T_{1p} + u_{AO'\_7} \cdot T_7 + u_{AO'\_8} \cdot T_8 + u_{AO'\_1n} \cdot T_{1n} \\ u_{B\_ref}^{*} \cdot T_s = u_{BO'\_1p} \cdot T_{1p} + u_{BO'\_7} \cdot T_7 + u_{BO'\_8} \cdot T_8 + u_{BO'\_1n} \cdot T_{1n} \\ u_{C\_ref}^{*} \cdot T_s = u_{CO'\_1p} \cdot T_{1p} + u_{CO'\_7} \cdot T_7 + u_{CO'\_8} \cdot T_8 + u_{CO'\_1n} \cdot T_{1n} \end{cases} \quad (2)$$

where $u_{X\_ref}^{*}$ (X=A, B, C) represents the three phase reference voltages in the three phase reference frame. $u_{XO'\_1p}$, $u_{XO'\_7}$, $u_{XO'\_8}$, $u_{XO'\_1n}$ (X=A, B, C) are the phase voltages of each space vector at the load side. According to KVL law, phase voltages of the load side are:

$$u_{XO'} = u_{XO} + u_{OO'} \quad (X = A, B, C) \quad (3)$$

Substituting Equation (3) into Equation (2), we obtain:

$$\begin{cases} u_{A\_ref}^{*} \cdot T_s = (u_{AO\_1p} \cdot T_{1p} + u_{AO\_7} \cdot T_7 + u_{AO\_8} \cdot T_8 + u_{AO\_1n} \cdot T_{1n}) \\ + (u_{OO'\_1p} \cdot T_{1p} + u_{OO'\_7} \cdot T_7 + u_{OO'\_8} \cdot T_8 + u_{OO'\_1n} \cdot T_{1n}) \\ u_{B\_ref}^{*} \cdot T_s = (u_{BO\_1p} \cdot T_{1p} + u_{BO\_7} \cdot T_7 + u_{BO\_8} \cdot T_8 + u_{BO\_1n} \cdot T_{1n}) \\ + (u_{OO'\_1p} \cdot T_{1p} + u_{OO'\_7} \cdot T_7 + u_{OO'\_8} \cdot T_8 + u_{OO'\_1n} \cdot T_{1n}) \\ u_{C\_ref}^{*} \cdot T_s = (u_{CO\_1p} \cdot T_{1p} + u_{CO\_7} \cdot T_7 + u_{CO\_8} \cdot T_8 + u_{CO\_1n} \cdot T_{1n}) \\ + (u_{OO'\_1p} \cdot T_{1p} + u_{OO'\_7} \cdot T_7 + u_{OO'\_8} \cdot T_8 + u_{OO'\_1n} \cdot T_{1n}) \end{cases} \quad (4)$$

where $(u_{XO\_1p} \cdot T_{1p} + u_{XO\_7} \cdot T_7 + u_{XO\_8} \cdot T_8 + u_{XO\_1n} \cdot T_{1n})$ are the terminal voltages of three phases. Their values are different from phase to phase.

$(u_{OO'\_1p} \cdot T_{1p} + u_{OO'\_7} \cdot T_7 + u_{OO'\_8} \cdot T_8 + u_{OO'\_1n} \cdot T_{1n})$ denotes the common mode voltages introduced by different voltage space vectors, which are the same for all three phases, and acts like the zero sequence voltage. These two terms are treated as a whole to obtain sinusoid line voltages and currents in traditional SVPWM. However, this process explains why the calculation of traditional SVPWM is very complex. Let

$\int_0^{T_s} u_{XO}(t)dt = u_{XO\_1p} \cdot T_{1p} + u_{XO\_7} \cdot T_7 + u_{XO\_8} \cdot T_8 + u_{XO\_1n} \cdot T_{1n}$,

$\int_0^{T_s} u_{OO'}(t)dt = u_{OO'\_1p} \cdot T_{1p} + u_{OO'\_7} \cdot T_7 + u_{OO'\_8} \cdot T_8 + u_{OO'\_1n} \cdot T_{1n}$,

Equation (4) can be simplified as:

$$\begin{cases} u_{A\_ref}^{*} \cdot T_s = \int_0^{T_s} u_{AO}(t)dt + \int_0^{T_s} u_{OO'}(t)dt \\ u_{B\_ref}^{*} \cdot T_s = \int_0^{T_s} u_{BO}(t)dt + \int_0^{T_s} u_{OO'}(t)dt \\ u_{C\_ref}^{*} \cdot T_s = \int_0^{T_s} u_{CO}(t)dt + \int_0^{T_s} u_{OO'}(t)dt \end{cases} \quad (5)$$

The conclusion is obtained from analyzing a triangle region, and can also be obtained by studying other regions. In SVPWM schemes, the term $\int_0^{T_s} u_{OO'}(t)dt$ changes in a complicated manner according to the phase volt-second balance equations.

B. Proposed Simplified PWM

As for the traditional SVPWM schemes, the selection of sectors (or triangle region) and the calculation of space vector duration consumes significant calculation time. To reduce the calculation time, the sector selection and duration time calculation should be simplified. An example is presented to explain the principle.

When we set $\int_0^{T_s} u_{OO'}(t)dt$ to zero, Equation (5) becomes:

$$\begin{cases} u^*_{A\_ref} \cdot T_s = \int_0^{T_s} u_{AO}(t)dt \\ u^*_{B\_ref} \cdot T_s = \int_0^{T_s} u_{BO}(t)dt \\ u^*_{C\_ref} \cdot T_s = \int_0^{T_s} u_{CO}(t)dt \end{cases} \quad (6)$$

Equation (6) implies that when we maintain $\int_0^{T_s} u_{OO'}(t)dt$ equal to zero in each PWM period, a PWM directly constructing the terminal voltage of three phases can be realized, implying that we can obtain a PWM scheme with a new simple volt-second balance rule, which only requires three-phase and DC voltage. In Equation (6), $u_{XO}(t)$ (X=A, B, C) can be expressed as U_{dc}, 0, $-U_{dc}$. For three-level converters, we can determine them by using reference phase voltages in advance based on the following rules. When $u^*_{X\_ref} > 0$ (X=A, B, C), $u_{XO}(t)$ consists of U_{dc} and zero; otherwise $u_{XO}(t)$ consists of $-U_{dc}$ and zero. This rule divides the space vector diagram into six sectors denoted by S in Fig. 4.

For example, when $u^*_{A\_ref} > 0$, $u^*_{B\_ref} < 0$, $u^*_{C\_ref} < 0$, the reference voltage space vector is located in sector I. $u_{AO}(t)$ consists of U_{dc} and zero, $u_{BO}(t)$ consists of $-U_{dc}$ and zero, $u_{CO}(t)$ consists of $-U_{dc}$ and zero, and we can obtain the PWM waveforms shown in Fig. 3(b). Substituting these results to Equation (6), we can obtain the duration times of the three phases:

$$\begin{cases} T_A = (u^*_{A\_ref} \cdot T_s)/U_{dc} \\ T_B = T_s + (u^*_{B\_ref} \cdot T_s)/U_{dc} \\ T_C = T_s + (u^*_{C\_ref} \cdot T_s)/U_{dc} \end{cases} \quad (7)$$

Other sectors can also be analyzed through this method. Setting $\int_0^{T_s} u_{OO'}(t)dt$ to zero simplifies the calculation of duration times. However, another problem occurs and will be explained in detail in section III.

III. Modulation Index Limitation and the Solution

A. Modulation Index Limitation Analysis

Equation (7) works quite well when the reference phase voltage is low. Once the reference voltage reaches the critical point U_{dc}, this method becomes invalid and the calculated results of the duration times appear to be unrealistic. Similar to the CBM with no zero sequence voltages injection, the method was referred to as weak usage of DC bus voltage.

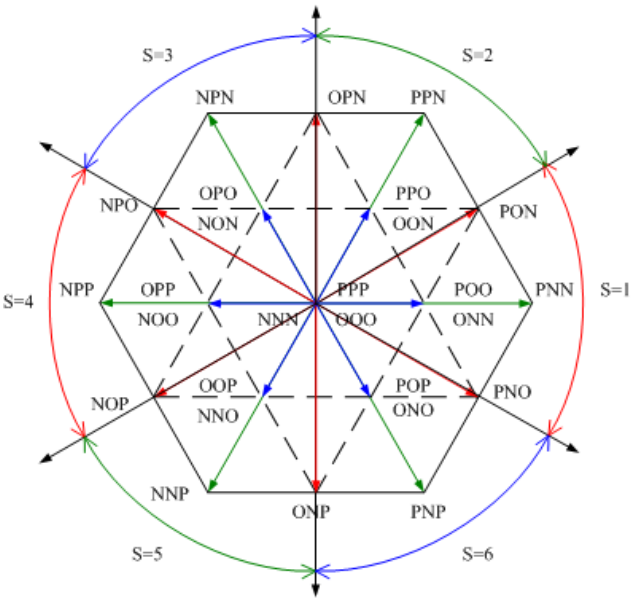


Fig. 4. Sectors for NPC three-level converter with proposed PWM.

In this section, adjustment in duration time will be introduced to break the modulation index limitation. Based on the adjustment, a multi-object control method will be presented in the next section with the advantages of NP potential balancing, minimum pulse width compensation, and switching losses reduction. Fig. 5 shows the changes in breaking the modulation index limitation; the principle will be studied in detail as follows.

When the modulation index limitation occurs, $u_{XO}(t)$ loses the pulse width modulation information because it is clamped to a fix voltage level. We assume $u^*_{A\_ref}$ reaches U_{dc}, the corresponding duration time T_A begins to exceed the available time T_s. The upper figure in Fig. 5 is an example of this situation. To extend the modulation range in CBM, a zero sequence voltage is injected into the reference phase voltages to decrease the peak value of the reference voltage. Unfortunately, the amplitude of the zero sequence voltage is difficult to decide. For two-level converters, SVPWM approach can be selected, but the three-level NP converters should consider more factors, such as NP potential balancing.

When the zero-sequence voltage injection is adopted in the proposed PWM, Equation (6) is modified to:

$$\begin{cases} (u^*_{A\_ref} - u_z) \cdot T_s = \int_0^{T_s} U_{AO}dt \\ (u^*_{B\_ref} - u_z) \cdot T_s = \int_0^{T_s} U_{BO}dt \\ (u^*_{C\_ref} - u_z) \cdot T_s = \int_0^{T_s} U_{CO}dt \end{cases}, \quad (8)$$

where u_z is the zero-sequence voltage. Hence, Equation (8)

can be modified as follows:

$$\begin{cases} T_A' = (u_{A\_ref}^* \cdot T_s)/U_{dc} - (u_z \cdot T_s)/U_{dc} \\ T_B' = T_s + (u_{B\_ref}^* \cdot T_s)/U_{dc} - (u_z \cdot T_s)/U_{dc} \\ T_C' = T_s + (u_{C\_ref}^* \cdot T_s)/U_{dc} - (u_z \cdot T_s)/U_{dc} \end{cases}. \quad (9)$$

From Equation (9), the modified duration times T_X' (X=A, B, C) for each phase can be easily derived. Let ΔT represent $(u_z \cdot T_s)/U_{dc}$. Equation (9) can be rewritten as:

$$\begin{cases} T_A' = T_A - \Delta T \\ T_B' = T_B - \Delta T \\ T_C' = T_C - \Delta T \end{cases}. \quad (10)$$

In Equation (10), the direct modification in the durations of the three phases has the same effect as a zero sequence voltage injection. Hence, the strategies with zero sequence voltage injection to improve the performance of the three-level converters can also be achieved by modifying the duration times directly.

B. Simple Solution to Break Modulation Index Limitation

The absolute value of ΔT is proportional to the zero-sequence voltage. For convenience, this modification can be executed in a simple manner as shown in Fig. 5, and the modification can also be explained in Equation (11) by assuming $\Delta T = T_A - T_s$. That is:

$$\begin{cases} T_A' = T_s \\ T_B' = T_B - (T_A - T_s) \\ T_C' = T_C - (T_A - T_s) \end{cases}. \quad (11)$$

Following Equation (11), our PWM scheme modifies the duration times directly to extend the linear modulation range. The extension is more convenient for pulse width control and is useful for NP potential balancing, minimum pulse width compensation, and switching losses reduction for NPC three-level converter. These topics will be presented in section IV.

C. Maximum Linear Modulation Index of the Proposed PWM Strategy

The duration times can be modified in a flexible way, and the mathematic derivation of the maximum linear modulation index is presented. Analyses for sector I in Fig. 4 are reasonable and sufficient because of symmetry.

The analysis indicated that the manner to overcome the modulation index limitation is to modify all duration times of the three phases. When T_A begins to exceed available time T_s, ΔT is subtracted from all duration times of three phases. If ΔT is smaller than $\min(T_A, T_B, T_C)$, the PWM can still

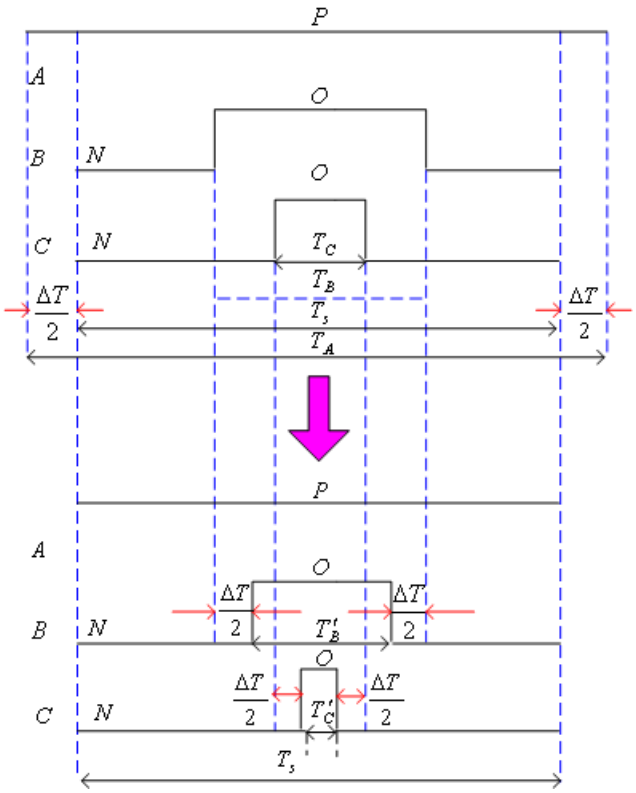


Fig. 5. Modulation index extending process.

acquire a linear modulation. However, once the ΔT is larger than $\min(T_A, T_B, T_C)$, two (even three) phases are clamped to fixed voltages. Therefore, over modulation occurs. The linear modulation in sector I should satisfy:

$$\begin{cases} [(u_{A\_ref}^* - u_z) \cdot T_s]/U_{dc} \le T_s + (u_{B\_ref}^* \cdot T_s)/U_{dc} \\ [(u_{A\_ref}^* - u_z) \cdot T_s]/U_{dc} \le T_s + (u_{C\_ref}^* \cdot T_s)/U_{dc} \end{cases}. \quad (12)$$

In sector I, the reference voltages are:

$$\begin{cases} u_{A\_ref}^* = m \cdot U_{dc} \cos(\theta) \\ u_{B\_ref}^* = m \cdot U_{dc} \cos(\theta - \frac{2\pi}{3}) \\ u_{B\_ref}^* = m \cdot U_{dc} \cos(\theta + \frac{2\pi}{3}) \end{cases} \quad -\frac{\pi}{6} \le \theta \le \frac{\pi}{6} \quad (13)$$

where m is the linear modulation index using the proposed PWM scheme. Substituting Equation (13) into Equation (12), the allowable range of the m can be deduced as follow:

$$m \le \frac{2}{\sqrt{3}\cos(\theta + \pi/6)} = \frac{2}{\sqrt{3}} = 1.15 \quad (14)$$

Equation (14) implies that the proposed PWM strategy obtains the same linear modulation range as traditional SVPWM.

IV. Optimized Strategy for NPC Three Level Converter

The drawbacks of NPC three-level converter are NP potential variation, unequal switching losses distribution, and so on. These problems should be resolved or suppressed to some extent to stabilize power system.

The NP potential variation can be suppressed through PWM control in many ways. Each NP potential balancing scheme should follow their own rules; however, they all employed the redundant switching states to achieve this goal essentially, and so does this proposed scheme.

The converter may operate in four quarters, and the NP potential will fluctuate in a more complex way. This paper will provide a universal analysis on the NP potential variation and the solutions.

A. Analysis of NP Potential Variation and Finer NP Potential Balancing Solution

Numerous studies have discussed the NP potential variation problem and provided the solutions. A comprehensive study regarding the problem has been done in [9], and provided the border of the NP potential controllability for different modulation indices and power factors. In [6], a CBM strategy with zero sequence voltage injection was proposed to improve the traditional CBM strategy. With the injected zero sequence voltage, the NP potential can be controlled to reduce the low frequency voltage oscillation, and the switching losses is reduced as well. In this paper, a new PWM scheme was used to analyze the problems and a solution is given.

From the point of SVPWM, some short voltage space vectors (like POO, ONN and so on) and medium voltage space vectors (like PON and so on) will affect the NP potential. Actually, all switching states connected to the NP will affect the NP potential. For convenience, the analysis used Fig. 2(b) as an example, and the direction of assumed current flow is shown in Fig. 1.

When the sample and switching frequency is high enough, the current in the sampling period can be treated as a constant value and the sampling delay is ignored. The average current i_{NP} that flows through the NP can be calculated as:

$$i_{NP} = \frac{i_A \cdot (T_s - T'_A) + i_B \cdot T'_B + i_C \cdot T'_C}{T_s} \tag{15}$$

When NP potential fluctuates, i_{NP} can be modified by changing the duration times to suppress the fluctuation. Assuming T_{err} is introduced to achieve this goal, the current i'_{NP} is:

$$\begin{aligned} i'_{NP} &= \frac{i_A \cdot [T_s - (T'_A + T_{err})] + i_B \cdot (T'_B + T_{err}) + i_C \cdot (T'_C + T_{err})}{T_s} \\ &= i_{NP} - \frac{2i_A}{T_s} \cdot T_{err} \end{aligned} \tag{16}$$

T_{err} causes i'_{NP} to increase or decrease according to the situation, and will act on the NP potential finally. T_{err} is determined by:

$$\begin{cases} T_{err} = \dfrac{i_{NP} \cdot T_s - C \cdot U_{err}}{2 \cdot i_A} \\ T_{err} \le T_s - \max(T'_A, T'_B, T'_C) \quad (when T_{err} \ge 0), \\ abs(T_{err}) \le \min(T'_A, T'_B, T'_C) \quad (when T_{err} < 0) \end{cases} \tag{17}$$

where $C = C1 = C2$ is the capacitance of DC link, $U_{err} = U_{C2} - U_{C1}$ is the error of the NP potential. When i'_{NP} is positive, the NP potential will decrease, otherwise, it will increase. We can pre-calculate the i_{NP} and modify T'_X (X=A, B, C) to meet the need to suppress NP potential drifting in theory. In practice, i_{NP} and i'_{NP} are different from the calculated values following Equations (15) and (16) because the sampling and the switching frequency are inadequate. Meanwhile, the dead time effects also function. A small asymmetric in the main circuit will result in long slow drifting in the NP potential. Therefore, a small ripple in the error of NP potential around the ideal zero line may occur. The modification of procedures on duration times are shown in Fig. 6, and the mathematical process is:

$$\begin{cases} T''_A = T'_A + T_{\text{err}} \\ T''_B = T'_B + T_{\text{err}} \\ T''_C = T'_C + T_{\text{err}} \end{cases} \tag{18}$$

B. Minimum Pulse Width Compensation

Minimum pulse width must be considered in designing PWM schemes because it may exceed the permissible values of power semiconductors. When the magnitude of one of the three-phase reference voltages is less than the minimum voltage, a discontinuous PWM method with on minimum pulse width compensation and an NP potential balancing scheme are proposed in [15]. However, threats to the power semiconductors will appear in two situations: the magnitude of one phase reference voltage is either too small or too large, which are known as active high and active low minimum pulse width in this paper. Fig.7 shows these two situations. For these two narrow pulses, each has two methods to compensate. The analysis and solutions are mirror images of each other. Only

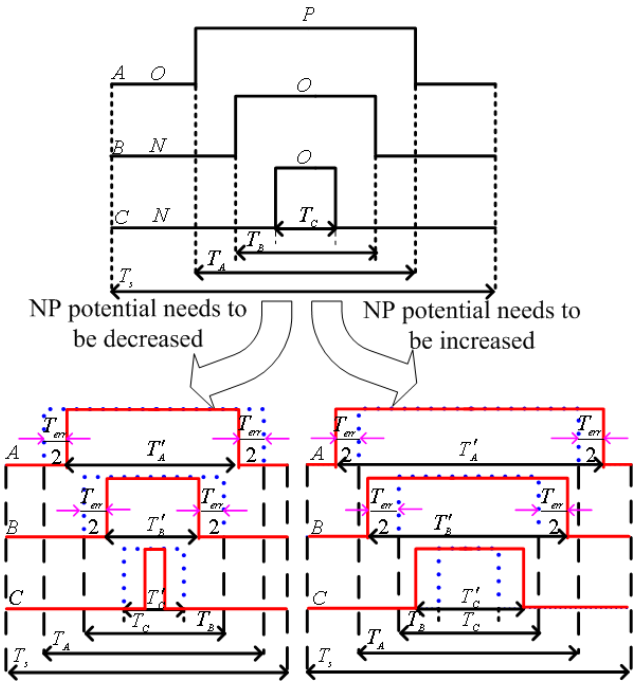


Fig. 6. Relation between PWM waveforms and NP potential drifting suppress.

one case is studied in detail, and the processes are shown clearly in Fig. 7.

Active high minimum pulse width compensation:

①Modify T'_X (X=A, B, C) by adding a time T_{offset} to T'_X, and the result should satisfy:

$$T_{\min\_allow} \le T'_X + T_{offset} \le T_{\max\_allow}. \tag{19}$$

②Modify T'_X (X=A, B, C) by subtracting a time T_{offset} to T'_X, and the result should satisfy :

$$\begin{cases} \max(T'_X - T_{offset}) \le T_{\max\_allow} \\ mid(T'_X - T_{offset}) \ge T_{\min\_allow} \\ \min(T'_X - T_{offset}) = 0 \end{cases} \tag{20}$$

In Equations (19) and (20), $T_{\min\_allow}$ and $T_{\max\_allow}$ are the minimum and maximum allowed pulse widths that prevent the modification from generating new narrow pulse. The values are decided by the characters of the power semiconductors.

These two methods can solve the narrow pulse problem, but they have different effects on the NP potential because of the change in i_{NP}. Moreover, the switching frequency of some phase legs will be different from these two methods. When dealing with the minimum pulse width compensation, we should consider the NP potential balancing and the switching losses reduction to meet the implementation requirement.

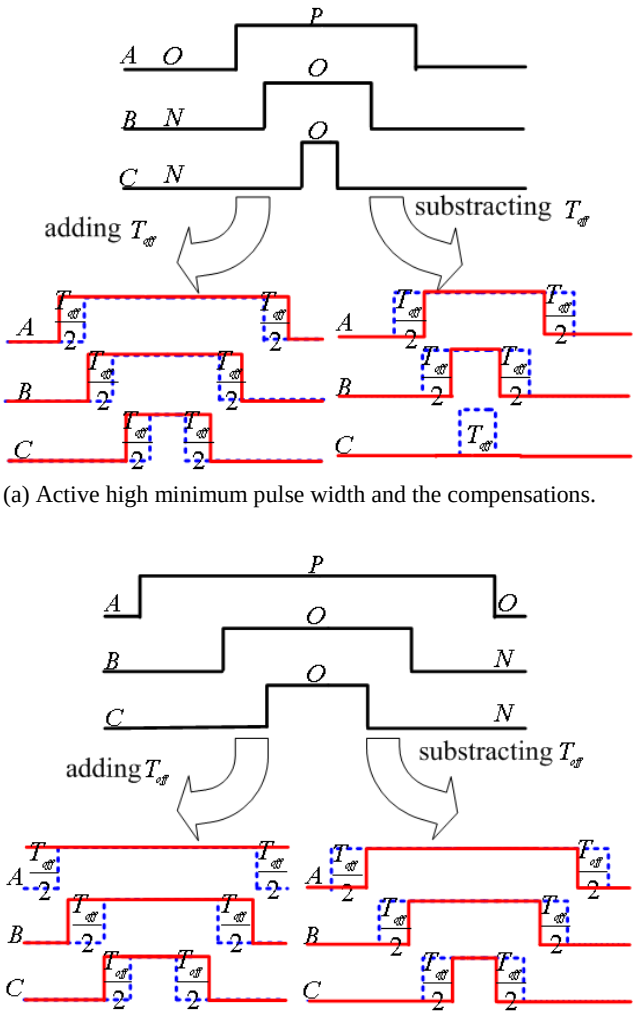


Fig. 7. Minimum pulse width in PWM and their compensations.

C. Switching Losses Reduction

To reduce the switching losses, the new PWM strategy adopts the DC bus clamped method of discontinuous PWM strategy. Fig. 4 illustrates that when the reference voltage space vector is located in sector I, phase A can be clamped to P point of the DC link or phase C can be clamped to N point by all duration times modification of the three phases. The absence of force-commutates in phase A or C will reduce the switching losses. In other sectors, three phase legs can be clamped to one of the three points (P, O, N) of the DC link.

The proposed PWM strategy provides the possibility to achieve this goal, with a modification in T'_X (X=A, B, C) following Equations (21) or (22):

$$\begin{cases} T''_A = T'_A + [T_s - \max(T'_A, T'_B, T'_C)] \\ T''_B = T'_B + [T_s - \max(T'_A, T'_B, T'_C)] \\ T''_C = T'_C + [T_s - \max(T'_A, T'_B, T'_C)] \end{cases} \tag{21}$$

$$\begin{cases} T_A'' = T_A' - \min(T_A', T_B', T_C') \\ T_B'' = T_B' - \min(T_A', T_B', T_C') \\ T_C'' = T_C' - \min(T_A', T_B', T_C') \end{cases} \quad (22)$$

However, contradiction between NP potential balancing and switching losses reduction may exist. Therefore, we should make a tradeoff between NP potential controllability and switching losses reduction, implying that roughly balancing of the NP potential variation is adopted when the switching losses reduction is necessary.

When the converter is required to operate in low switching losses state, the priority should be given to switching losses reduction. First, we set the NP potential unbalance threshold. This threshold should be set to under 5% of the DC voltage to reduce the even harmonics and avoid the low frequency torque pulsation introduced by NP potential when driving motors. We set the threshold to 4% in the experiments. Second, we should monitor the operation of the converter and balance the NP potential according to the convertor operation state. For example, the converter will run in the low switching losses state with the time modification following Equation (21) until the NP potential varies beyond the threshold. When the threshold is exceeded, time modification will be calculated according to Equation (22), and i_{NP} will be calculated using Equation (15) by substituting T_X'' to T_X'. The i_{NP}, which decreases the NP potential is preferred, and the corresponding time modification is adopted. The flow chart is shown in Fig.8.

The entire control strategy is shown in Fig. 9.

V. Analysis on Experiments of Simplified PWM Strategy

To verify the proposed simplified PWM strategy of the NPC three-level converter, the experiments were conducted on two platforms. The measuring equipments include an Agilent Technologies MSO6014A scope, three Tektronix P5200A high voltage differential Probes, a Rogowski current waveform transducer CWT1, and a three phase power quality analyzer Fluke 435. The experiment equipment of NPC three-level converter is shown in Fig.10.

A. Time Consuming of the Simplified PWM

The proposed PWM strategy and the simplified SVPWM strategy proposed in [10] were programmed using the TMS320F2812 DSP board with the same code composer studio configuration and coding style. The DSP consumed 7.43 μS to complete the proposed PWM strategy, whereas the reference SVPWM strategy duration was 14.46 μS. The calculation time was reduced significantly. Moreover, the code size was decreased by nearly 50%.

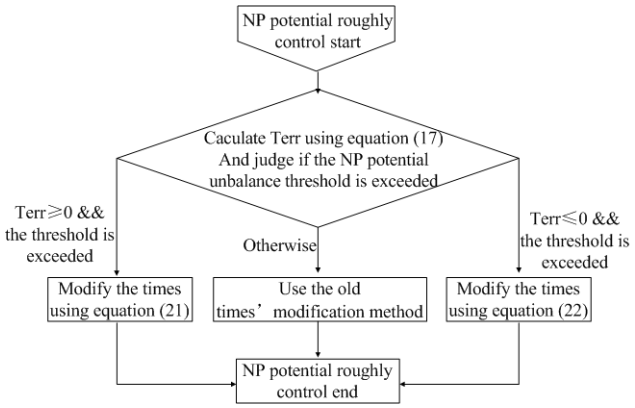


Fig. 8. Flow chart of the rough NP potential control.

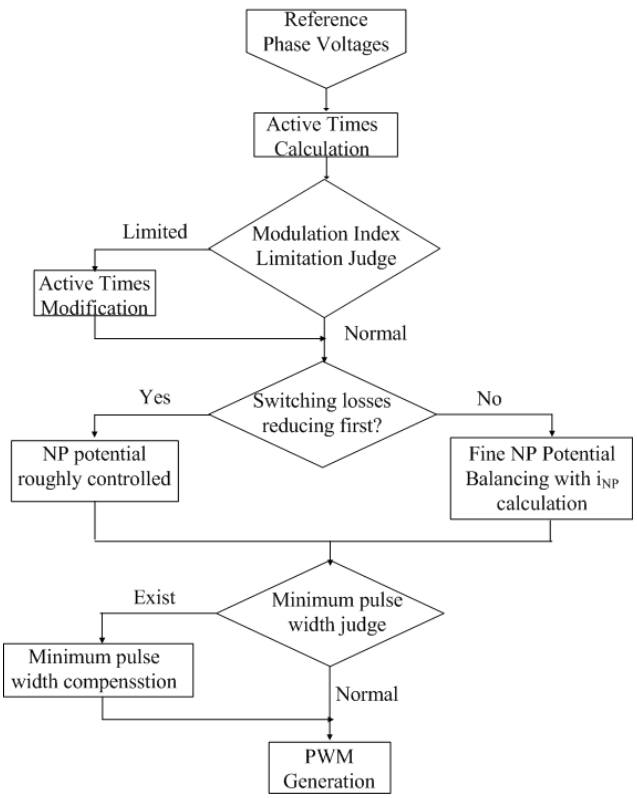


Fig. 9. Flow chart of the simplified PWM control strategy.

The strategy is an attractive alternative for some time-critical or cost-sensitive applications,

B. Results of Three-level Inverter

A test for NPC three-level converter working as an inverter over a wide modulation range was conducted. The main experimental parameters were DC-bus voltage $2U_{dc} = 270V$, DC link capacitors $C1 = C2 = 2500\mu F$, switching frequency $f_{sw} = 2kHz$, and three phase resistive–inductive load $R = 8\Omega$ and $L = 23mH$.

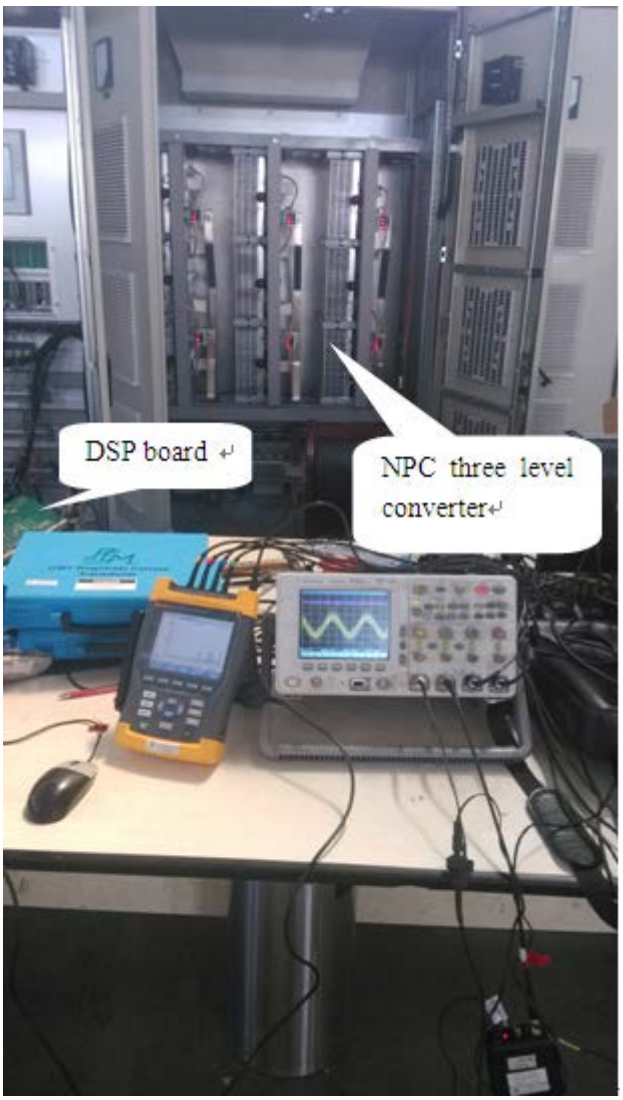


Fig. 10. Experiment equipment of NPC three-level converter.

Experiments have been conducted by modifying the modulation index from 0.07 to 1.03 with a fixed increment, and 15 samples were used for analysis. Figs. 11 and 12 show the curves of load side phase voltage total harmonic distortion (THD) and the relative error in different modulation index. The curves show that phase voltage THD decreases as the modulation increases, and the relative error was maintained at a low level. Compared with the reference SVPWM, the proposed PWM performed better to a certain degree.

However, the proposed PWM showed a poor THD in the modulation index from 0.48 to 0.68 because a simple solution using Equation (11) was adopted to solve the over modulation problem. This procedure changed the PWM waveform from centralized seven segments to five segments. Therefore, THD increased.

C. Results of Three-Level Rectifier

A test for NPC three-level converter working as a rectifier

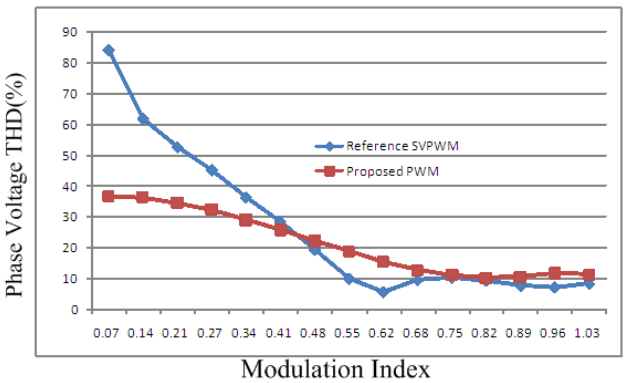


Fig. 11. Relation between phase voltage THD and modulation index.

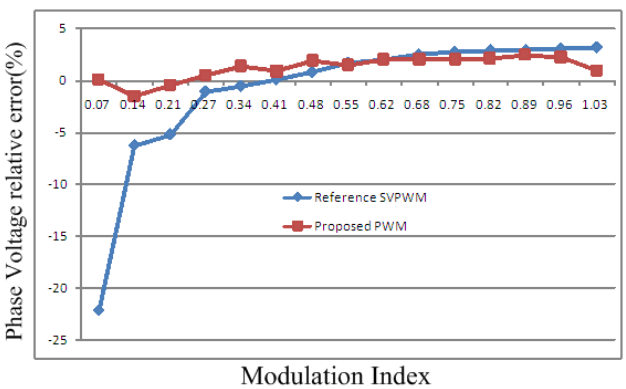


Fig. 12. Relation between the relative error of phase voltage and modulation index.

was conducted. The main experimental parameters were DC-bus voltage $2U_{dc} = 300V$, DC-link capacitors remained the same, switching frequency $f_{sw} = 2kHz$, the load of DC link ($R_{Load} = 16\Omega$), grid side voltage $U_g = 120V$, and inductor of grid side ($L = 1.5mH$). To measure the phase voltage of the converter, a three phase resistive load ($R = 5.1k\Omega$) was used.

Experiments were performed with fine NP potential balancing and switching losses reduction. Figs. 13-15 show the phase A terminal voltage, phase voltage, phase current, and DC link voltages with fine NP potential balancing. With the i'_{NP} calculation, the NP potential variation was suppressed and the THD of the phase A current was controlled to 3.3%. Figs. 16-18 show the phase A terminal voltage, phase voltage, phase current, and DC link voltages with switching losses reduction. We know that the switching frequency significantly decreased. The NP potential oscillated because a rough NP potential balancing scheme was adopted. As the switching frequency decreased, the phase A current THD increased to 6.2%. The harmonic contents in the current were mainly distributed in high order harmonics and could be easily

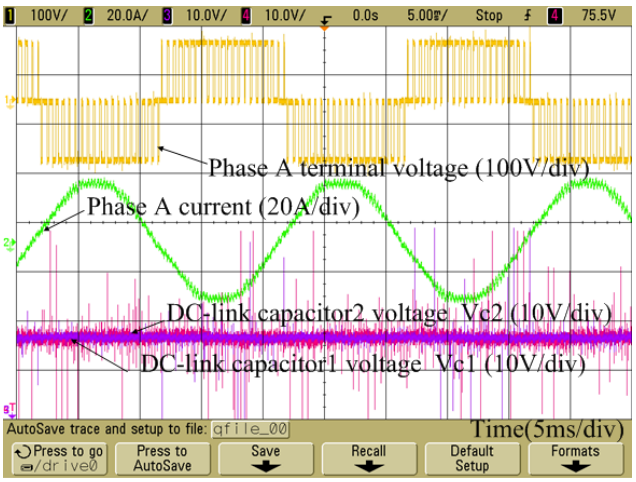


Fig. 13. Phase A terminal voltage, phase A current, DC-link voltages with fine NP potential balancing.

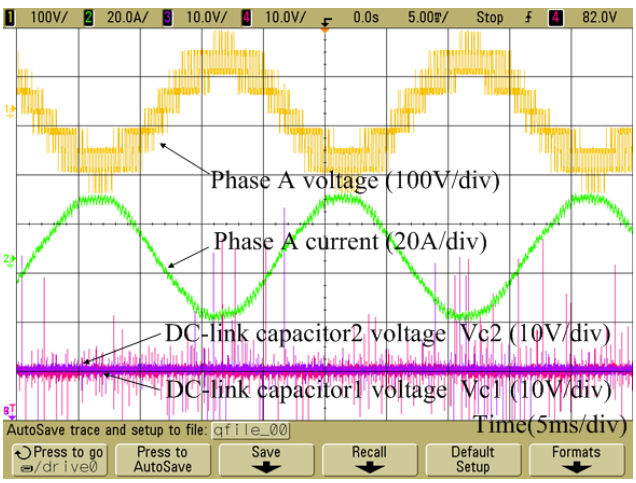


Fig. 14. Phase A voltage, phase A current, DC-link voltages with fine NP potential balancing.

eliminated by a passive filter. However, the reduction was useful for some high power, high voltage applications because of the significant switching losses reduction.

D. Results of Three-Level Inverter with Unequal DC Link Capacitors

In practical engineering, the NPC three-level converter could not operate in ideal conditions. For example, the capacitance of the DC link capacitors in series may not be the same. The dead time used to avoid the short circuit state existed. Therefore, the calculated time in theory using Equation (17) for the control of the converter may not be the required one. The accumulative errors could lead to NP potential variation. In this state, the calculated T_{err} will not be the best value, but the control remained stable because U_{err} was introduced in Equations (16) and (17). The NP potential will fluctuate around the ideal line.

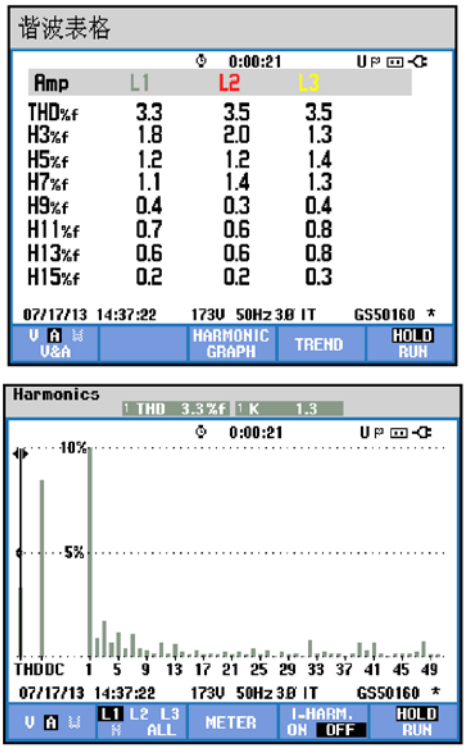


Fig. 15. Measured phase A current spectra with fine NP potential balancing.

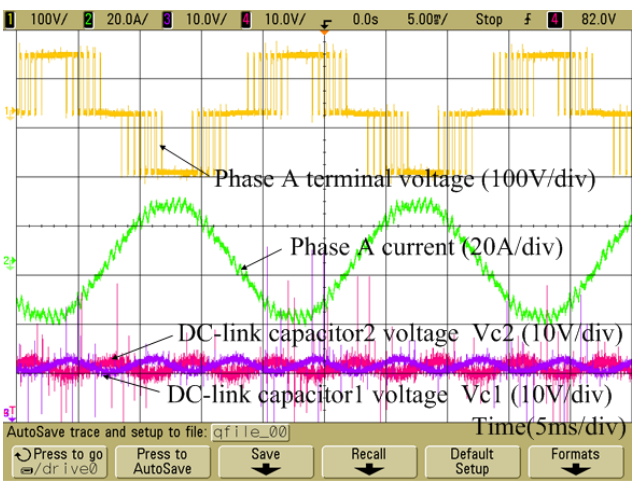


Fig. 16. Phase A terminal voltage, phase A current, DC-link voltages with switching losses reduction.

A test for NPC three-level converter working as an inverter with unequal DC link capacitors was conducted. The main experimental parameters were DC-bus voltage $2U_{dc} = 270V$, DC link capacitors $C1 = 2500\mu F$, $C2 = 2970\mu F$, switching frequency $f_{sw} = 2kHz$, and three phase resistive–inductive load $R = 8\Omega$ and $L = 23mH$. Figs.19 and 20 show the waveforms of the experiment. The NP potential states were from unbalance to balance. We conclude that the NP potential

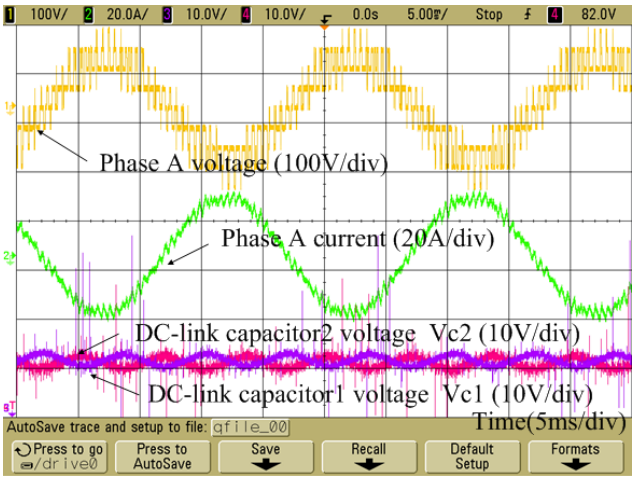


Fig. 17. Phase A voltage, phase A current, DC-link voltages with switching losses reduction.

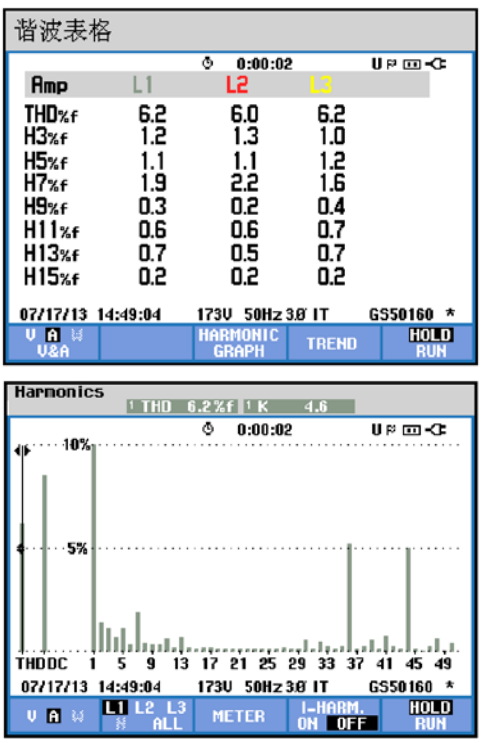


Fig. 18. Measured phase A current spectra with switching losses reduction.

could also be balanced under the unequal DC link capacitors with the proposed PWM strategy. However, the NP potential fluctuated because the calculated T_{err} was not the appropriate one.

VI. Conclusions

Based on a new volt-second balance rule for NPC three-level converters, a simplified PWM strategy was proposed. The duration times of three phases can be calculated easily using this method. Different from SVPWM,

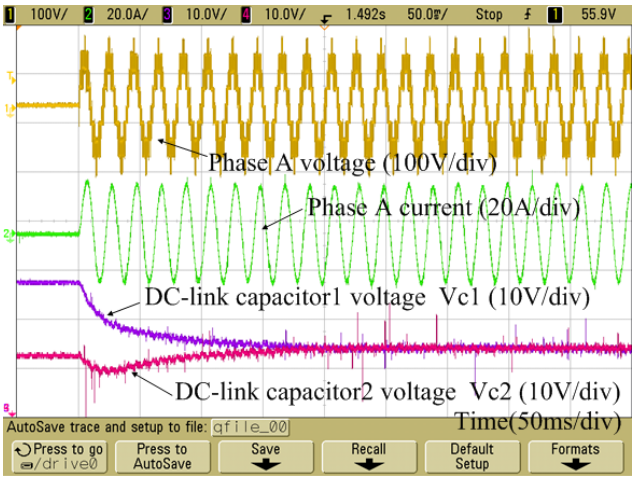


Fig. 19. Phase A voltage, phase A current, DC-link voltages under unequal DC link capacitors (overview).

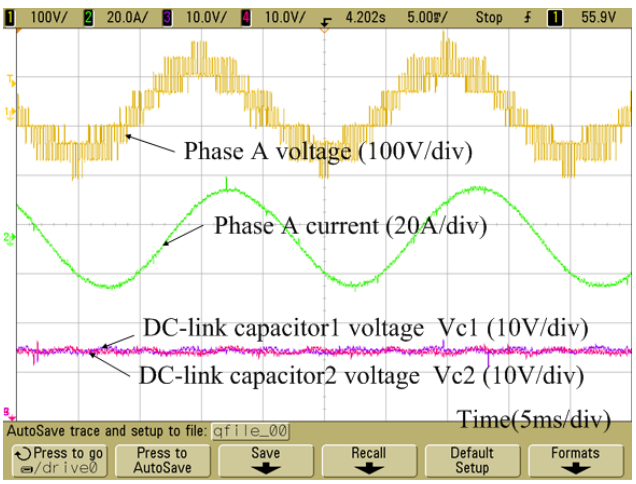


Fig. 20. Phase A voltage, phase A current, DC-link voltages under unequal DC link capacitors (detail).

calculating each space voltage vector duration was unnecessary. The basic principle of the proposed strategy was studied. Meanwhile, the modulation index limitation and the corresponding solution were analyzed. The relationship between zero sequence voltage injection and direct duration times modification was revealed. Based on the analysis, several optimized control were realized. A fine balancing method is proposed because the NP potential variation is a problem for NPC three-level converter. Moreover, this paper presented solutions including minimum pulse width compensation and switching losses reduction for high power, high voltage applications. Another test with unequal DC link capacitors was conducted. The results indicated that the proposed strategy can still balance the NP potential even in this worse state. Finally, the experiments were conducted to verify this proposed PWM strategy.

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