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Bi-Directional Multi-Level Converter for an Energy Storage System

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Abstract

This paper proposes a 3 kW single-phase bi-directional multi-level converter for energy storage applications. The proposed topology is based on the H-bridge structure with four switches connected to the DC-link. A simple phase opposition disposition PWM method that requires only one carrier signal is also suggested. The switching sequence to balance the capacitor voltage is considered. The topology can be extended to a nine-level converter or a three-phase system. The operating principle of the proposed converter is verified through a simulation and an experiment.

Key words: Multi-level converter, Power conditioning system, PWM strategy , Renewable energy sources

I. INTRODUCTION

Grid-connected converter systems are increasingly becoming important as a result of the increasing demand on renewable energy [1]-[3]. The prospect of vehicles plugging into electric grids, known as plug-in electric vehicles, reinforces the undeniable economic benefits that result in the independence from petroleum and the displacement of gasoline by electricity. The importance of the trend in future power systems will further intensify. Thus, converters for grid-connected operation should meet the following requirements.

1) The converter has to generate a pure sinusoidal output voltage.
2) The converter output current should possess low total harmonic distortion (THD).

Two-level PWM converters are traditionally used for grid-tied inverter systems. In the case of a two-level converter, the converter switching frequency should be high or the inductance of the output filter inductor has to be sufficient to satisfy the required THD for two-level converters. To address the problems associated with two-level converters, multi-level converters (MLCs) are introduced for grid-connected converters. Several MLC topologies have been suggested. These topologies can be mainly classified into three types, as shown in Fig. 1: neutral point clamped type, flying capacitor type, and cascaded type [4]-[7].

MLCs are advantageous because their switching frequency and device voltage rating can be significantly lower than those of a traditional two-level converter under the same output voltage. Therefore, switching loss can be reduced significantly, and converter efficiency can be increased [8]-[10].

In this paper, a circuit based on the H-bridge topology with four switches connected to the DC-link is proposed as MLC topology. Fig. 2 shows the proposed MLC. The power flow is bi-directional, and the power factor of the ac side is controllable. The number of the active switches is similar to that of traditional MLCs, as shown in Fig. 1. However, the switches in the H-bridge of the proposed converter (T_A^+, T_A^-, T_B^+ , and T_B^-) are turned on and off once at the fundamental 60/50 Hz frequency. The voltage stress the switches in the H-bridge is twice the number of switches in the DC-link (T_P^+, T_P^-, T_N^+, and T_N^-). Thus, a relatively slow and high voltage rating switch is used in the H-bridge, and a fast and low voltage rating switch is used in the DC-link.

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TABLE I
OUTPUT VOLTAGES ACCORDING TO SWITCHING STATES

Output voltage (V_{AB})	Switching state					
	T_P^+	T_P^-	T_N^+	T_N^-	T_A^+, T_B^-	T_A^-, T_B^+
V_{DC}	ON	OFF	OFF	ON	ON	OFF
V_{DC} /2	OFF	ON	OFF	ON	ON	OFF
	ON	OFF	ON	OFF	ON	OFF
0	OFF	ON	ON	OFF	ON	OFF
	OFF	ON	ON	OFF	OFF	ON
-V_{DC} /2	OFF	ON	OFF	ON	OFF	ON
	ON	OFF	ON	OFF	OFF	ON
-V_{DC}	ON	OFF	OFF	ON	OFF	ON

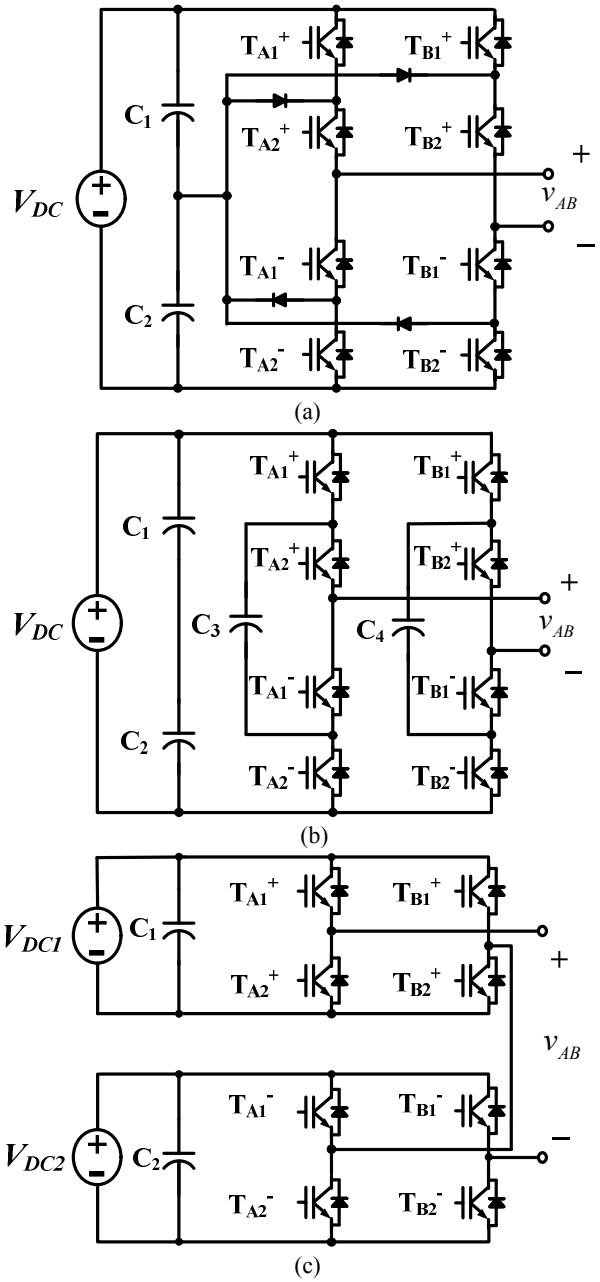


Fig. 1. Topologies of MLC: (a) Neutral point clamped type. (b) Flying capacitor type. (c) Cascaded type.

TABLE II
OPERATING MODES OF THE PROPOSED MLC

Operating mode	Reference voltage range	Output voltage
Mode 1	$V_c \le v_{ref} < 2V_c$	$V_{DC}/2$ or V_{DC}
Mode 2	$0 \le v_{ref} < V_c$	0 or $V_{DC}/2$
Mode 3	$-V_c \le v_{ref} < 0$	$-V_{DC}/2$ or 0
Mode 4	$-2V_c \le v_{ref} < -V_c$	$-V_{DC}$ or $-V_{DC}/2$

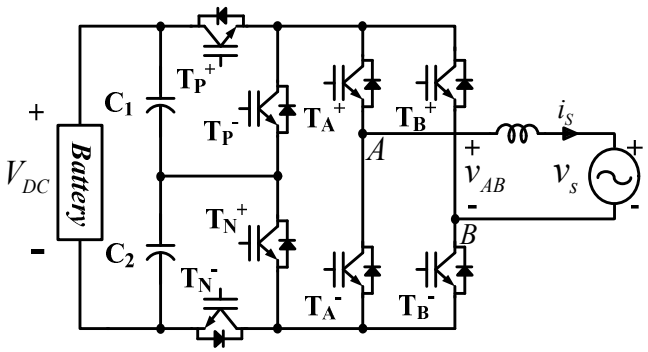


Fig. 2. Proposed grid-connected bi-directional multi-level converter for application to the energy storage system.

II. OPERATING PRINCIPLE OF THE PROPOSED MULTI-LEVEL CONVERTER

A. Topology of Multi-Level Converter

The proposed MLC is composed of two DC-link capacitors (C_1, C_2) and four switching devices (T_A^+, T_A^-, T_B^+, T_B^-) for the H-bridge, as well as four active switches (T_P^+, T_P^-, T_N^+, T_N^-) located between the DC-link and the H-bridge, as shown in Fig. 2. The voltage across the switching devices in the DC-link is $V_{DC}/2$. These devices are switched at switching frequency. Meanwhile, the voltage across the switching devices in the H-bridge is V_{DC}. These devices are switched at a frequency of the fundamental component of the output voltage (e.g., 50 or 60 Hz).

Thus, the switches in the DC-link and the H-bridge can be strategically selected based on the rated power of the converter system to reduce system cost and increase efficiency. Table I shows the output voltage according to the switching states.

B. Operating Modes and the Proposed PWM Strategy

The output voltage of the proposed MLC shown in Fig. 2 consists of five levels (V_{DC}, $V_{DC}/2$, 0, $-V_{DC}/2$, and $-V_{DC}$) based on the switching states of the converter. The four operating modes depend on the instantaneous value of the reference voltage and the maximum value of the carrier signal. Table II shows the possible converter output voltage levels according to the operating modes.

For the N-level NPC type multi-level converter, (N-1)

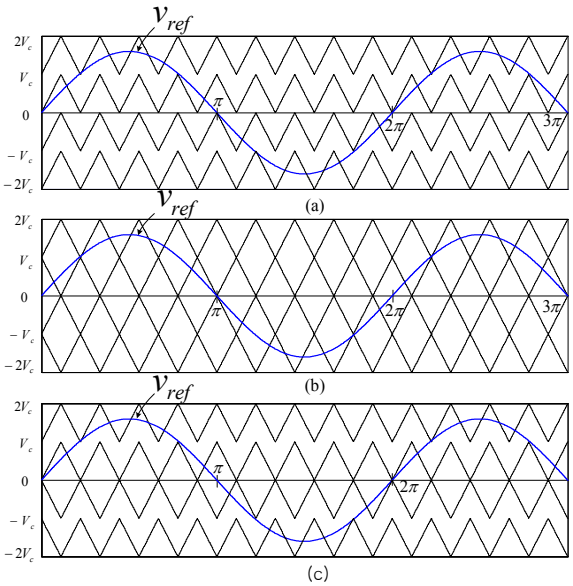


Fig. 3. Carrier and reference signal arrangements for: (a) Phase disposition (PD). (b) Alternative phase opposition disposition (APOD). (c) Phase opposition disposition (POD).

triangular carrier signals with the same frequency and amplitude are used to occupy contiguous bands that range from $+V_{DC}$ to $-V_{DC}$. A single sinusoidal reference signal is compared with each carrier signal to determine the output voltage for the converter. Three dispositions of the carrier signal are considered in generating the PWM signal [11]-[13].

1) Phase disposition (PD), in which all carriers are in a phase;
2) Alternative phase opposition disposition (APOD), in which each carrier is phase shifted by 180° from its adjacent carrier; and
3) Phase opposition disposition (POD), in which the carriers above zero voltage are 180° out of phase with those below a zero voltage.

Fig. 3 shows the reference and carrier signal arrangements for PD, APOD, and POD modulations.

A new PWM strategy based on POD modulation that requires only one carrier signal ($v_{carrier}$) is proposed. The detailed PWM strategy is depicted in Fig. 4. If the reference signal is positive, then the switch pair (T_A^+, T_B^-) is turned on; otherwise, the switch pair (T_A^-, T_B^+) is turned on. Thus, the switches comprising the H-bridge converter are turned on and off once during the reference signal period. The voltage across the switch in the H-bridge at the blocking state is V_{DC}. The switches (T_P^-, T_N^+) are operated complementarily to the switches (T_P^+, T_N^-).

The generation of the PWM signal for the DC link switches can be explained as follows:

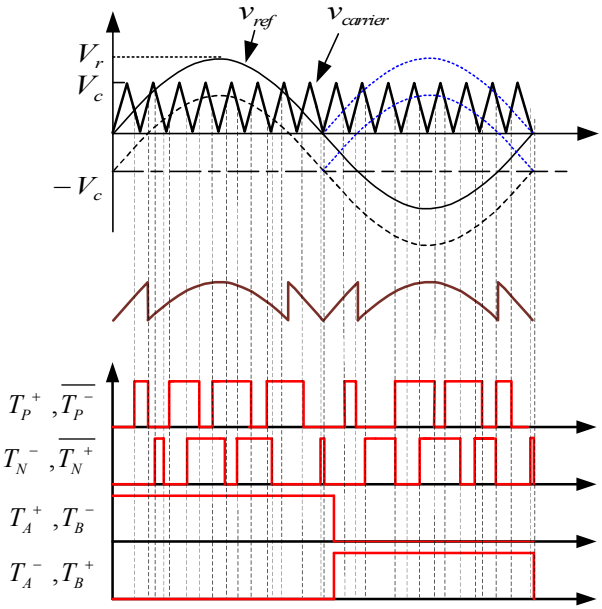


Fig. 4. PWM strategy based on a POD with a single carrier signal.

Mode 1: a signal subtracted from the reference signal by V_c is compared with the carrier signal. If (v_{ref}-V_c)> $v_{carrier}$, then T_P^+ and T_N^- are turned on. If (v_{ref}-V_c)< $v_{carrier}$, then the switch T_P^+ or T_N^- is alternately turned off.

Mode 2: the reference signal is directly compared with a carrier signal. If v_{ref} > $v_{carrier}$, then the switch T_P^+ or T_N^- is alternately turned on. If v_{ref}< $v_{carrier}$, then the switches T_P^+ and T_N^- are turned off.

Mode 3: -v_{ref} is directly compared with a carrier signal. If -v_{ref} > $v_{carrier}$, then the switch T_P^+ or T_N^- is alternately turned on. If -v_{ref}< $v_{carrier}$, then the switches T_P^+ and T_N^- are turned off.

Mode 4: a signal subtracted from -v_{ref} by V_c is compared with the carrier signal. If (-v_{ref}-V_c)> $v_{carrier}$, then the switches T_P^+ and T_N^- are turned on. If (-v_{ref}-V_c)< $v_{carrier}$, then the switch T_P^+ or T_N^- is alternately turned off.

The proposed PWM method is simple because only one carrier signal is used to generate four PWM signals.

C. Voltage Balancing of the DC-Link Capacitor

One of the important issues on MLC is the voltage balance of the DC-link capacitor [14], [15]. The voltage across capacitors C_1 and C_2 should be equally balanced to $V_{DC}/2$. However, the midpoint voltage fluctuates when C_1 and C_2 continuously charge and discharge. If the capacitor voltage is unbalanced, the output voltage becomes asymmetrical, resulting in a high harmonic content in the grid current.

To solve this problem, the switching state should be selected appropriately, as shown in Fig. 5. If only one switch in the DC-link is turned on, the output voltage becomes $V_{DC}/2$. The DC-link switches (T_P^+, T_N^-) are alternately turned

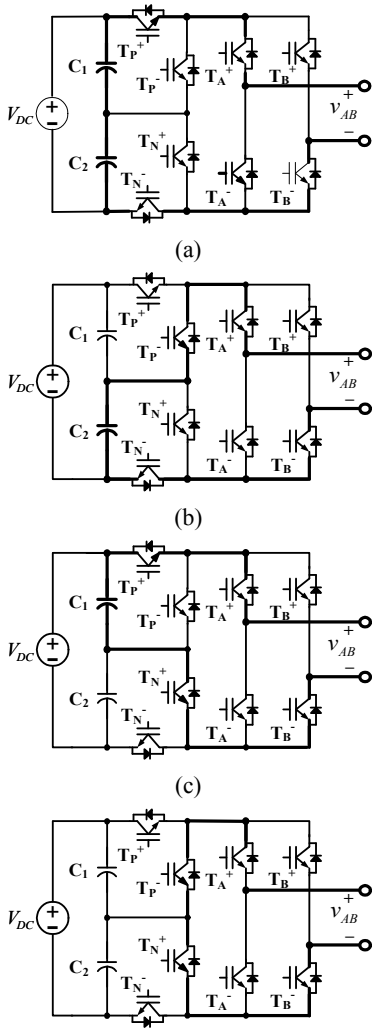


Fig. 5 Switching states of the proposed converter in a positive half cycle: (a) state 1 : $v_{AB} = V_{DC}$. (b) state 2 : $v_{AB} = V_{DC}/2$. (c) state 3 : $v_{AB} = V_{DC}/2$. (d) state 4 : $v_{AB} = 0$.

on at mode 2 and alternately turned off at mode 1 to balance the DC-link capacitor voltage. The switches (T_P^-, T_N^+) are operated complementarily to the switches (T_P^+, T_N^-). Therefore, the switching sequences of modes 1 and 2 are (a)-(b)-(a)-(c) and (b)-(d)-(c)-(d), respectively. The switching sequences of modes 3 and 4 are similar to those of modes 1 and 2.

D. Control Strategy

Fig. 6 shows the block diagram of the current control. A proportional-resonant (PR) controller with a stationary frame is used for the current controller. If the DC-link voltage is controlled by a proportional-integral controller, the voltage controller output can be treated as the active power reference. Thus, if the reactive power reference is given, then the grid current reference can be calculated as follows:

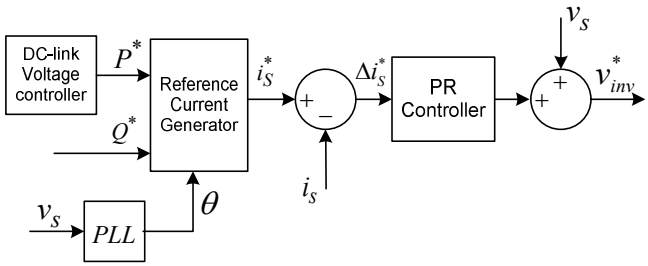


Fig. 6. Block diagram of current control.

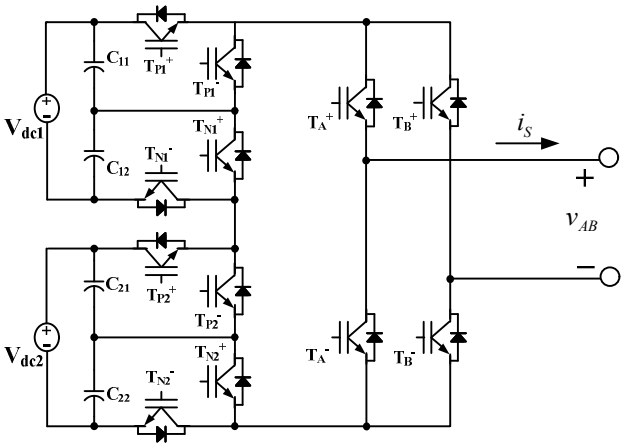


Fig. 7. Proposed 9-level converter topology.

$$v_S = \sqrt{2} V_S \sin\theta \tag{1}$$

$$i_S{}^* = \sqrt{2} I_S{}^* \sin(\theta - \phi^*) \tag{2}$$

, where $I_S{}^* = P^* / (V_S \cos\phi^*)$, $\phi^* = \tan^{-1}(Q^* / P^*)$.

The PR controller is a good candidate for reference tracking in a stationary frame because the grid current, which is the control object of the current controller, is a fixed frequency AC (50 or 60 Hz). No steady state error is required and transforming the axes is unnecessary because the gain of the PR controller at a selected resonant frequency is infinite [16], [17].

E. Extensions for the Nine-Level and Three-Phase Five-Level Converters

Notably, although the number of the switching devices in the proposed five-level converter is the same as that of the conventional cascaded H-bridge MLC, the switches in the H-bridge of the proposed MLC are switched at a low frequency (60 Hz). Moreover, unlike the cascaded H-bridge MLC, the proposed five-level inverter requires only one isolated voltage source, V_{DC}.

A nine-level converter, which is extended from the five-level converter shown in Fig. 2, is proposed in this paper to maximize the effectiveness of the proposed MLC. The overall circuit diagram is shown in Fig. 7. As shown in Fig. 7,

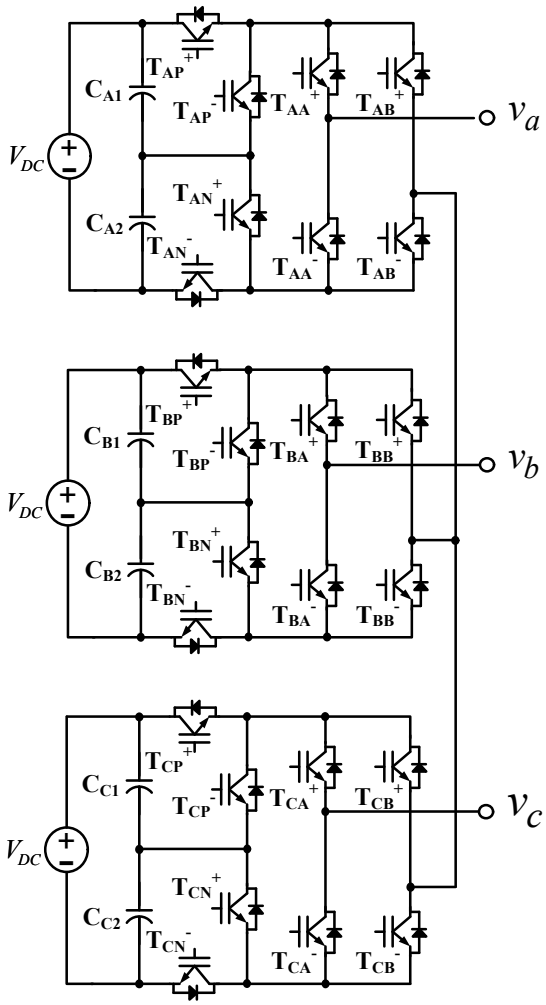


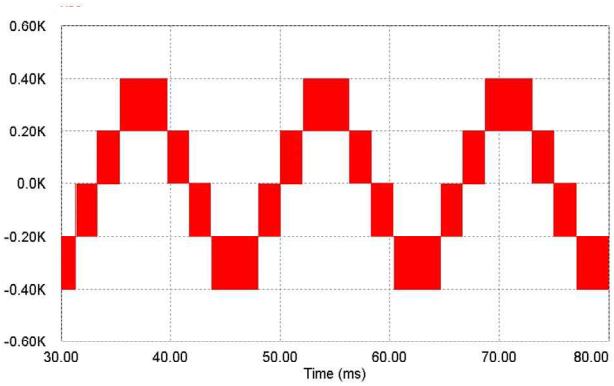
Fig. 8. Proposed three-phase five-level converter topology.

the proposed converter requires 12 active devices for the nine-level converter, but 16 active devices are required for the cascaded H-bridge MLC. Therefore, the number of switching devices in the proposed MLC can be reduced significantly as the number of voltage level increases.

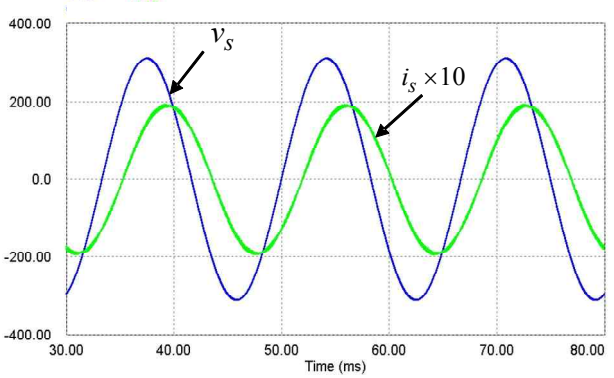
A unit cell can be produced as a module and the extension of the output voltage level is achieved simply by connecting the modules in a series. The construction of the three-phase multi-level converter is also possible.

III. Simulation Results

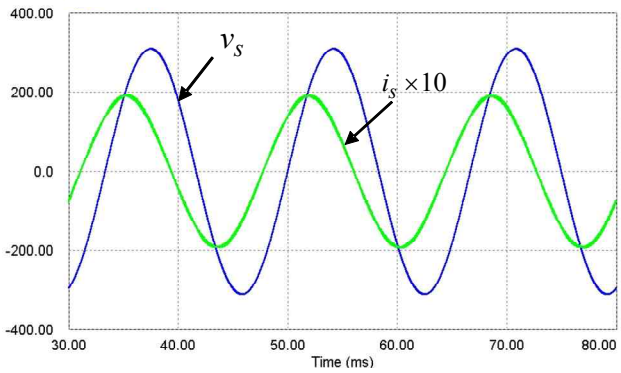
The proposed 3 kVA, five-level converter is simulated to verify the operating principle. The L filter is inserted between the output of the converter and the grid. The electrical specification of the proposed converter is summarized in Table III. Fig. 9 shows the waveforms of the proposed five-level converter. The grid current is satisfactorily controlled in the discharging [Figs. 9(b) to 9(d)] and charging modes [Fig. 9(e)], and the power factor can also be controlled.



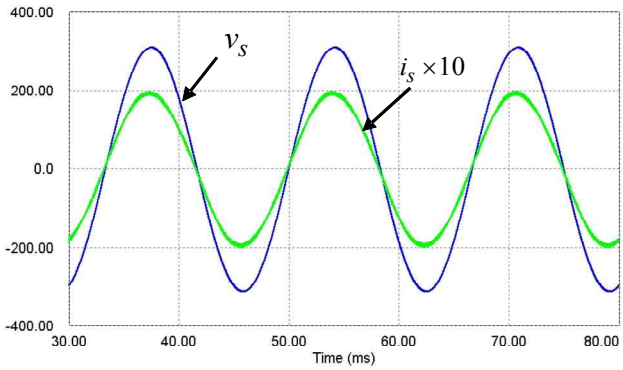
(a) Output voltage.



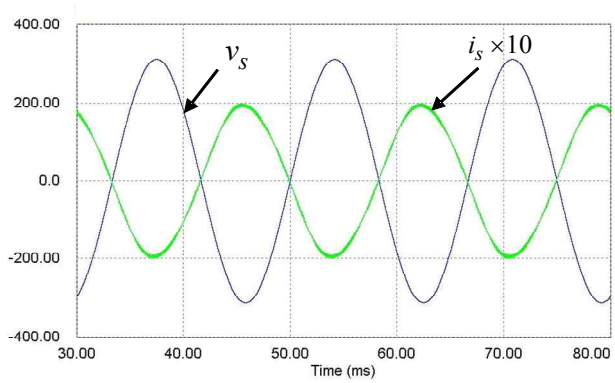
(b) Grid injected current and grid voltage at discharging mode; lagging power factor.



(c) Grid injected current and grid voltage at discharging mode; leading power factor.



(d) Grid injected current and grid voltage at discharging mode; unity power factor.



(e) Grid injected current and grid voltage at charging mode.

Fig. 9. Waveforms of the 5-level converter.

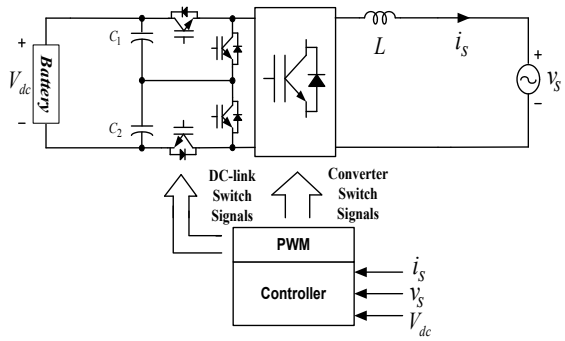


Fig. 10. Grid-connected multi-level converter system.

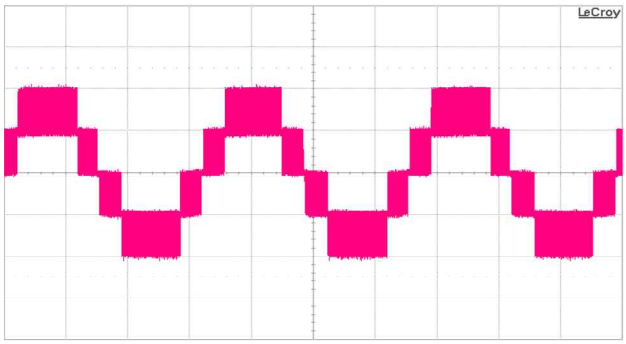
TABLE III
ELECTRICAL SPECIFICATION OF THE PROPOSED SINGLE-PHASE FIVE-LEVEL CONVERTER

DC-link voltage	400 V	Line voltage	220 V_{rms}
DC-link capacitor	2200 uF	Output frequency	60 Hz
Filter inductor	1 mH	Switching frequency	10 kHz
Switching device	SKM75GB128D		

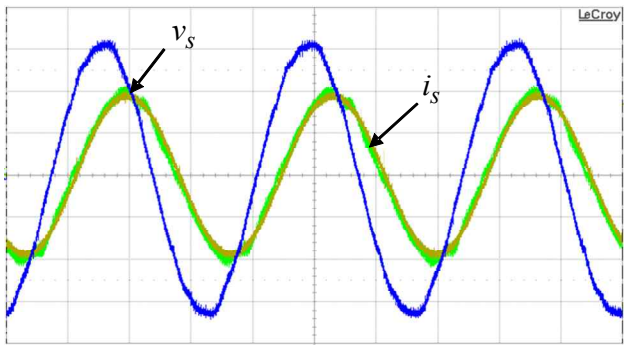
IV. EXPERIMENTAL RESULTS

Fig. 10 shows the grid connected multi-level converter system with the same conditions as the simulation. The voltage at the Point of Common Coupling (PCC) and the current injected to the PCC are measured. The DC link voltage is also sensed. DSP TMS320F2812 is used to implement the current controller and the voltage controller, to obtain the grid voltage phase, and to generate the PWM signals.

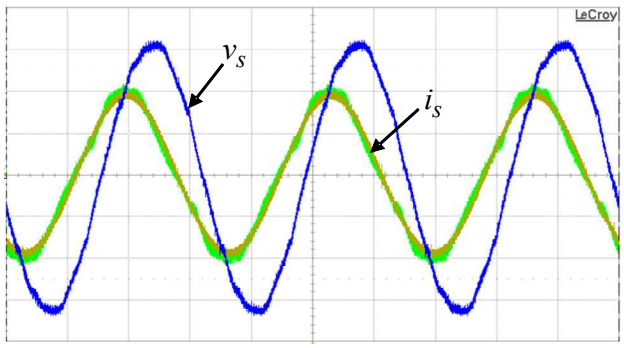
Fig. 11 shows the output waveforms of the proposed converter. With a five-level output voltage, the grid current is satisfactorily controlled during the discharging and charging modes. Only the waveform at unity power factor is shown for the charging mode because the power factor control function is necessary only for the discharging mode. The THD of the output current is 3.8 %.



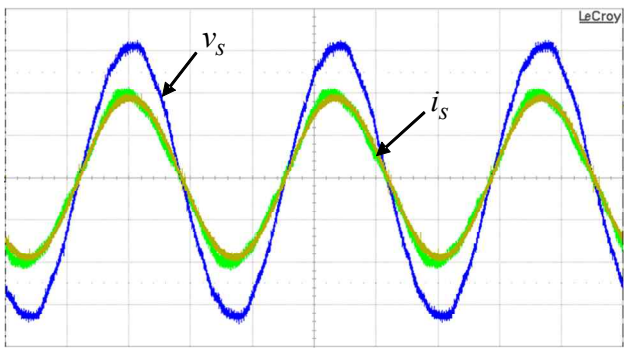
(a) Output voltage (200 V/div). Time: 5ms/div.



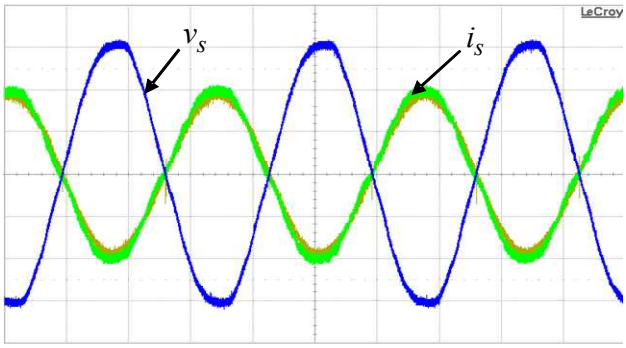
(b) Grid injected current (5 A/div) and grid voltage (100 V/div) at discharging mode; lagging power factor. Time: 5ms/div.



(c) Grid injected current (5 A/div) and grid voltage (100 V/div) at discharging mode; leading power factor. Time: 5ms/div.



(d) Grid injected current (5 A/div) and grid voltage (100 V/div) at discharging mode; unity power factor. Time: 5ms/div.



(e) Grid injected current (5 A/div) and grid voltage (100 V/div) at charging mode. Time: 5ms/div.

Fig. 11. Experimental waveforms of the proposed converter.

V. CONCLUSIONS

This paper proposed a new multi-level converter topology based on an H-bridge converter with four switches connected to the DC-link.

The power semiconductor switching devices that configure the H-bridge circuit in the proposed multi-level converter are only responsible for the polarity reversal of the AC output voltage, and the five-level output voltages are generated by the appropriate switching of the DC-link switches. The switching devices in the H-bridge converter are synchronized according to the output voltage signal. Therefore, switching loss is smaller than that of the other converter.

The configuration of the control circuit is simple because the PWM signal is generated by using only one carrier signal. The number of the switching devices in the proposed MLC is fewer than that in the conventional multi-level converter. Thus, the reliability of the proposed system is high, and the cost of the system can be low.

A unit cell can be produced as a module, and extending output voltage level is achieved simply by connecting the module in a series. The construction of the three-phase multi-level converter is also possible.

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