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Selective Harmonic Elimination for a Single-Phase 13-level TCHB Based Cascaded Multilevel Inverter Using FPGA

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Abstract

This paper presents an implementation of selective harmonic elimination (SHE) modulation for a single-phase 13-level transistor-clamped H-bridge (TCHB) based cascaded multilevel inverter. To determine the optimum switching angle of the SHE equations, the Newton-Raphson method is used in solving the transcendental equation describing the fundamental and harmonic components. The proposed SHE scheme used the relationship between the angles and a sinusoidal reference waveform based on voltage-angle equal criteria. The proposed SHE scheme is evaluated through simulation and experimental results. The digital modulator based-SHE scheme using a field-programmable gate array (FPGA) is described and has been implemented on an Altera DE2 board. The proposed SHE is efficient in eliminating the 3rd, 5th, 7th, 9th and 11th order harmonics, which validates the analytical results. From the results, it can be seen that the adopted 13-level inverter produces a higher quality with a better harmonic profile and sinusoidal shape of the stepped output waveform.

Key words: Field-programmable gate array (FPGA), Multilevel inverter, Pulse-width modulation, Total harmonic distortion (THD)

I. INTRODUCTION

Multilevel inverter technology has drawn tremendous interest among researchers from industry and academia in recent years due to its superior performance. In contrast to conventional two-level inverters, they are more efficient and better suited for applications requiring high power and high voltage levels. Among the various types of multilevel inverter topologies, the cascaded H-bridge (CHB) has attracted special attention due to its modular structure, which provides high reliability and better fault tolerance. Increasing the number of levels is also easier with minimal modifications in the hardware and control algorithm. Therefore, the CHB multilevel inverter has become popular in renewable energy (solar/wind power inverters), reactive power compensation (STATCOMs) and motor-drive applications up to MegaWatt (MW) power levels [1]-[6]. For these applications, the converter's output voltage must fulfill the requirement for maximum voltage and current THD as specified in IEEE Std.519-1992 [7].

It is essential to produce an effective power converter from the perspective of cost, efficiency and output quality. These factors have leads for developing a new family of multilevel inverters known as transistor-clamped converters (TCC) [5], [8]. By adding additional devices (such as power switches, power diodes and capacitors) to an existing H-bridge topology, it is possible to increase the number of output voltage levels and produce a better sinusoidal output waveform. The TCC has a reduced number of dc power supplies and switches when compared to the conventional CHB topology designed for the same number of voltage levels.

The modulation strategy has a profound impact on the performance of multilevel inverters, since it determines the switching losses as well as the voltage and current harmonics. Generally, multilevel modulation strategies can be classified, according to the switching frequency, into two categories: high-frequency switching and low-frequency (fundamental frequency) switching methods. The most popular modulation

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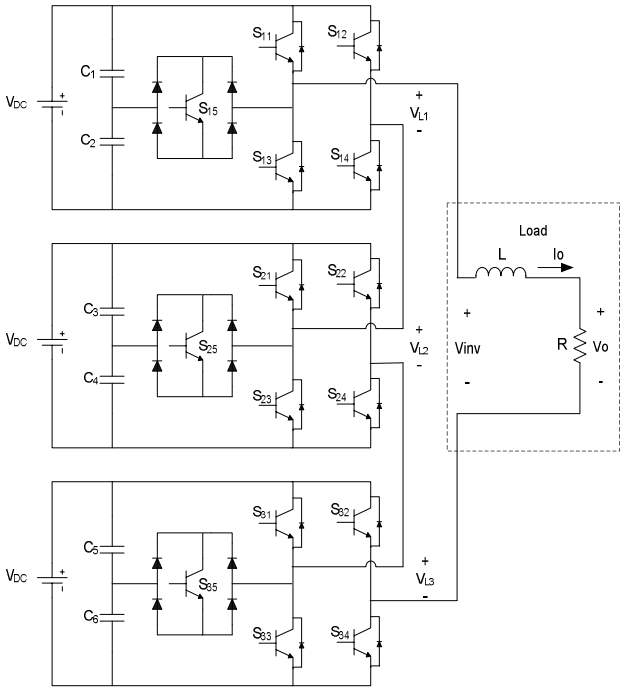


Fig. 1. The 13-level TCHB based cascaded multilevel inverter topology.

schemes discussed in the literature for multilevel inverters are multireference/multicarrier-based PWM [4], [5], [9], [10], multilevel space-vector PWM (SVM) [11], [12] and multilevel selective harmonic elimination (SHE) [7], [13]. The multilevel carrier-based PWM and SVM techniques are considered high-switching frequency schemes, whereas SHE falls within the low-switching frequency group. Each solution has its unique advantages and drawbacks. As a result, the choice of the modulation technique usually depends on the inverter topology and its application.

Among the many modulation strategies, SHE is commonly adopted in high power applications where the switching frequency has to be low enough to minimize the switching losses. Since the effectiveness of the SHE method depends heavily on the switching angle, various algorithms have been developed for determining the optimum switching angles [14], [15]. Usually, this is done offline, using optimization techniques such as the Newton-Raphson (NR) method [14]-[17]. More complex techniques such as the genetic algorithm (GA) [15], [18]-[20] and the particle swarm optimization (PSO) [15], [21], [22] have also been demonstrated. Although these new techniques are fast in determining the optimized angle, the solutions only minimize the harmonics rather than eliminate them. Moreover, as a prerequisite, the engineers need to understand advance control and mathematics algorithms [6].

More recently, online methods have been proposed where the real-time calculations of the switching angles are made possible using a high speed processor. In [23], a mathematical calculation based on a trigonometric function was proposed to obtain the switching angles. In [24], a simple and improved real-time algorithm for calculating the switching angles has been introduced and then proven by mathematical derivation. In [6], the authors proposed a four-equation method based on harmonic injection and equal area criteria, regardless of the number of inverter output levels. In [3], an artificial neural network (ANN) was used for obtaining the optimal switching angles for multilevel inverters in solar applications. However, due to the simplifications used, these online methods cannot fully eliminate the harmonics. Hence, they generally yield a significantly higher THD and are inferior to the offline methods.

SHE analyses for 5-level to 13-level CHB inverters with an unequal dc sources considering the minimum THD with or without elimination of the lowest order harmonics are discussed in [25]. However, the real implementation results are discontinued for 11-level and 13-level cases. For the 13-level case, only simulation studies have been reported so far [26]. In this paper, real implementation of the SHE method on a 13-level inverter is demonstrated.

Normally, digital implementation of SHE modulation involves two steps. First, the switching angles are calculated offline through solving a set of non-linear and transcendental equations. Then, the switching angles are stored in a look-up table (LUT) for real-time application [27].

In order to implement real-time control systems in power electronics applications, the system designers have many choices. Microcontrollers, microprocessors and DSPs are software-based devices, which come with efficient software compilers and programs usually written in C or assembly language. Although these technologies are matured and usually have dedicated PWM generation blocks, they have limited sampling rates and limited speed due to their natural sequence based operation (the programs are executed line by line, not simultaneously). This limitation can be resolved with a field-programmable gate array (FPGA) as an alternative to programmable logic device (PLD) and application specific integrated circuit (ASIC) technologies. FPGAs are digital hardware-based devices and they have become an increasingly popular technology in digital prototyping for multilevel inverters [15], [28] due to their speed and flexibility.

In this paper, SHE modulation is suggested for a 13-level transistor-clamped H-bridge (TCHB) inverter based cascaded multilevel inverter topology. The Newton-Raphson method is used to calculate switching angles with the capability to eliminate the lowest order harmonics while maintaining the fundamental component. In order to generate an optimum stepped output waveform, a simple SHE modulation is defined according the voltage-angle equal criteria. Real implementation of SHE modulation for a TCHB inverter using an FPGA is presented. The analytical results are validated through both simulation and experimental results.

TABLE I
SWITCHING STATES AND VOLTAGE LEVELS OF THE 13-LEVEL TCHB INVERTER

States	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{21}	S_{22}	S_{23}	S_{24}	S_{25}	S_{31}	S_{32}	S_{33}	S_{34}	S_{35}	V_{inv}
1	1	0	0	1	0	1	0	0	1	0	1	0	0	1	0	3 V_{DC}
2	1	0	0	1	0	1	0	0	1	0	0	0	0	1	1	2½ V_{DC}
3	1	0	0	1	0	0	0	0	1	1	0	0	0	1	1	2 V_{DC}
4	0	0	0	1	1	0	0	0	1	1	0	0	0	1	1	1½ V_{DC}
5	0	0	0	1	1	0	0	0	1	1	0	0	1	1	0	V_{DC}
6	0	0	0	1	1	0	0	1	1	0	0	0	1	1	0	½ V_{DC}
7	0	0	1	1	0	0	0	1	1	0	0	0	1	1	0	0
8	1	1	0	0	0	1	1	0	0	0	1	1	0	0	0	0
9	0	1	0	0	1	1	1	0	0	0	1	1	0	0	0	-½ V_{DC}
10	0	1	0	0	1	0	1	0	0	1	1	1	0	0	0	- V_{DC}
11	0	1	0	0	1	0	1	0	0	1	0	1	0	0	1	-1½ V_{DC}
12	0	1	1	0	0	0	1	0	0	1	0	1	0	0	1	-2 V_{DC}
13	0	1	1	0	0	0	1	1	0	0	0	1	0	0	1	-2 ½ V_{DC}
14	0	1	1	0	0	0	1	1	0	0	0	1	1	0	0	-3 V_{DC}

II. THE POWER CIRCUIT

Fig. 1 shows the studied inverter configuration based on a 5-level transistor-clamped H-bridge (TCHB) multilevel inverter. The 5-level TCHB is modified by adding one bidirectional switch to the H-bridge module. A very attractive feature of the bidirectional switch is that it allows for a bidirectional current flow and enables five output voltage levels of 0, $\pm\frac{1}{2}V_{DC}$ and $\pm V_{DC}$. Even though such a topology has been discussed in [9], the SHE modulation method is used instead of the multicarrier modulation method.

The inverter is supplied by three independent dc sources, three H-bridge modules and three bidirectional switches to produce a 13-level output. Multiple dc sources at the input of the inverter may be obtained from constant dc supplies, batteries, super capacitors, photovoltaics or fuel cells. Generally, the number of output levels for the inverter is given by $4i + 1$, where i is the number of TCHB cells.

Through combinations of the on state of the switches (S_{i1}-S_{i5}), the cell output voltage V_i can be expressed as:

$$V_i = V_{DC}(S_{i4} - S_{i2})\left\{\frac{1}{2}S_{i5} + \left|S_{i1} - S_{i2}\right| \cdot \left|S_{i3} - S_{i4}\right|\right\} \quad (1)$$

The modes of operation, the switches to be turned on and the corresponding output voltage levels are summarized in Table I. The 13-level TCHB inverter's operation involves 14 switching states, and all the operating states are illustrated in Fig. 2.

In order to justify the use of a TCHB inverter, performance comparisons are made against a conventional CHB inverter with the same 13-level voltage outputs. In general, the output voltage quality for both inverters is the same. The most obvious advantage of the adopted inverter is that it has a lower component count when compared to a CHB inverter with the same number of output levels. This results in lower total power losses produced by the TCHB inverter when compared to the CHB inverter [5]. Since the CHB inverter requires two series connected cells to produce 5 voltage levels, a total of 24 switches are needed to generate a 13-level voltage. On the other hand, the TCHB inverter requires only 15 switches to produce the same number of voltage levels. Moreover, the provision of isolated sources is the main disadvantage of the CHB topology. In this case, a total of six isolated dc sources is needed for the CHB, whereas the TCHB inverter requires three isolated dc sources. Owing to a bidirectional switch connected at the midpoint of the dc link to the TCHB inverter output, both of the topologies require six capacitors. However, a larger capacitance is required in the TCHB inverter to prevent a capacitor voltage imbalance [5], [9]. A few practical approaches for balancing capacitor voltages are by replacing the capacitors with isolated dc sources, applying a back-to-back intertie system [29] or the use of auxiliary dc-dc converter circuits [30]. It is expected that the overall cost of the TCHB inverter will be lower than that of the conventional CHB inverter due to the reduced switch count and the lower number of isolated dc sources required.

III. BACKGROUND AND SOLUTION FOR SHE MODULATION

A. Harmonic Elimination Technique

In general, the inverter output voltage V_{inv} waveform (see Fig. 3) can be expressed in the Fourier series as:

$$V_{inv}(\omega t) = a_0 + \sum_{n=1}^{\infty}\left[a_n \cos(n\omega t) + b_n \sin(n\omega t)\right] \quad (2)$$

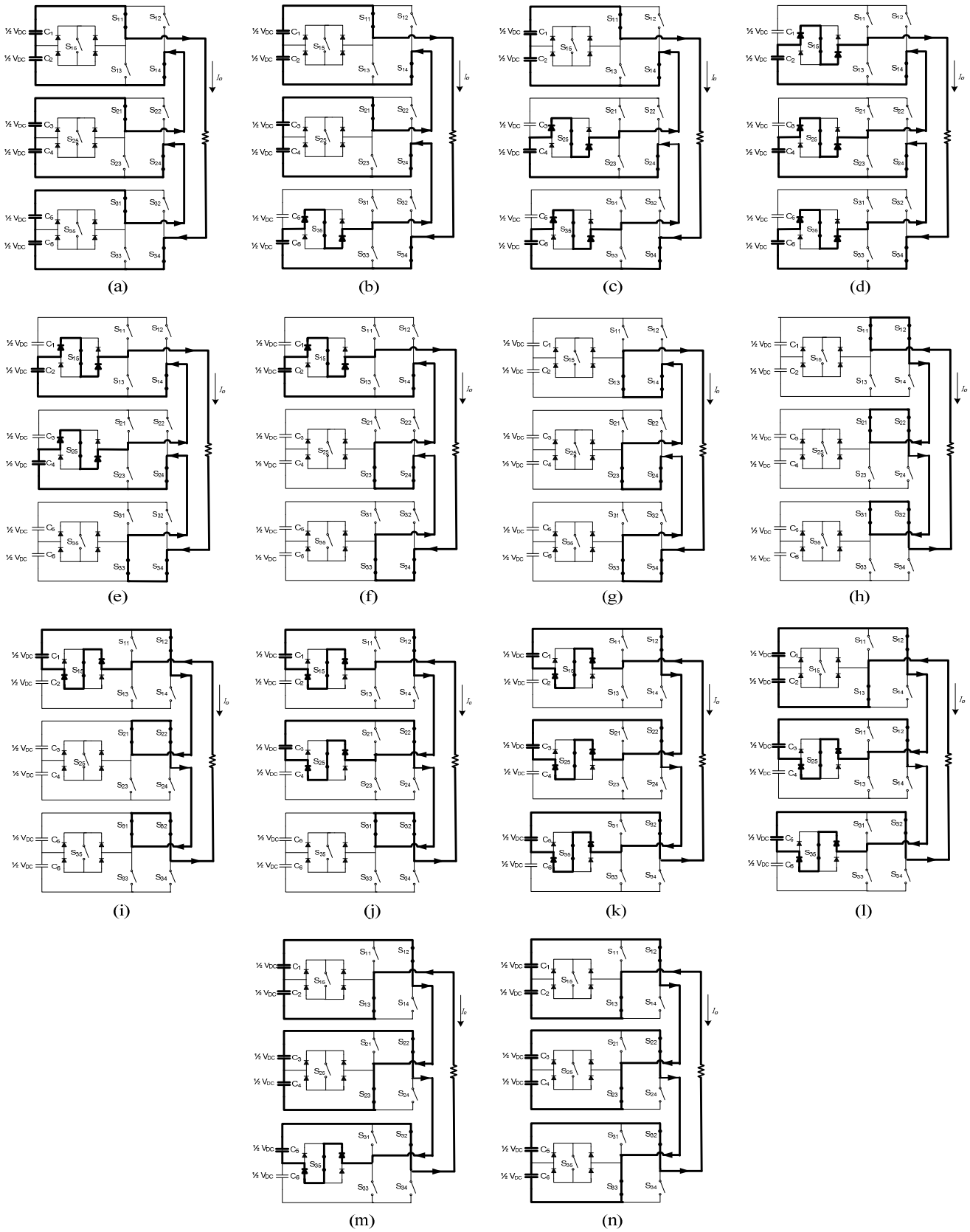


Fig. 2. Operating states of the 13-level TCHB inverter. (a) State 1. (b) State 2. (c) State 3. (d) State 4. (e) State 5. (f) State 6. (g) State 7. (h) State 8. (i) State 9. (j) State 10. (k) State 11. (l) State 12. (m) State 13. (n) State 14.

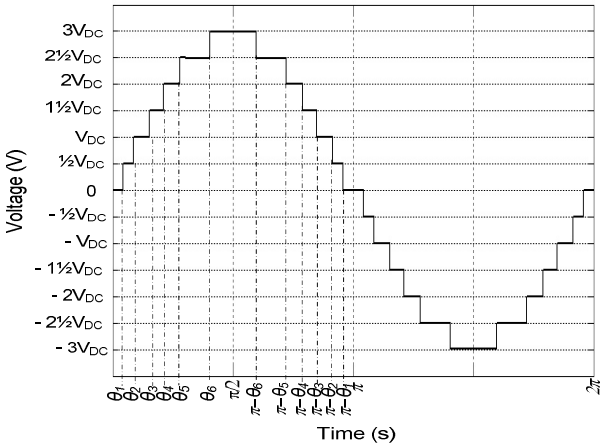


Fig. 3. The inverter output voltage V_{inv} waveform.

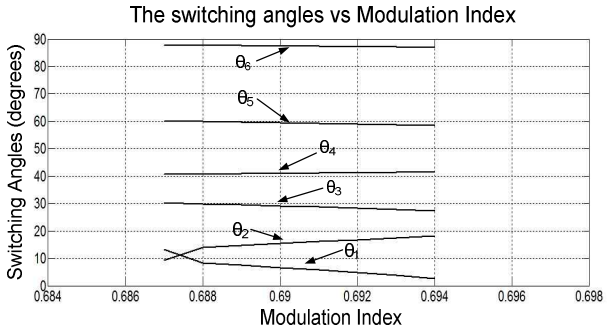


Fig. 4. The switching angles solutions for 13-level inverter.

It is worth noting that the actual waveform consists of sine terms only. The even harmonics are also absent due to the quarter-wave symmetry of the output voltage along the *x*-axis. Thus, both a_0 and a_n are zero, and (2) can be simplified into:

$$V_{inv}(\omega t) = \sum_{n=odd}^{\infty} b_n \sin(n\omega t) \tag{3}$$

Note that, when three TCHB cells are connected in cascade they provide a total output voltage V_{inv} as given by:

$$V_{inv} = V_{L1} + V_{L2} + V_{L3} \tag{4}$$

For each 5-level TCHB module in the adopted inverter, the output waveform has a minimum step of $\frac{1}{2}V_{DC}$. Thus, the Fourier series expansion of the inverter output V_{inv} waveform as seen in Fig. 3 is [4]:

$$V_{inv}(\omega t) = \frac{2V_{DC}}{n\pi} \sum_{n=1,3,5..}^{\infty} [\cos(n\theta_1) + ... + \cos(n\theta_6)] \sin(n\omega t) \tag{5}$$

From (5), the fundamental output voltage V_1 can be expressed as:

$$b_1 = \frac{2V_{DC}}{\pi} [\cos(\theta_1) + \cos(\theta_2) + ... + \cos(\theta_6)] = V_1 \tag{6}$$

and as indicated in Fig. 3, the switching angles $\theta_1 - \theta_6$ must satisfy the following condition:

$$0 < \theta_1 < \theta_2 < ... < \theta_6 < \pi/2 \tag{7}$$

Assuming that the expression of the modulation index M is given by:

$$M = \frac{\pi V_1}{2sV_{DC}} (0 \le M \le 1) \tag{8}$$

where s is the number of positive steps in a quarter waveform.

The main objective of this paper is to produce an output waveform with the ability to eliminate the 3rd, 5th, 7th, 9th and 11th order harmonics. In order to generate a staircase waveform, the switching angles can be obtained by solving the following equations:

$$\begin{aligned}
\cos(\theta_1) + \cos(\theta_2) + ... + \cos(\theta_5) + \cos(\theta_6) &= 6M \\
\cos(3\theta_1) + \cos(3\theta_2) + ... + \cos(3\theta_5) + \cos(3\theta_6) &= 0 \\
\cos(5\theta_1) + \cos(5\theta_2) + ... + \cos(5\theta_5) + \cos(5\theta_6) &= 0 \\
\cos(7\theta_1) + \cos(7\theta_2) + ... + \cos(7\theta_5) + \cos(7\theta_6) &= 0 \\
\cos(9\theta_1) + \cos(9\theta_2) + ... + \cos(9\theta_5) + \cos(9\theta_6) &= 0 \\
\cos(11\theta_1) + \cos(11\theta_2) + ... + \cos(11\theta_5) + \cos(11\theta_6) &= 0
\end{aligned} \tag{9}$$

A different approach is used to solve the harmonic problem of the adopted inverter. There are three steps involved in this method. A brief description of the implementation steps are given as follows:

1) The switching angle calculations are performed through the Newton-Raphson (NR) method.
2) The voltage-angle equal criteria of the sinusoidal reference waveform is used to find the threshold voltage corresponding to the calculated angles.
3) A sinusoidal voltage reference is compared with the threshold voltages and combination logics are used to generate the gating signals.

B. Newton-Raphson Method

The Newton-Raphson (NR) method is a commonly used iterative method for solving equations which are difficult to solve analytically. Here, the NR method is used in Matlab to solve the set of transcendental equations in (8). The solutions, which are the set of switching angles for the 13-level inverter, are illustrated in Fig. 4. These switching angle are then examined for their corresponding total harmonic distortion (THD) given by:

$$THD_V = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \tag{10}$$

where V_n is the rms value of the nth harmonic component and V_1 is the rms value of the fundamental component.

IV. SHE Modulation and Its Implementation

The 13-level TCHB inverter topology is built with three isolated dc supplies. It is worth noting that there are a total of six equal steps ($\frac{1}{2}V_{DC}$, V_{DC}, $1\frac{1}{2}V_{DC}$, $2V_{DC}$, $2\frac{1}{2}V_{DC}$ and $3V_{DC}$) in a quarter of the output waveform as depicted in Fig. 3. Taking into account the instances where output voltage is zero, this gives a total of thirteen steps in the output voltage waveform,

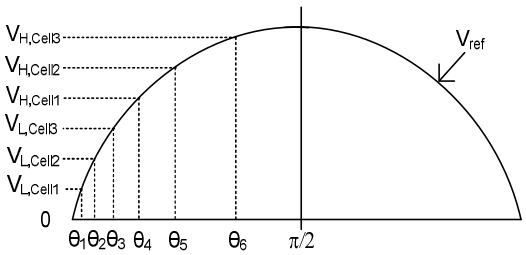


Fig. 5. The reference signal and triggered voltages for the respective angles.

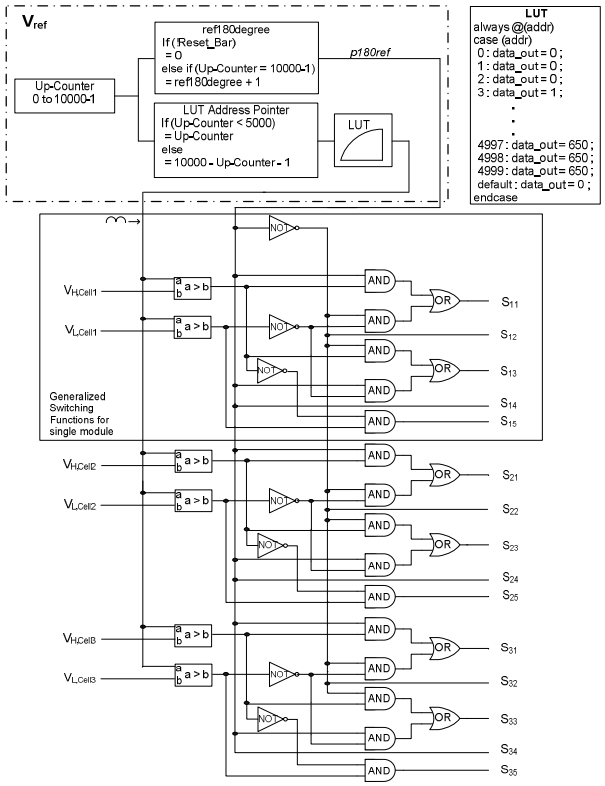


Fig. 6. Illustration of FPGA-based SHE modulator.

hence the name 13-level TCHB.

A. Proposed SHE Modulation

Fig. 5 illustrates the proposed SHE modulation for the 13-level TCHB inverter which is derived from one sinusoidal reference signal and several triggered voltage levels (V_H and V_L). Voltages V_H and V_L are classified as the triggered voltage levels; which correspond to the switching angles and switching states of the related cell.

According to Fig. 5, the reference voltage V_{ref} waveform is given by:

$$V_{ref} = V_m \sin \omega t \tag{11}$$

where V_m is an arbitrary (peak) value. For the developed SHE technique, only a half-wave diagram is illustrated and the modulus operation of a sinusoidal waveform has been included due to the fact that the steps in the other regions are sequential.

TABLE II

THE FPGA USAGE (ALTERA CYCLONE II - EP2C35F672C6)

Item	Utilization
Total logic elements	1 173 / 33 216 (4%)
Total combinational function	1 170 / 33 216 (4%)
Total register	53 / 33 216 (<1%)
Total pin	17 / 475 (4%)

TABLE III

THE SWITCHING ANGLES SET

Case	Switching Angles (°)
Minimum THD	[4.90 16.75 28.27 41.18 58.95 87.19]
Maximum THD	[9.30 13.20 30.20 40.60 60.10 87.80]

There are six voltage levels ($V_{L,Cell1}$, $V_{H,Cell1}$, $V_{L,Cell2}$, $V_{H,Cell2}$, $V_{L,Cell3}$, and $V_{H,Cell3}$) during the positive half-cycle of the modulating signal, where two voltage levels are specified for each cell. By using the voltage-angle equal criteria, a simple calculation for the triggered voltage levels is derived from the calculated switching angles ($\theta_1 - \theta_6$), which can be computed as:

$$\begin{aligned} V_{L,Cell1} &= \sin(\theta_1 \times \pi/180) \times V_m \\ V_{L,Cell2} &= \sin(\theta_2 \times \pi/180) \times V_m \\ V_{L,Cell3} &= \sin(\theta_3 \times \pi/180) \times V_m \\ V_{H,Cell1} &= \sin(\theta_4 \times \pi/180) \times V_m \\ V_{H,Cell2} &= \sin(\theta_5 \times \pi/180) \times V_m \\ V_{H,Cell3} &= \sin(\theta_6 \times \pi/180) \times V_m \end{aligned} \tag{12}$$

Equation (12) is a generalized set of trigger voltages corresponding to the switching angles in order to perform the SHE modulation for the adopted inverter. The sequence is chosen such that cell 1 turns on and off at angles θ_1 & θ_4, cell 2 at θ_2 & θ_5, and cell 3 at θ_3 & θ_6, respectively. This is to ensure that each cell has approximately the same turn on time, and to avoid over-burdening of any particular cell. This concept can be applied to any angle, number of voltage levels and type of multilevel inverter topology.

B. Hardware Implementation Using FPGA

Fig. 6 shows a block diagram of the SHE scheme implemented in an FPGA. The controller functional model was designed by means of Verilog HDL code and schematic design entries in Quartus II software. There are four sub-modules in the modulator architecture. One module is designated for the sine look-up table (LUT) for the reference V_{ref} signal and three logic modules are derived for the switches in each 5-level inverter cell.

In order to generate a sine reference waveform, only data for a quarter sine wave is needed. The sinusoidal reference generator of a 50 Hz signal is stored in the LUT with a 1 MHz

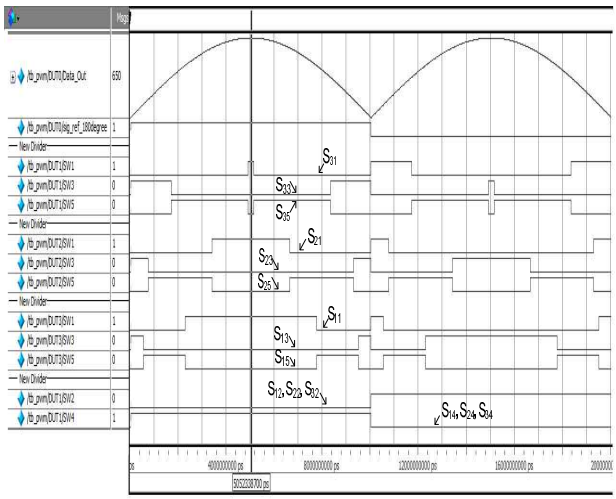


Fig. 7. Waveform of switching signals.

sampling frequency. This requires only 5,000 sample data to be stored in the LUT, reducing the utilization of the FPGA devices without compromising the performance of the controller. The sine-wave LUT (see Fig. 6) displayed data value of 650 used with Verilog code as the chosen peak reference throughout the simulations and hardware implementation. The 180° reference signal is generated based on the first 10,000 counter in logic low, and the next 10, 000 sequences in logic high. This will be continuously repeated.

The logic modules consist of the assigned voltage levels as representatives of the switching angles, comparators and combinational logics. The switching patterns of each cell in the 13-level inverter were then formed by logic combinations from the reference and the calculated threshold voltage comparisons. Switches S_{i1}, S_{i3}, and S_{i5} (i is the cell number) operate by comparing the reference signal with the triggered voltage levels and through the combinational logic gates, whereas S_{i2} and S_{i4} operate complementarily in a half cycle of the reference signal (i.e 50 Hz). Therefore, signals S_{12}, S_{22} and S_{32} have the same pattern, as well as the signals S_{14}, S_{24} and S_{34}.

The general logic expression (simple combinations of AND, OR and NOT logics) of the gating signals are given as follows:

$$\begin{aligned} S_{i1} &= (C_{i1} \,.\, p180ref) + (\overline{C_{i2}} \,.\, \overline{p180ref}) \\ S_{i2} &= \overline{p180ref} \\ S_{i3} &= (C_{i1} \,.\, \overline{p180\text{ref}}) + (\overline{C_{i2}} \,.\, p180ref) \\ S_{i4} &= p180ref \\ S_{i5} &= \overline{C_{i1}} \,.\, C_{i2} \end{aligned} \tag{13}$$

where C_{i1} and C_{i2} are the outputs of the comparators and the $p180ref$ signal is the 180° reference based on the 50 Hz pulse signal which is also identified as the S_{i4} signal. This control scheme can be extended to any numbers of 5-level TCHB modules.

In order to implement the modulator on an FPGA, a cost effective Altera DE2 development board has been chosen to generate the digital gating signal. A Cyclone II 2C35 FPGA device has been included with aid of various hardware resources and components incorporated on-board, including 33 216 logic elements (LE), 483 840 RAM bits, 35 embedded multipliers, and 475 user I/O pins. The FPGA utilizations for the proposed system are summarized in Table II.

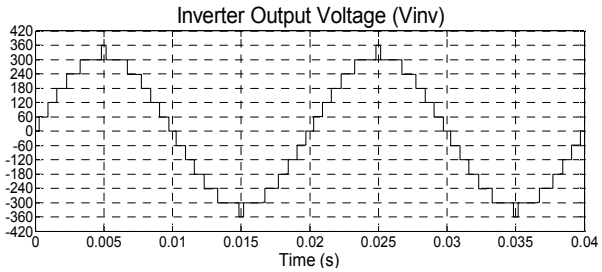


Fig. 8. The inverter output voltage V_{inv} using solution set with minimum THD.

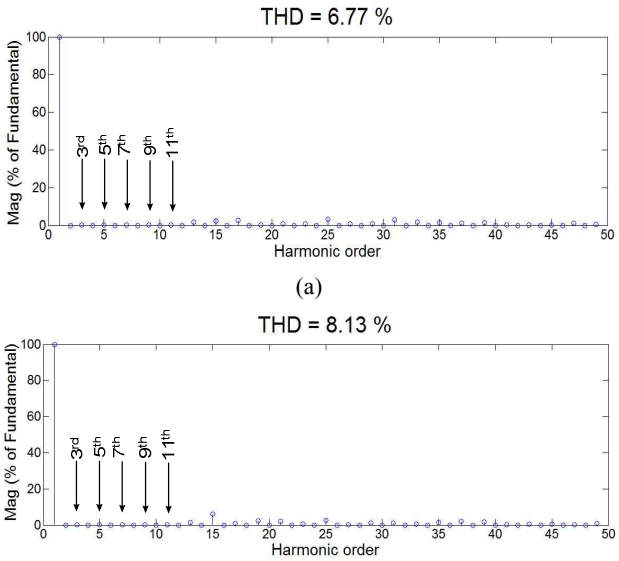


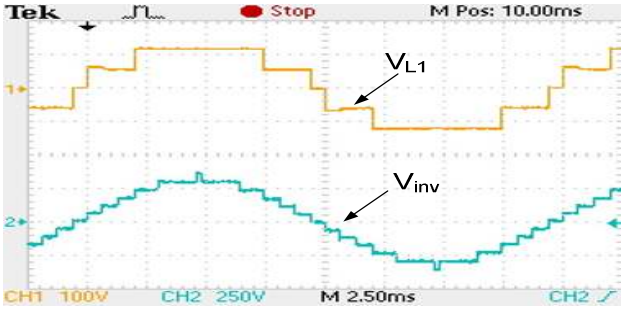
Fig. 9. Harmonic spectrum. (a) Solution set with minimum THD. (b) Solution set with maximum THD.

V. Simulation and Experimental Results

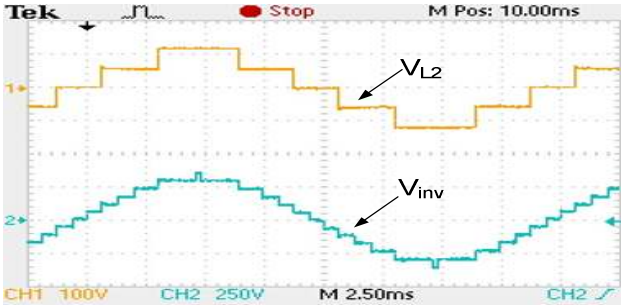
A. Simulation Results

For verification of the FPGA-based design, simulations are done on ModelSim software. Two sets of switching angles are used: one is a set of angles which yields the minimum THD. The other case uses a set of angles which yields the maximum THD. The used switching angles are presented in Table III. Fig. 7 shows the simulated gating signals of the minimum THD for the TCHB inverter switches in the ModelSim simulation environment. The highlighted line in Fig. 7 is the location of the peak sine wave at a duration of 0.005 second, which has been determined by (11) and the respective gating signals.

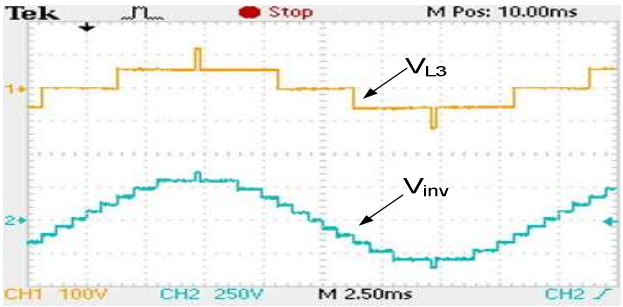
The THCB inverter is then simulated using Matlab/Simulink



(a)



(b)



(c)

Fig. 10. Experiment results with respect to 13-level output. (a) Output voltage V_{L1}. (b) Output voltage V_{L2}. (c) Output voltage V_{L3}.

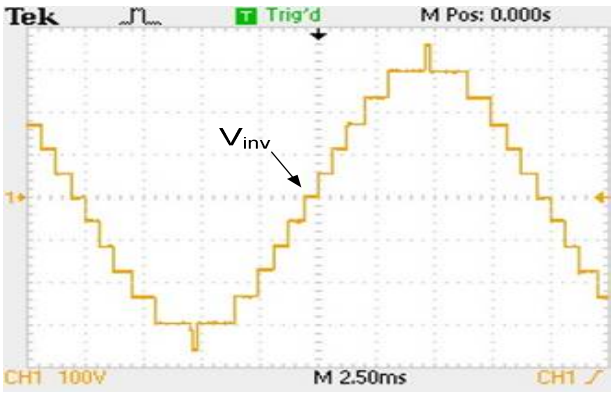
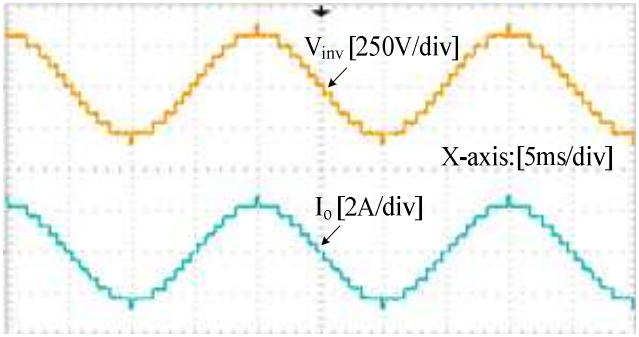
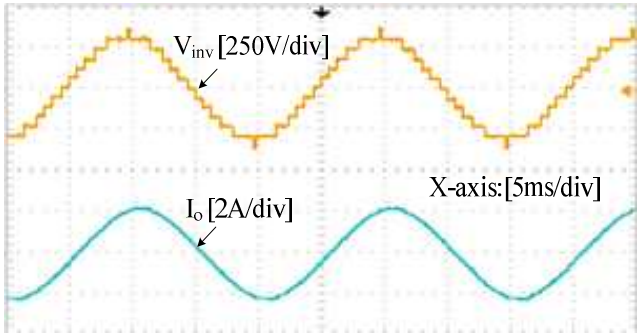


Fig. 11. Inverter output V_{inv} waveform for solution set with minimum THD.

in order to verify the SHE modulation. The total dc voltage input is set to 360 V, so that the dc-link for each 5-level TCHB inverter module is 120 V. Two types of loads are tested, i.e. a purely resistive load and an RL load. The former uses only a



(a)



(b)

Fig. 12. Experiment results for solution set with minimum THD. (a) The waveforms for R load. (b) The waveforms for RL load.

130 Ω resistor at the inverter output, while the later adds an 81 mH inductor in series with the resistor. These RL values are chosen to be the same as those in the experimental setup to facilitate the analysis and performance comparison between the simulation and experimental results.

Fig. 8 shows the simulated results of the inverter output voltage V_{inv} when the adopted inverter operates with the switching angles of the minimum THD. Fig. 9a shows the inverter output voltage THD of 6.77% for the minimum THD case. Meanwhile, Fig. 9b shows the inverter voltage THD of 8.13% for the maximum THD case. Both THD results show that the specific 3rd, 5th, 7th, 9th and 11th harmonic orders have been eliminated.

B. Experiment Results

A prototype inverter is built to verify the effectiveness of the proposed SHE scheme. The experimental setup has been constructed to be similar to the simulation setup and it operates using the same switching angles shown in Table III. Insulated gate bipolar transistors (IGBTs) with ultrafast soft recovery diodes (IRG4PC50UD) and power diodes (30CPF12PBF) are used in the prototype inverter. The inverter was supplied by three GW Instek (GPC6030D) isolated dc sources V_{DC}= 120 V for each of the cells. Six 3300 µF electrolyte capacitors are used as dc-link capacitors (C_1-C_6). The large capacitance is used to reduce the effects of voltage unbalance [5], so that the voltage across each capacitor is maintained at approximately

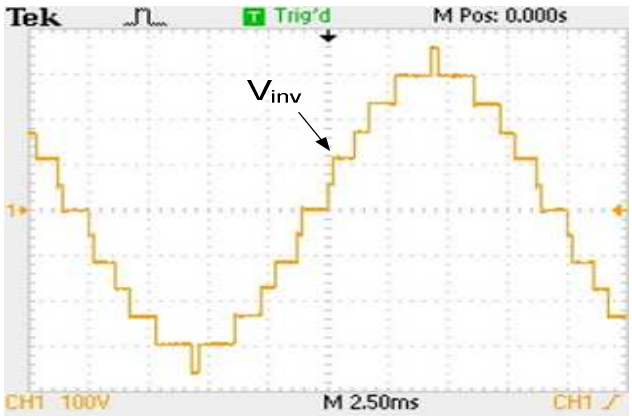
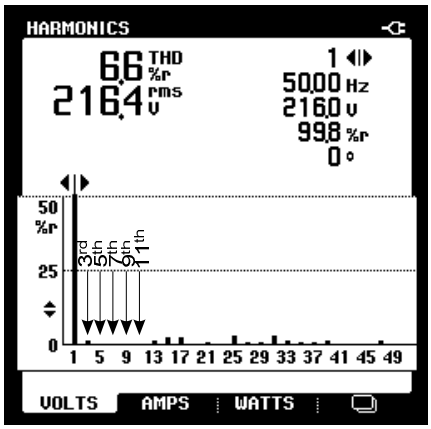
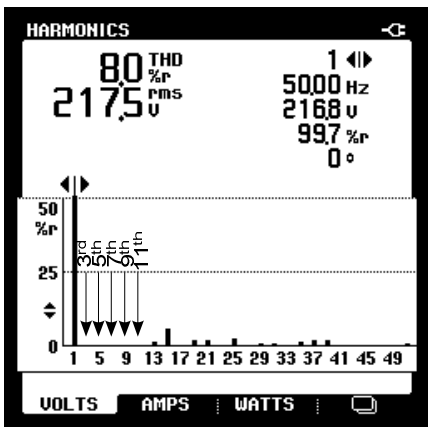


Fig. 13. Inverter output V_{inv} waveform for solution set with maximum THD.



(a)



(b)

Fig. 14. The harmonic spectrum. (a) For minimum THD. (b) For maximum THD.

½V_{DC} throughout the experiment. The prototype is tested under two load conditions as in the simulation: the resistive load case, R= 130 Ω, and the RL load case, R= 130 Ω and L= 81 mH.

Figs. 10-12 illustrate the waveform results of the adopted inverter in the test experiments using the solution angles set of the minimum THD. Figs. 10a-10c show the output voltage for module 1, module 2 and module 3 (V_{L1}, V_{L2}, V_{L3}) together with

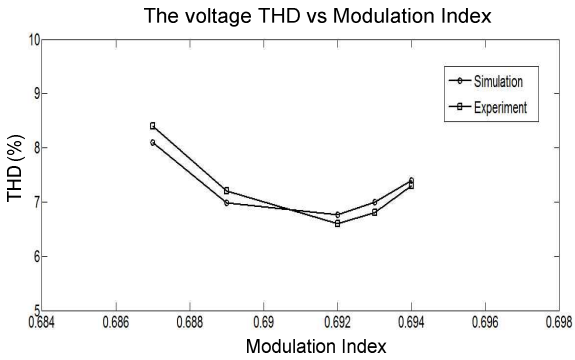


Fig. 15. Comparison of inverter output voltage THD between simulation and experiment.

the resultant output voltage V_{inv} of the 13-level inverter. Fig. 11 shows a zoom-in of the waveform of the 13-level inverter output. Figs. 12a and 12b show the inverter output voltage V_{inv} and the load current I_o waveforms when the inverter is tested with a highly resistive load and an RL load, respectively.

The inverter output voltage V_{inv} waveform when conducted with the solution angles set of the maximum THD is shown in Fig. 13. The output voltage THD for the minimum and maximum THD cases are found to be 6.6% and of 8.0% respectively, and they are shown in Fig. 14. These THD values demonstrate that the low order harmonics have been almost completely eliminated. They are generally in good agreement with the simulation results as depicted in Fig. 15, with slight deviations (not more than 0.3% THD).

VI. Conclusions

This paper has presented a modular method for implementing SHE modulation in an FPGA for a single-phase 13-level transistor-clamped H-bridge (TCHB) based cascaded multilevel inverter. When more TCHB cells are cascaded, double voltage levels are produced when compared to the conventional CHB topology. As a result, the output quality can be improved with a lower number of switches. Using Newton-Raphson's method, the optimum switching angles for eliminating the low order harmonics are obtained. The proposed SHE method produced a simple and precise implementation in practical applications. The analytical results were verified through simulation and experimental results, where the 3rd, 5th, 7th, 9th and 11th order harmonics have been successfully eliminated. The proposed SHE modulation can be extended to others multilevel topologies at any level of output.

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