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Analysis and Implementation of a New Three-Level Converter

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Abstract

This study presents a new interleaved three-level zero-voltage switching (ZVS) converter for high-voltage and high-current applications. Two circuit cells are operated with interleaved pulse-width modulation in the proposed converter to reduce the current ripple at the input and output sides, as well as to decrease the current rating of output inductors for high-load-current applications. Each circuit cell includes one half-bridge converter and one three-level converter at the primary side. At the secondary side, the transformer windings of two converters are connected in series to reduce the size of the output inductor or switching current in the output capacitor. Based on the three-level circuit topology, the voltage stress of power switches is clamped at $V_{in}/2$. Thus, MOSFETs with 500 V voltage rating can be used at 800 V input voltage converters. The output capacitance of the power switch and the leakage inductance (or external inductance) are resonant at the transition interval. Therefore, power switches can be turned on under ZVS. Finally, experiments verify the effectiveness of the proposed converter.

Key words: DC/DC Converter, PWM

I. INTRODUCTION

High-efficiency DC/DC converters have been studied as power units in the mature stage of the telecommunication systems, server systems, data storage systems, medical instruments, and cloud power units. For three-phase power factor correction (PFC) converters, DC bus voltage may be equal to or greater than 500 V to 800V. Thus, MOSFETs with 500 or 650 V voltage stress cannot be used for DC/DC converters at the mature stage. Although high-voltage MOSFETs can be used in DC/DC converters, such as those with 900 V voltage stress, these units are expensive, and the high turn-on resistance of MOSFETs will reduce circuit efficiency. Three-level or multi-level converters/inverters [1]-[4] have been established by using low-voltage switch devices for high-voltage applications, such as reactive power compensators and high-power motor drives. For modern switching converters, high-efficiency converters are required to reduce circuit size and weight. Therefore, power losses should be reduced to meet this requirement. Soft-switching techniques [5]-[10] with duty cycle control have been developed in three-level converters to reduce the switching losses on power semiconductors. The output capacitance of power switches and the leakage inductance of transformers are resonant at the transition interval to achieve zero voltage switching (ZVS) on power switches. Three-level converters with variable frequency control [11]-[14] have been proposed to enhance circuit efficiency further. If the operating switching frequency is less than the series resonant frequency, the rectifier diodes at the secondary side can be turned off under zero current switching. However, the output ripple current of a three-level resonant converter is larger than that of a conventional three-level PWM converter. Therefore, high output capacitance is necessary for use at the output side.

A new three-level converter is presented for high-input-voltage applications. The proposed converter includes two circuit cells, which are operated by an interleaved pulse-width modulation (PWM) to reduce the output ripple current and decrease the current stress of passive and active power components. Each circuit cell includes a half-bridge circuit and a three-level PWM circuit. In the proposed three-level converter, the voltage stress of power switches is limited to $V_{in}/2$. To reduce the ripple current on the output inductors or capacitor, the transformer secondary windings of two PWM circuits are connected in series at the low-voltage

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side to decrease the output inductor voltage variation. The flying capacitors are used in each circuit cell to balance input split capacitor voltages. Based on the resonant behavior of the output capacitances of MOSFETs and resonant inductance at the transition interval, all power switches can be turned on under ZVS. Finally, experiments based on a laboratory prototype are conducted to verify the effectiveness of the proposed converter.

II. CIRCUIT CONFIGURATION AND OPERATION PRINCIPLE

Figs. 1(a) and 1(b) show the circuit configurations of the conventional half-bridge and full-bridge converters with 400V input voltage for normal single-phase switching mode power supplies for server power or data storage power units. In Fig. 1(b), the phase-shift PWM scheme is adopted to regulate output voltage and achieve ZVS for all power switches within the desired load range. Normally, the ZVS condition of power switches at the leading leg is easier to be achieved than the power switches at the lagging leg. For three-phase switching mode power converters, the DC bus after the three-phase power factor corrector is normally controlled at 750 V to 800 V. To use MOSFETs instead of IGBTs for high switching operation, a three-level converter is given in Fig. 1(c). Two clamped diodes and one flying capacitor are adopted to reduce the voltage stress of power switches at $V_{in}/2$ and to balance two input capacitor voltages. Two voltage levels, namely, $V_{in}/(2n)$ and 0, are observed at the rectified voltage v_{rect}. If the voltage variation across the output inductor is decreased, the current ripple on the output inductor can be decreased. Thus, one more half-bridge converter can be added to the conventional three-level DC converter to reduce the current ripple at output side. Fig. 2(a) shows the circuit configuration of the proposed three-level converter. The proposed converter includes a conventional three-level converter [Fig. 1(c)] and a half-bridge converter [Fig. 1(a)] to reduce the voltage variation on the output inductor. The input voltage V_{in} is obtained from a three-phase AC/DC converter with PFC. C_1 and C_2 are input as split capacitances to obtain the equal voltages $V_{C1}=V_{C2}=V_{in}/2$. S_1–S_4 are power MOSFETs with $V_{in}/2$ voltage stress. The average voltages of flying capacitors are $V_{Cf1}=V_{Cf2}=V_{in}/4$. C_{r1}–C_{r4} are the output capacitances of S_1–S_4, respectively. L_{r1} and L_{r2} are resonant inductances. L_o is the output inductance. D_1 and D_2 are rectifier diodes. T_1 and T_2 are the isolated transformers. C_o and R_o denote output capacitance and load resistance, respectively. In the proposed circuit, a three-level converter and a half-bridge converter are used to achieve ZVS turn-on for all switches and to reduce the output inductance or output capacitance. Components C_{f1}, C_{f2}, S_3, S_4, T_2, and L_{r2} are operated as an uncontrolled half-bridge converter with 50% duty cycle. Two voltage levels, $V_{in}/4$ and

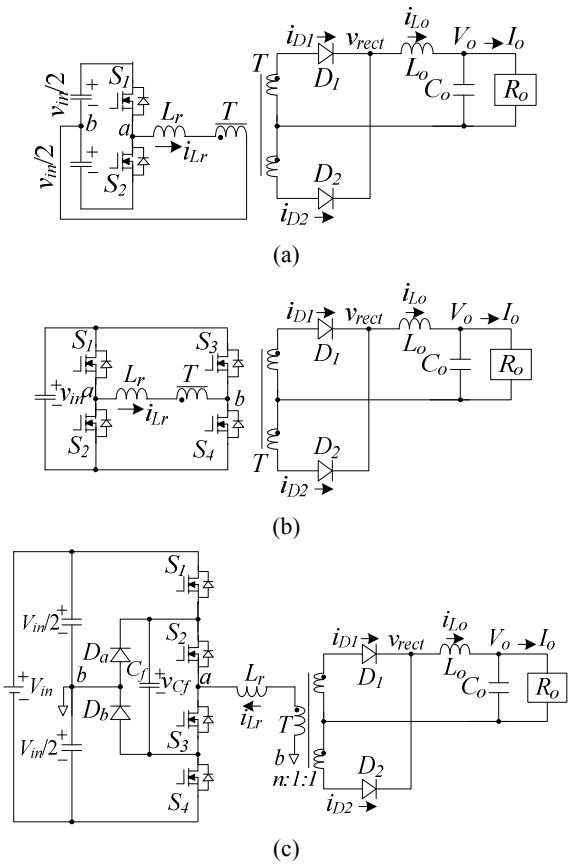
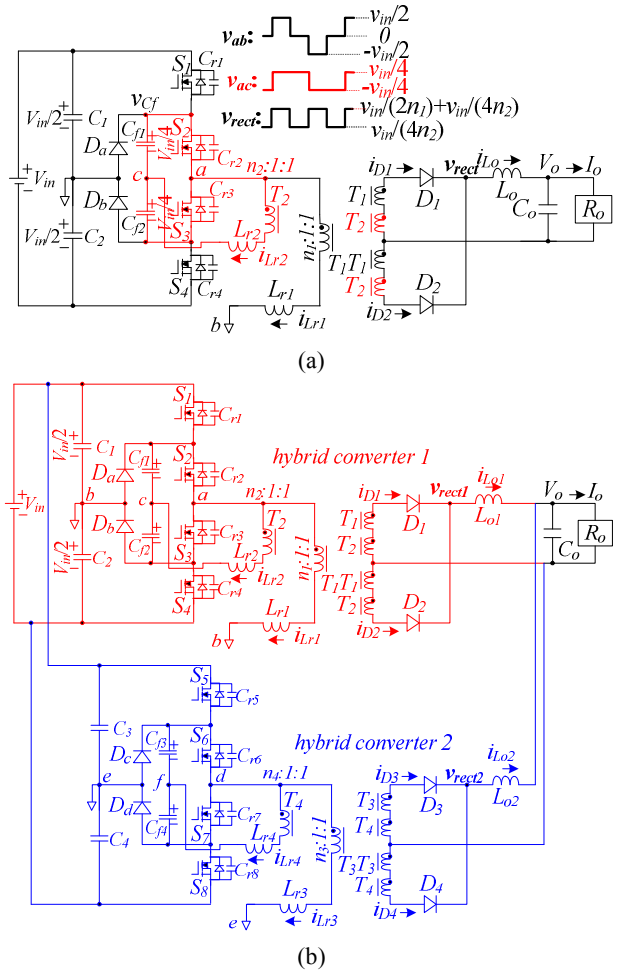


Fig. 1. Circuit configurations. (a) Conventional PWM half-bridge converter. (b) Conventional phase-shift full-bridge converter. (c) Conventional three-level converter.

$-V_{in}/4$, are generated on v_{ac}. Components C_1, C_2, D_a, D_b, C_{f1}, C_{f2}, S_1–S_4, L_{r1}, and T_1 are operated as the conventional three-level converter. Three voltage levels, namely, $V_{in}/2$, 0, and $-V_{in}/2$, are generated on v_{ab}. Two voltage levels, $V_{in}/(2n_1)+V_{in}/(4n_2)$ and $V_{in}/(4n_2)$, can be observed on the rectified voltage v_{rect}. Thus, low ripple current or switching current on the output inductor can be achieved because of the low voltage across the output inductor. The output capacitances of S_1–S_4 and the resonant inductance (or transformer leakage inductance) are resonant at the transition interval. Therefore, S_1–S_4 can be turned on under ZVS. To reduce the current ripple further at the input and output sides, as well as to reduce the current rating of output inductor for high load current application, an interleaved three-level converter is shown in Fig. 2(b). The interleaved PWM scheme is adopted to generate eight gate signals of S_1–S_4. The input and output ripple currents of two converters can partially cancel each other. Therefore, the input and output capacitances and output inductances can be reduced.

The system analysis of the proposed converter is based on the following assumptions: (1) $V_{Cf1}=V_{Cf2}=V_{Cf3}=V_{Cf4}=V_{in}/4$; (2) $V_{C1}=V_{C2}=V_{C3}=V_{C4}=V_{in}/2$; (3) $C_{r1}=C_{r2}=\ldots=C_{r7}=C_{r8}=C_r$; (4) S_1–S_8, D_1–D_4, and D_a–D_d are ideal; (5) turn ratio of T_1 and T_3



(a)

(b)

Fig. 2. Circuit configuration. (a) New three-level converter. (b) Adopted interleaved three-level converter.

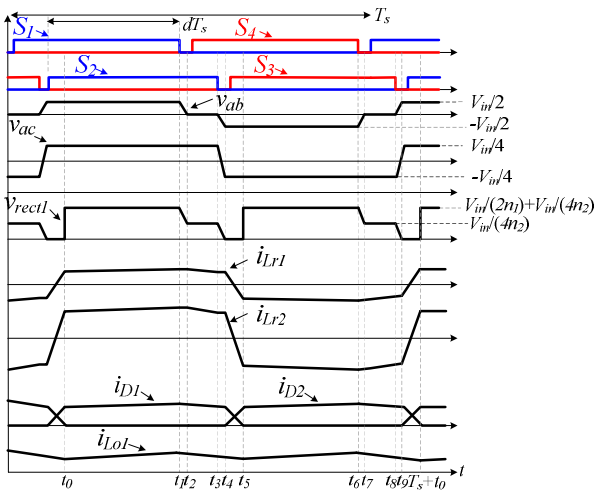


Fig. 3. Main waveforms of three-level converter 1.

is $n_1=n_3=n$ and that of T_2 and T_4 is $n_2=n_4=n/2$; and (6) the energy stored in the resonant inductances is greater than that stored in the resonant capacitances, such that the ZVS turn-on of all switches can be achieved. Based on the on/off states of S_1–S_8, D_a–D_d, and D_1–D_4, 10 operation modes exist in each three-level converter during one switching cycle. The key waveforms of each three-level converter during one switching cycle are given in Fig. 3. Fig. 4 shows the key waveforms of the proposed interleaved three-level converter. Two output inductor currents partially cancelled each other. Two three-level converters have the same operation modes. Thus, only the operation modes of converter 1 are discussed to simplify the system analysis. Three-level converter 1 has 10 operation modes (Fig. 5). Prior to t_0, S_1, S_2 D_1, and D_2 are conducting. Inductor currents i_{Lr1} and i_{Lr2} are increasing.

***Mode 1 [t_0≤t<t_1, Fig. 5(a)]*:** At t_0, i_{D2} is decreased to zero current, such that D_2 is off. S_1 and S_2 are still turned on, such that $v_{ab}=V_{in}/2$, $v_{ac}=v_{Cf1}=V_{in}/4$, $v_{rect1}\approx V_{in}/(2n_1)+V_{in}/(4n_2)=V_{in}/n$, and $v_{Lo1}=V_{in}/n-V_o>0$. The output inductor current i_{Lo1} and the primary currents i_{Lr1} and i_{Lr2} increase in this mode. Power is transferred from input voltage source $V_{in}/2$ to output load R_o.

***Mode 2 [t_1≤t<t_2, Fig. 5(b)]*:** At t_1, S_1 is turned off. Given that $i_{Lr1}>0$ and $i_{Lr2}>0$, C_{r1} and C_{r4} are charged and discharged in this mode. If the energy stored in L_{r1} and L_{o1} is greater than the energy stored in C_{r1} and C_{r4}, then C_{r4} can be discharged to zero voltage. The ZVS turn-on condition of S_4 can be expressed as

$$(L_{r1}+n^2L_{o1})i_{Lr1}^2(t_1)\geq C_rV_{in}^2/2 \quad (1)$$

This mode ends at t_2 when $v_{Cr1}=V_{in}/2$ and $v_{Cr4}=0$.

***Mode 3 [t_2≤t<t_3, Fig. 5(c)]*:** At t_2, $v_{Cr1}=V_{in}/2$, $v_{Cr4}=0$, and D_a are conducting. Capacitor voltage $v_{C2}=v_{Cf1}+v_{Cf2}=V_{in}/2$. Given that $i_{Lr1}>0$, the anti-parallel diode of S_4 is conducting. Thus, S_4 can be turned on at this moment to achieve ZVS. In this mode, the primary side voltage $v_{ab}=0$ and $v_{ac}=v_{Cf1}=V_{in}/4$, and the secondary side voltage $v_{rect1}=V_{in}/(2n)$. The output inductor voltage $v_{Lo1}=V_{in}/(2n)-V_o<0$, such that that the output inductor current i_{Lo1} decreases in this mode.

***Mode 4 [t_3≤t<t_4, Fig. 5(d)]*:** At t_3, S_2 is turned off. Given that $i_{Lr1}>0$ and $i_{Lr2}>0$, C_{r2}, and C_{r3} are charged and discharged, respectively. If the energy stored in L_{r1}, L_{r2}, and L_{o1} is greater than the energy stored in C_{r2} and C_{r3}, then C_{r3} can be discharged to zero voltage. Thus, the ZVS turn-on condition of S_3 can be obtained in (2).

$$(L_{r1}+n^2L_{o1})i_{Lr1}^2(t_3)+(L_{r2}+n^2L_{o1}/4)i_{Lr2}^2(t_3)\geq C_rV_{in}^2/2 \quad (2)$$

***Mode 5 [t_4≤t<t_5, Fig. 5(e)]*:** At time t_4, $v_{Cr2}=V_{in}/2$, and $v_{Cr3}=0$. Given that $i_{Lr1}>0$ and $i_{Lr2}>0$, the anti-parallel diode of S_3 is conducting. S_3 can be turned on at this moment under ZVS. D_1 and D_2 are conducting to commutate the inductor current i_{Lo1}. The secondary side voltage $v_{rect1}=0$, and the inductor current i_{Lo1} is decreasing. The primary inductor currents i_{Lr1} and i_{Lr2} decrease with the slopes $-V_{in}/(2L_{r1})$ and $-V_{in}/(4L_{r2})$,

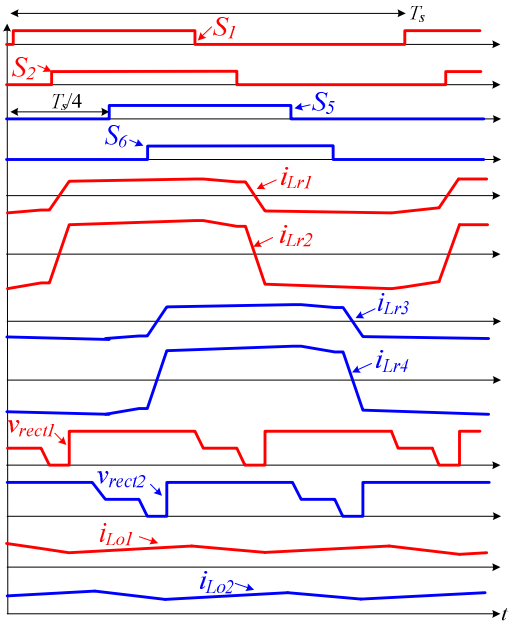


Fig. 4. Key waveforms of the proposed interleaved three-level converter.

respectively. The slopes of the diode currents i_{D1} and i_{D2} are given by

$$\frac{di_{D1}(t)}{dt}=-\frac{nV_{in}}{4L_{r1}}=-\frac{nV_{in}}{16L_{r2}},\quad \frac{di_{D2}(t)}{dt}=\frac{nV_{in}}{4L_{r1}}=\frac{nV_{in}}{16L_{r2}} \quad (3)$$

Based on (3), the relationship of L_{r1} and L_{r2} can be described as $L_{r1}=4L_{r2}$. At t_5, i_{D1} is decreased to zero current. The current variation on inductor L_{r1} is $\Delta i_{Lr1}=i_{Lr1}(t_5)-i_{Lr1}(t_4)\approx -I_o/(2n)-I_o/(2n)=-I_o/n$. The time interval in this mode is given as

$$\Delta t_{45}=t_5-t_4=-\frac{I_o}{n}\times(-\frac{2L_{r1}}{V_{in}})=\frac{2I_oL_{r1}}{nV_{in}} \quad (4)$$

In this mode, S_3, S_4, D_1, and D_2 are conducting, and the rectified voltage $v_{rect1}=0$. No power is transferred from input voltage source V_{in} to output load R_o. The duty loss in this mode can be expressed as

$$d_{loss,5}=\frac{\Delta t_{45}}{T_s}\approx\frac{2I_oL_{r1}f_s}{nV_{in}} \quad (5)$$

***Mode 6 [$t_5\le t<t_6$, Fig. 5(f)]*:** At t_5, $i_{D1}=0$. S_3 and S_4 are conducting. The primary side AC voltages $v_{ab}=-V_{in}/2$ and $v_{ac}=-v_{Cf2}=-V_{in}/4$, and the output inductor voltage $v_{Lo1}=V_{in}/n-V_o>0$. The primary side inductor currents i_{Lr1} and i_{L2} both decrease, whereas the output inductor current i_{Lo1} increases in this mode.

***Mode 7 [$t_6\le t<t_7$, Fig. 5(g)]*:** At t_6, S_4 is turned off. Given that $i_{Lr1}<0$ and $i_{Lr2}<0$, C_{r1} and C_{r4} are discharged and charged, respectively. The ZVS turn-on condition of S_1 can be expressed as

$$(L_{r1}+n^2L_{o1})i_{Lr1}^2(t_6)\ge C_rV_{in}^2/2 \quad (6)$$

At t_7, C_{r1} is discharged to zero voltage.

***Mode 8 [$t_7\le t<t_8$, Fig. 5(h)]*:** At t_7, $v_{Cr1}=0$, and $v_{Cr4}=V_{in}/2$. Given that $i_{Lr1}<0$, the anti-parallel diode of S_1 is conducting. S_1 can be turned on at this moment under ZVS. D_b is conducting, and the AC terminal voltages $v_{ab}=0$ and $v_{ac}=-v_{Cf2}=-V_{in}/4$. The primary inductor currents i_{Lr1} and i_{Lr2} are both decreasing. The rectified voltage $v_{rect1}=V_{in}/(2n)$, and the output inductor voltage $v_{Lo1}=V_{in}/(2n)-V_o<0$, such that i_{Lo1} decreases in this mode.

***Mode 9 [$t_8\le t<t_9$, Fig. 5(i)]*:** At t_8, S_3 is turned off. Given that $i_{Lr1}<0$ and $i_{Lr2}<0$, C_{r2} and C_{r3} are discharged and charged, respectively. Similar to (2), the ZVS turn-on condition of S_2 can be obtained as

$$(L_{r1}+n^2L_{o1})i_{Lr1}^2(t_8)+(L_{r2}+n^2L_{o1}/4)i_{Lr2}^2(t_8)\ge C_rV_{in}^2/2 \quad (7)$$

***Mode 10 [$t_9\le t<t_0+T_s$, Fig. 5(j)]*:** At t_9, C_{r2} is discharged to zero voltage. Given that $i_{Lr1}(t_9)+i_{Lr2}(t_9)<0$, the anti-parallel diode of S_2 is conducting. S_2 can be turned on at this moment under ZVS. D_1 and D_2 are conducting to commutate the load inductor current i_{Lo1}. In this mode, S_1, S_2, D_1, and D_2 are conducting. Thus, the rectified voltage $v_{rect1}=0$ and the inductor voltage $v_{Lo1}=-V_o$. No power is transferred from input voltage source V_{in} to output load R_o. Thus, the duty loss in this mode is given as

$$d_{loss,10}=\frac{\Delta t_{09}}{T_s}\approx\frac{2I_oL_{r1}f_s}{nV_{in}}=d_{loss,5} \quad (8)$$

At t_0+T_s, i_{D2} is decreased to zero current. The circuit operations of the proposed converter in a switching period are then completed.

III. Circuit Characteristics

In the above discussions, the charge and discharge times of C_{r1}–C_{r4} in modes 2, 4, 7, and 9 are significantly less than the other time intervals. Thus, these modes can be neglected in the discussion of circuit characteristics. From modes 3 and 8 in Fig. 5, the spite capacitor voltages v_{C1}–v_{C4} can be obtained as $v_{C1}=v_{C2}=v_{C3}=v_{C4}=V_{in}/2$. Applying the volt-second balance to L_{r2} and T_2 in steady state, the average capacitor voltages V_{Cf1}–V_{Cf4} can be derived as

$$V_{Cf1}=V_{Cf2}=V_{Cf3}=V_{Cf4}=V_{in}/4 \quad (9)$$

Based on the volt-second balance on output inductors L_{o1} and L_{o2}, the output voltage V_o can be derived as

$$\begin{aligned}V_o&=\frac{V_{in}}{n}(0.5+d-2d_{loss,10})-V_f\\&=\frac{V_{in}}{n}(0.5+d-\frac{4L_{r1}I_of_s}{nV_{in}})-V_f\end{aligned} \quad (10)$$

where V_f is the voltage drop on diodes D_1–D_4; and d is the duty ratio of the AC side voltages v_{ab}, v_{ac}, v_{de}, and v_{df}. The ripple currents of L_{o1} and L_{o2} are expressed in (11).

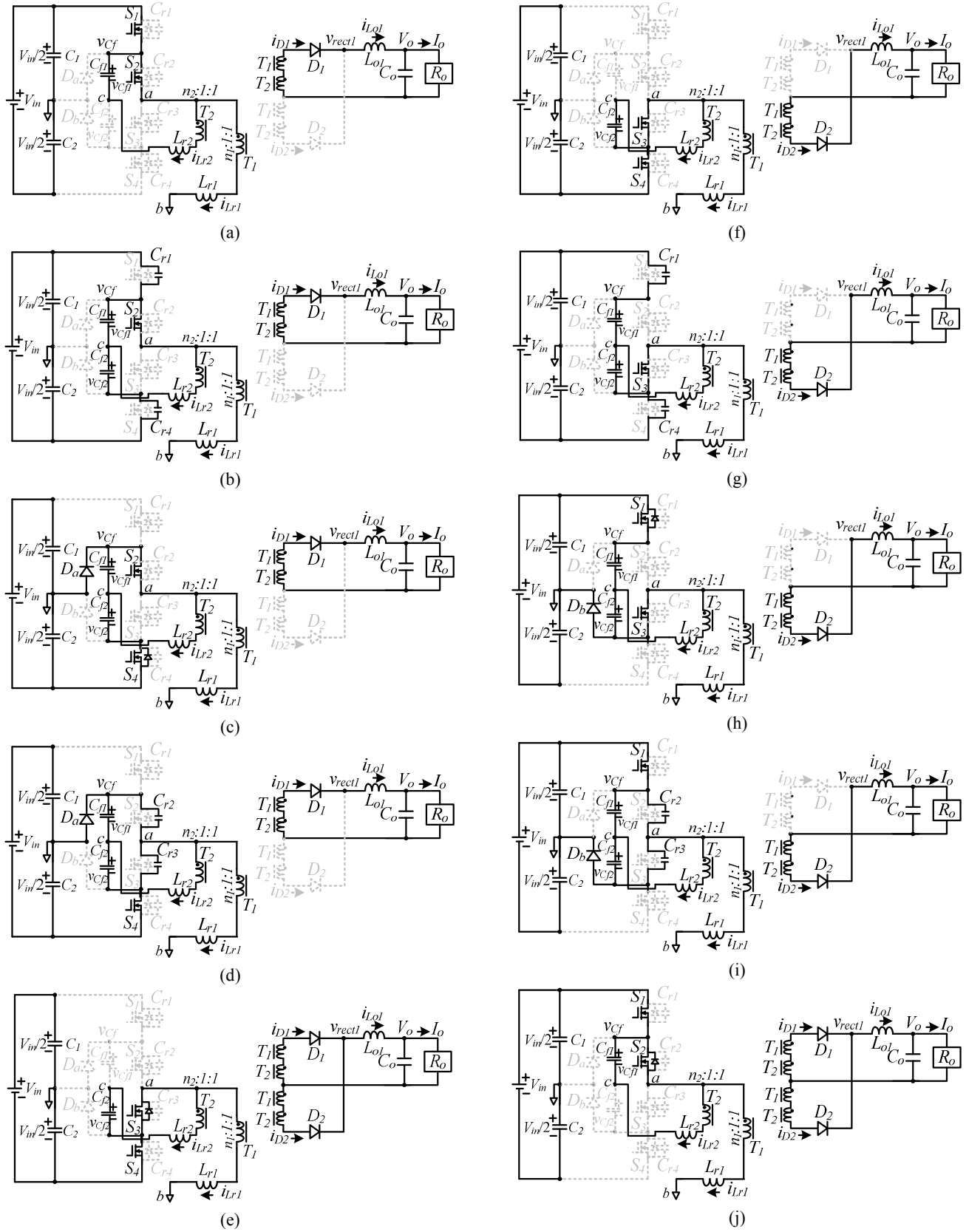


Fig. 5. Operation modes of the proposed converter during one switching cycle. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (h) Mode 8. (i) Mode 9. (j) Mode 10.

$$\Delta i_{Lo1} = \Delta i_{Lo2} = \frac{(V_{in}/n - V_o - V_f)}{L_o f_s}(d - \frac{2I_o L_{r1} f_s}{nV_{in}}) = rI_o/2 \quad (11)$$

where r is the current ripple factor of output inductors. The maximum output inductor currents at steady state are expressed in (12).

$$i_{Lo1,\max} = i_{Lo2,\max} = (1+0.5r)I_o/2 = \frac{I_o}{2} + \frac{(V_{in}/n - V_o - V_f)}{2L_o f_s}(d - \frac{2I_o L_{r1} f_s}{nV_{in}}) \quad (12)$$

In modes 1 and 6, the magnetizing ripple currents Δi_{Lm1}–Δi_{Lm4} can be expressed in (13) and (14).

$$\Delta i_{Lm1} = \Delta i_{Lm3} \approx \frac{V_{in}(d - d_{loss,10})T_s}{2L_{m1}} = \frac{dV_{in}T_s}{2L_{m1}} - \frac{I_o L_{r1}}{nL_{m1}} \quad (13)$$

$$\Delta i_{Lm2} = \Delta i_{Lm4} \approx \frac{V_{in}(d - d_{loss,5})T_s}{4L_{m2}} = \frac{dV_{in}T_s}{4L_{m2}} - \frac{I_o L_{r1}}{2nL_{m2}} \quad (14)$$

where L_{m1}=L_{m3}, and L_{m2}=L_{m4}. The average diode currents $i_{D1,av}$–$i_{D4,av}$ and the diode voltage stresses $v_{D1,stress}$–$v_{D4,stress}$ are given in (15) and (16), respectively.

$$i_{D1,\text{av}} = i_{D2,av} = i_{D3,\text{av}} = i_{D4,av} \approx I_o/4 \quad (15)$$

$$v_{D1,\text{stress}} = v_{D2,\text{stress}} = v_{D3,\text{stress}} = v_{D4,\text{stress}} \approx 2V_{in}/n \quad (16)$$

If the ripple currents of S_1-S_8 can be ignored, the root-mean-square (*rms*) currents and the voltage stress of S_1–S_8 are given in (17)–(19).

$$i_{S1,rms} = i_{S4,rms} = i_{S5,rms} = i_{S8,rms} \approx \frac{I_o}{2n\sqrt{2}} \quad (17)$$

$$i_{S2,rms} = i_{S3,rms} = i_{S6,rms} = i_{S7,rms} \approx \frac{3I_o}{2n\sqrt{2}} \quad (18)$$

$$v_{S1,stress} = ... = v_{S8,stress} \approx V_{in}/2 \quad (19)$$

In mode 2, $i_{Lr1}(t_1)$ can be expressed as

$$i_{Lr1}(t_1) = -i_{Lr1}(t_6) \approx i_{Lm1,\max} + \frac{i_{Lo1,\max}}{n} = \frac{dV_{in}T_s}{4L_{m1}} - \frac{I_o L_{r1}}{2nL_{m1}} + \frac{I_o}{2n} + \frac{(V_{in}/n - V_o - V_f)}{2nL_o f_s}(d - \frac{2I_o L_{r1} f_s}{nV_{in}}) \quad (20)$$

In mode 4, the inductor currents $i_{Lr1}(t_3)$ and $i_{Lr2}(t_3)$ can be expressed as

$$i_{Lr1}(t_3) = -i_{Lr1}(t_8) \approx i_{Lr1}(t_1) - \frac{(V_o + V_f - V_{in}/2n)\Delta t_{23}}{nL_o} = \frac{dV_{in}T_s}{4L_{m1}} - \frac{L_{r1}I_o}{2nL_{m1}} + \frac{I_o}{2n} + \frac{(V_{in}/n - V_o - V_f)}{2nL_o f_s}(d - \frac{2L_{r1}I_o f_s}{nV_{in}}) - \frac{(V_o + V_f - V_{in}/2n)(0.5-d)}{nL_o f_s} \quad (21)$$

$$i_{Lr2}(t_3) = i_{Lr2}(t_8) \approx i_{Lm2,\max} + \frac{i_{Lo1}(t_3)}{n/2} = \frac{dV_{in}T_s}{8L_{mb}} - \frac{L_{r1}I_o}{4nL_{m2}} + \frac{I_o}{n} + \frac{(V_{in}/n - V_o - V_f)}{nL_o f_s}(d - \frac{2L_{r1}I_o f_s}{nV_{in}}) - \frac{2(V_o + V_f - V_{in}/2n)(0.5-d)}{nL_o f_s} \quad (22)$$

Based on (1), (6), and (20), the necessary resonant inductance L_{r1} for ZVS turn-on of S_1 and S_4 is expressed in (23).

$$L_{r1} \geq \frac{C_r V_{in}^2}{2i_{Lr1}^2(t_1)} - n^2 L_{o1} \quad (23)$$

From (2), (7), (21), and (22), the necessary resonant inductance L_{r2} for ZVS turn-on of S_2 and S_3 is given in (24).

$$L_{r2} \geq [\frac{C_r V_{in}^2}{2} - (L_{r1} + n^2 L_{o1})i_{Lr1}^2(t_3)]/i_{Lr2}^2(t_3) - n^2 L_{o1} \quad (24)$$

Given that the switch currents i_{S5}–i_{S8} are similar to i_{S1}–i_{S4} in steady state, the necessary resonant inductances L_{r3} and L_{r4} are equal to L_{r1} and L_{r2}, respectively, to achieve ZVS conditions of S_5–S_8.

IV. Experimental Results

A laboratory prototype shown in Fig. 6 is implemented to verify the effectiveness of the proposed converter. The electrical specifications of the proposed converter are V_{in}=750 V–800 V, V_o=48 V, I_o=40 A, and f_s=100 *k*Hz. The resonant inductances in this prototype are L_{r1}=L_{r3}=48 μH and L_{r2}=L_{r4}=12 μH. The magnetic core TDK EER-40C is used for T_1–T_4. The winding turns of T_1 and T_3 a 48:4:4 and the winding turns of T_2 is 30:5:5. The magnetizing inductances L_{m1}=L_{m3}=2.3 *m*H and L_{m2}=L_{m4}=*1.2 m*H, and the output inductances L_{o1}=L_{o2}=1 2μ*H*. MOSFETs IRFP460 with V_{DS}=500 V, $I_{d,rms}$=20 A are used for switches S_1–S_8. The KCU30A30 fast recovery diodes with 300 V voltage rating and 30 A average current are used for D_1–D_4. Fast recovery diodes 30ETH06 are adopted for the clamped diodes D_a–D_d. The DC input capacitances C_1–C_4 are 220μF. The flying capacitances C_{f1}–C_{f4} are 1 μF. The output capacitance C_o is 4000 μF. The measured waveforms of the PWM signals of S_1–S_4 of the first circuit cell at full load are shown in Fig. 7. Fig. 8 provides the measured gate voltages of S_1 and S_2 in the first circuit cell and those of S_5 and S_6 in the second circuit cell under full load conditions. S_5 and S_6 in the second circuit are clearly phase-shifted by one-fourth of the switching period with respect to S_1 and S_2 in the first circuit. Fig. 9 shows the measured results of the AC side voltages v_{ab}–v_{df} and the rectified voltages v_{rect1} and v_{rect2} at full load. Three voltage levels, V_{in}/2, 0, and -V_{in}/2, are generated on AC side voltages v_{ab} and v_{de}; and two voltage levels V_{in}/4 and -V_{in}/4 are generated on voltages v_{ac} and v_{df}. Three voltage levels, V_{in}/n, V_{in}/(2n), and 0, are shown at the rectified voltages v_{rect1} and v_{rect2}. Fig. 10 gives the measured results of gate voltage, drain voltage, and switch current of S_1 at half and full load conditions under 800 V input voltage. Similarly, the measured gate voltage, drain voltage, and switch current of S_2 at 50% and 100% loads are given in Fig. 11. Figs. 10 and 11 clearly show that S_1 and S_2 are all turned on under ZVS. S_3 and S_4 have the same switch current and voltage waveforms as S_2 and S_1, respectively. Thus, S_3 and S_4 are also turned on

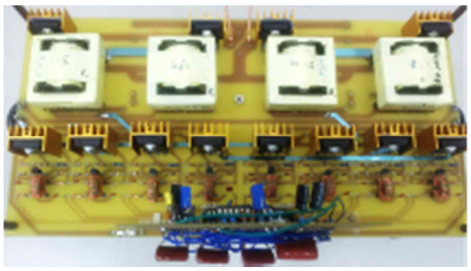


Fig. 6. Photograph of the prototype circuit.

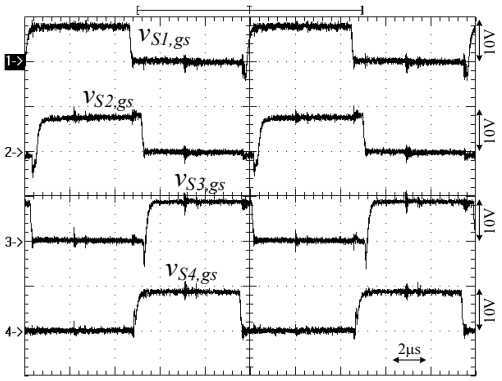


Fig. 7. Measured results of gate voltages of S_1–S_4 at full load.

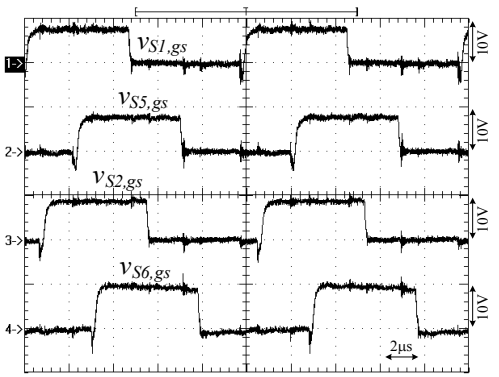


Fig. 8. Measured results of gate voltages of S_1, S_2, S_5, and S_6 at full load.

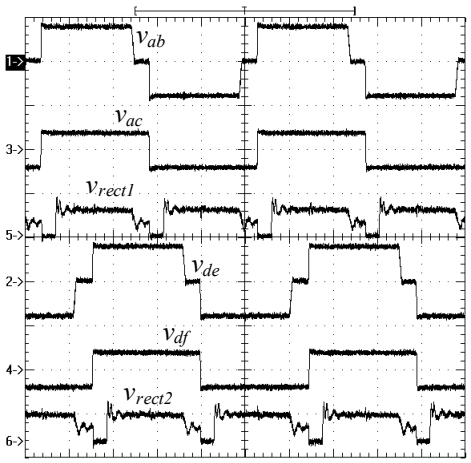


Fig. 9. Measured results of the AC side voltages v_{ab}–v_{df} and the rectified voltages v_{rect1} and v_{rect2} at full load [v_{ab}–v_{df}: 500V/div; v_{rect1}, v_{rect2}100 V/div; time 2 µs/div].

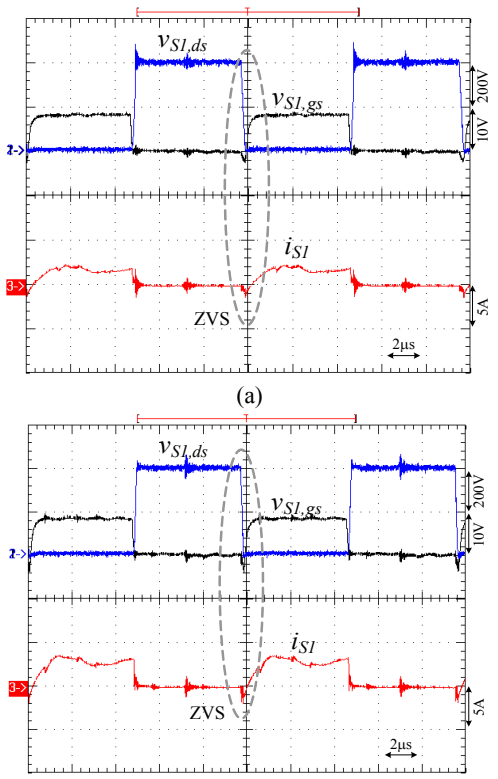


Fig. 10. Measured waveforms of gate voltage, drain voltage and switch current of S_1 at (a) 50% load and (b) full load.

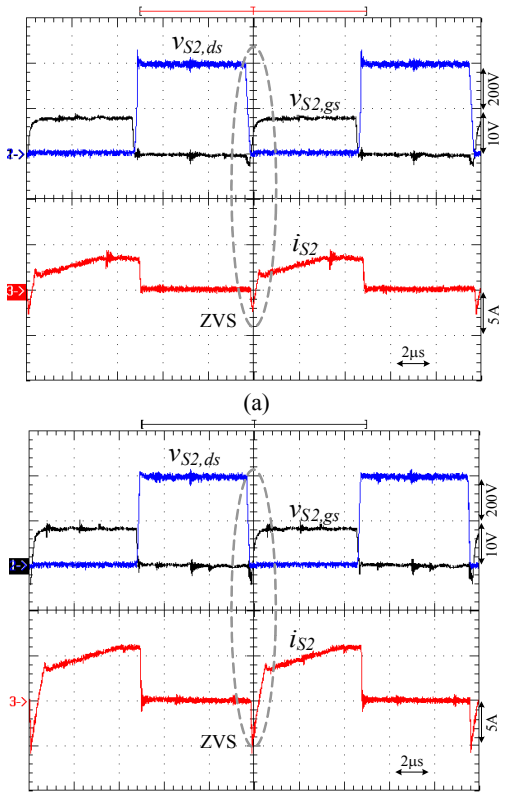


Fig. 11. Measured waveforms of gate voltage, drain voltage, and switch current of S_2 at (a) 50% load and (b) full load.

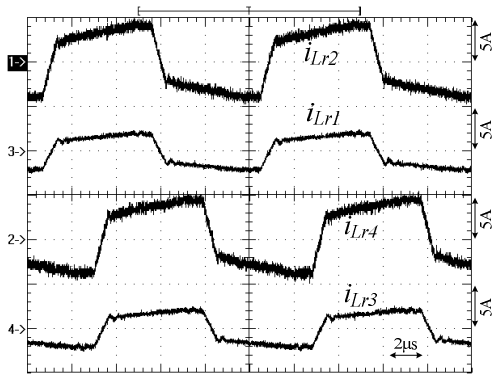


Fig. 12. Measured waveforms of inductor currents i_{Lr1}–i_{Lr4} at full load.

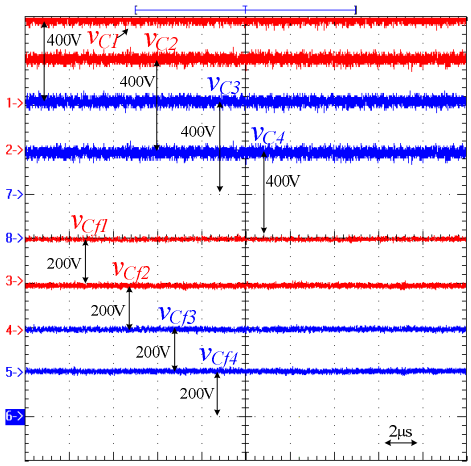


Fig. 13. Measured input capacitor voltages v_{C1}–v_{C4} and flying capacitor voltages v_{Cf1}–v_{Cf4} at full load.

under ZVS from 50% load to full load. Switches S_5–S_8 in the second circuit cell have the same PWM signals as S_1–S_4 in the first circuit cell. Thus, S_5–S_8 are also turned on under ZVS from 50% to 100% load. Fig. 12 shows the measured waveforms of inductor currents i_{Lr1}–i_{Lr4} at full load. When v_{ab} is positive, inductor currents i_{Lr1} and i_{L2} both increase. Moreover, inductor currents i_{Lr1} and i_{L2} both decrease when v_{ab} is negative. Inductor currents i_{Lr3} and i_{Lr4} are phase-shifted by one-fourth of the switching period with respect to i_{Lr1} and i_{Lr2}. Fig. 13 shows the measured input capacitor voltages v_{C1}–v_{C4} and the flying capacitor voltages v_{Cf1}–v_{Cf4} at full load, and V_{in}=800 V. The average flying capacitor voltages v_{Cf1}–v_{Cf4} are equal to 200 V, and the average voltages v_{C1}–v_{C4} are equal to 400 V. The measured diode currents i_{D1}–i_{D4} at full load are shown in Fig. 14. Fig. 15(a) shows the output inductor current at full load without interleaved PWM operation. The measured ripple current is approximately 16 A. Fig. 15(b) shows the measured output inductor currents i_{Lo1}, i_{Lo2} and the resultant output current i_{Lo1}+i_{Lo2} at full load. Two output inductor currents i_{Lo1} and i_{Lo2} are balanced and phase-shifted by one-half of the switching period. The ripple current on i_{Lo1}+i_{Lo2} is approximately 6 A in Fig. 15(b). From

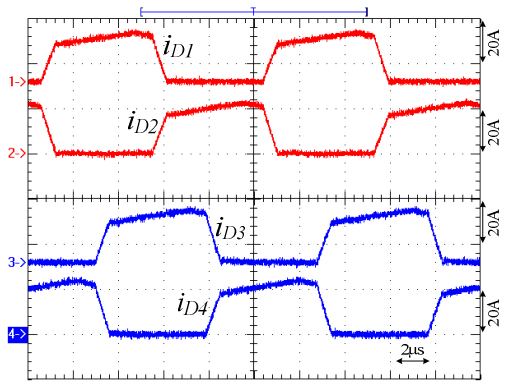


Fig. 14. Measured diode currents i_{D1}–i_{D4} at full load.

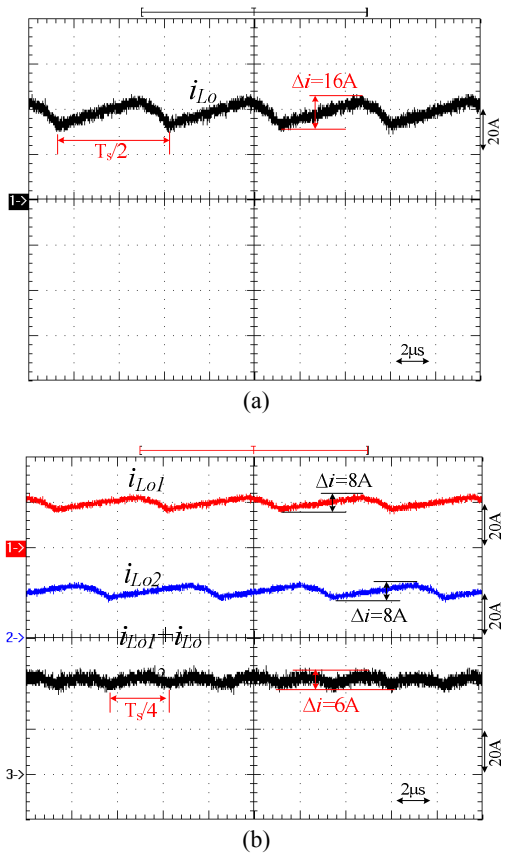


Fig. 15. Measured waveforms of output inductor currents at full load (a) without interleaved operation and (b) with interleaved operation.

Fig. 15, the resultant output inductor current iLo1+iLo2 with interleaved operation has less current ripple than the output inductor current without interleaved operation. Fig. 16 presents the measured output ripple voltage with and without interleaved PWM operation under full load condition. The proposed converter with interleaved PWM operation has low output ripple voltage. The measured circuit efficiencies at different input voltage and load conditions are shown in Fig. 17.

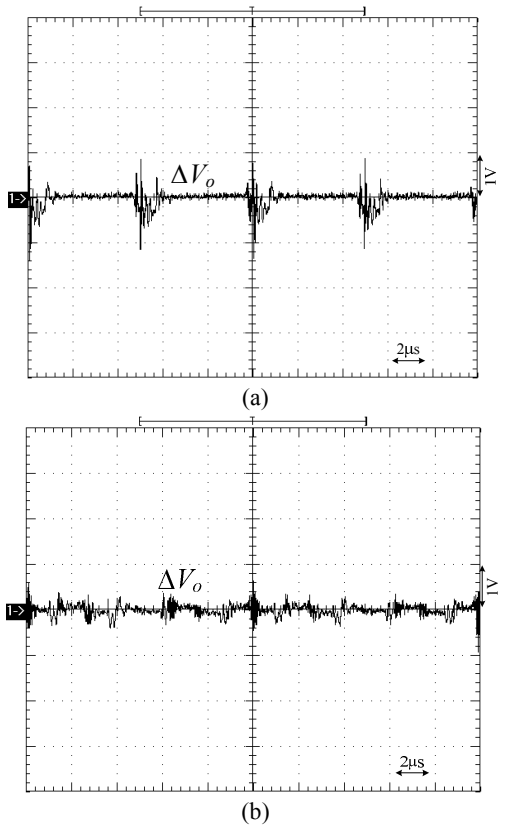


Fig. 16. Measured output ripple voltage under full load (a) without interleaved operation and (b) with interleaved operation.

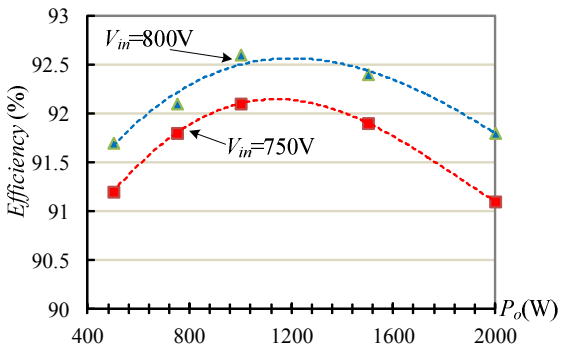


Fig. 17. Measured circuit efficiencies at different input voltage and load conditions.

V. Conclusions

A new three-level ZVS converter for high-input-voltage applications is presented with the features of ZVS turn-on for all switches from 50% load to full load, low voltage stress of power switches, and low voltage variation on output inductors. Two three-level converters are operated by interleaved PWM scheme to reduce the current rating of active and passive components and decrease the current ripple at the output side. In each converter, the voltage stress of power switches is clamped at $V_{in}/2$ by using three-level diode clamped topology. Two flying capacitors are adopted in each circuit cell to balance two input split capacitor voltages. The proposed three-level converter combines one half-bridge PWM converter and one three-level PWM converter to reduce the output inductor voltage variation. Therefore, the switching current in the output capacitor can be reduced compared with the switching capacitor current in the conventional three-level PWM converter. Finally, experiments are provided to verify the effectiveness of the proposed converter.

Acknowledgment

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