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Digital Control of Secondary Active Clamp Phase-Shifted Full-Bridge Converters

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Abstract

A DSP-based self-adaptive proportional-integral (PI) controller to control a DC-DC converter is proposed in this paper. The full-bridge topology is adopted here to obtain higher power output capability and higher conversion efficiency. The converter adopts the zero-voltage-switching (ZVS) technique to reduce the conduction losses. A parallel secondary active clamp circuit is added to deal with the voltage overshoot and ringing effect on the transformer's secondary side. A self-adaptive PI controller is proposed to replace the traditional PI controller. Moreover, the designed converter adopts the constant-current and constant-voltage (CC-CV) output control strategy. The secondary active clamp mechanism is discussed in detail. The effectiveness of the proposed converter was experimentally verified by an IGBT-based 10kW prototype.

Key words: Digital control, Phase-shifted full-bridge, Secondary active clamp, Self-adaptive PI control

I. INTRODUCTION

Nowadays, clean and renewable energies including fuel cells, wind energy, photovoltaic, etc., have been widely applied to achieve environmentally-friendly objectives. Converters play key roles in the energy transformation [1].

As is known, a full-bridge converter can possess a higher power density by increasing the carrier frequency of the power transistors. However, the energy conversion efficiency is reduced due to the switching loss of the higher switching frequency, worsening the thermal and electromagnetic interference effects. In order to solve these problems, a phase-shift full-bridge (PSFB) converter with ZVS is proposed here. Some of the prominent features of this topology include high efficiency, high power density, and ZVS that is easy to achieve [2]. ZVS for all of the switches can be obtained by utilizing the transformer's leakage inductance and the intrinsic capacitance of the switches without any additional circuitry [3,4]. In high power level applications, for example higher than 5 kW, insulated gate bipolar transistor (IGBT) devices are usually preferred and predominantly used as power switches [5], [6].

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DC-DC converters usually utilize rectifiers at the output side. However, rectifiers having a relatively long recovery time will produce voltage spikes. The parasitic capacitance of the rectifiers will resonate with the transformer's leakage inductance causing high frequency oscillations on the transformer's secondary side [3].

There have been some attempts to overcome the aforementioned drawbacks. A resistance-capacitor-diode snubber circuit was proposed and it works well by limiting the peak value of the rectifier voltage oscillation [7], [8]. However, a power loss in the snubber resistance degrades the system efficiency when the output power increases.

The converter proposed in [2] employs an asymmetric auxiliary circuit to provide reactive current for the full-bridge semiconductor switches, which guarantees ZVS at the turn-on time. Although this control scheme is able to determine the optimum value of the reactive current injected by the auxiliary circuit, extra conduction losses in the power MOSFETs as well as in the auxiliary circuit can not be eliminated.

Papers [9] and [10] add auxiliary passive networks into the traditional converter and all of the primary switches can achieve ZVS in the entire load range. Furthermore, the parasitic oscillations of the rectifier voltage are lower because the leakage inductance can be designed to be rather small. However, it is a passive method not a fundamental solution for the oscillation between the leakage inductance and the

parasitic capacitance of the rectifier.

In addition, there have been some improvements in the control strategy of the converter. The converter in paper [11] adopts a constant-current and constant-voltage (CC-CV) charging strategy to charge lithium-ion battery packs. To improve the transient of the voltage regulation during load variations, a Probabilistic Fuzzy Neural Network (PFNN) controller is proposed to replace the traditional PI controller and to have the ability of online learning algorithms.

A novel ZVS PSFB PWM converter is proposed here. In order to reduce the voltage oscillations and the duty cycle loss on the transformer's secondary-side, a secondary active clamp circuit is added in this topology. The active clamp circuit consists of an IGBT, a capacitor and a diode. The voltage stress of the switches on the primary side is reduced and the ringing effect of the rectifier switches is restrained [12]. The PSFB converter realizes ZVS for the leading legs over a wide load range. The converter uses a digital signal processor (DSP) as the control core. The digital control core adopts a self adaptive PI control strategy, which provides good control performance even in harsh conditions and is simple when compared to that in paper [11]. In addition, the implementation of AD sampling and fault protection are also incorporated into the DSP [13], [14]. Experimental results are presented to verify the validity and strong points of the proposed converter.

II. Operation Analysis of the Converter and its Digital Fulfillment

The main topology of a PSFB converter with a secondary active clamp is shown in Fig. 1. There is a DC blocking capacitor C_{AB} in the transformer's primary side that is not sketched here. The converter is constructed using a full-bridge converter, a high frequency transformer T_1, and a LC low-pass filter. Switches Q_1-Q_4 are the working switches in the full bridge. Diodes D_1-D_4 serve as a rectifier. The output power is controlled by adjusting the phase-shift angle ϕ. In the steady state, the relationship between the input voltage V_{in} and the output voltage V_o can be represented by the following equation:

$$V_o = n_{tr}\frac{\Phi}{\pi}V_{in} \tag{1}$$

Where n_{tr} =Ns/Np is the transformer turns ratio, Np is the transformer primary turns, and Ns is the transformer secondary turns.

A. Phase-Shift Full-Bridge Operation Analyses

One working cycle of the PSFB converter can be divided into 12 operation modes (t_0~t_{12}). It is enough to analyze the first 6 operation modes since the following (7-12) modes are similar to the preceding 6 modes. The corresponding theoretical waveforms are depicted in Fig.2.

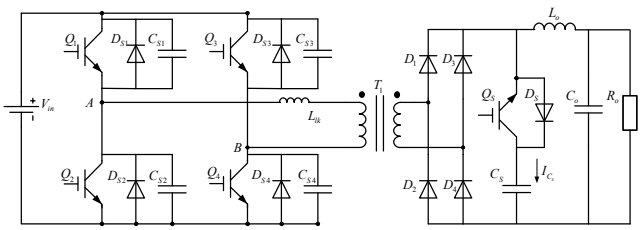


Fig. 1. Topology of PSFB converter with secondary active clamp circuit.

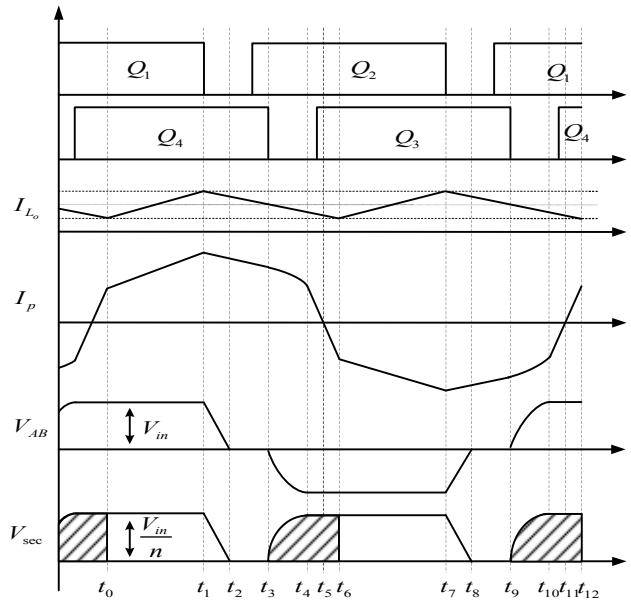


Fig. 2. Key waveforms of the PSFB converter.

1) Mode 1 (t_0-t_1): During this period, the IGBTs Q_1 and Q_4 are conducted. The transformer's primary voltage V_{ab} is equal to the input voltage V_{in}. The slope of I_p is depicted as:

$$\frac{di_p}{dt} = \frac{V_{in} - (V_o / n_{tr})}{L_{lk} + (L_o / n_{tr}^2)} \tag{2}$$

2) Mode 2 (t1-t2): S_1 turns off at t_1 and the current I_p flows through C_{s1} (the parallel buffer capacitor of Q_1). C_{s2} discharges when V_{ab} gradually decreases. Both sides of the transformer are still coupled. The secondary inductor is large. Therefore, I_p remains unchanged. This mode is usually known as the leading arm transition.

3) Mode 3 (t2-t3): The intrinsic diode D_{s2} (Q_2's reverse parallel diode) forward conducts and serves as a channel for I_p to flow through. During this period Q_2 can turn on under zero-voltage. The current I_p is predicted as:

$$\frac{di_p}{dt} = -\frac{V_o / n_{tr}}{L_{lk} + (L_o / n_{tr}^2)} \tag{3}$$

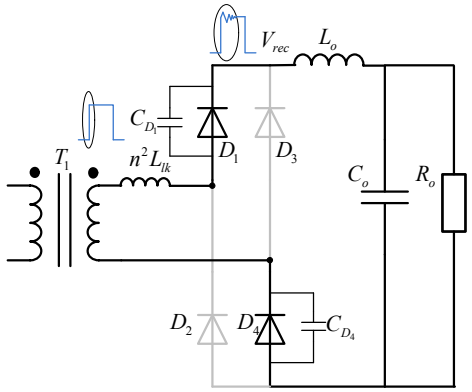


Fig. 3. Equivalent circuit of parasitic oscillation.

4) Mode 4 (t3-t4): Q_4 turns off under zero-voltage at t_3. The primary current I_p charges capacitor C_{s4} while capacitor C_{s3} gets discharged. The voltage V_{ab} gradually decreases and drops to $-V_{in}$ at t_4. This negative voltage forces the secondary diodes D_2 and D_3 to conduct. D_1 and D_4 can not be shut down immediately and eventually make the transformer's secondary short-circuited. Thus, the transformer becomes decoupled. This mode is also known as the lagging arm transition.

5) Mode 5 (t4-t5): D_{s3} forward conducts at t_4 and serves as a channel for I_p. Q_3 can turn on under zero-voltage during this period. The current I_p is predicted as:

$$\frac{di_p}{dt} = -\frac{V_{in}}{L_{lk}} \tag{4}$$

6) Mode 6 (t5-t6): The primary current I_p drops to zero at t_5 and it flows through S_2 and S_3. I_p begins to grow reversely and its pace is the same as in the preceding mode. I_{sec} also gradually increases and is equal to I_o at t_6. D_1 and D_4 turn off and both windings of the transformer regain their coupling.

B. Ringing Effect and the Secondary Active Clamp Circuit Operation Analysis

The transformer's secondary side in a typical PSFB converter is depicted in Fig. 3. The rectifier diodes have a relatively long reverse recovery time and will cause voltage spikes when it is reversely cut-off. The voltage V_{rec} on the rectifier can be seen as a step voltage. Under the action of V_{rec}, the parasitic capacitor of the rectifier diodes C_p will resonate with the leakage inductance L_{lk}, thus causing high frequency oscillations on the secondary side. This phenomenon is called the ringing effect [15], [16].

The oscillation frequency:

$$f_{ring} = \frac{1}{2\pi\sqrt{\frac{L_{lk}\cdot C_p}{n_{tr}^2}}} \tag{5}$$

The defects of the voltage spike include electric stress on the components, producing EMI noise and affecting the inverter's output characteristic. There are four commonly used measures to restrain peak oscillations [17], [18]:

1) Connecting the RC absorbing circuit and rectifier diodes in parallel. This method is easy to realize. However, it has greater losses in superpower circuits and does not perform well.
2) Adding a clamp diode at the primary side can restrain oscillations on the secondary to some extent. However, it cannot completely eliminate oscillations.
3) Connecting a saturated inductance in series with the rectifier circuits to restrain the transient change when low current flows through. This is an easy method. However, its main drawback is the heat trouble generated by the saturated inductance.
4) Adding an active clamp circuit in parallel with the rectifier output side can efficaciously suppress peak oscillations and release the energy to the loads. This method needs additional control circuits.

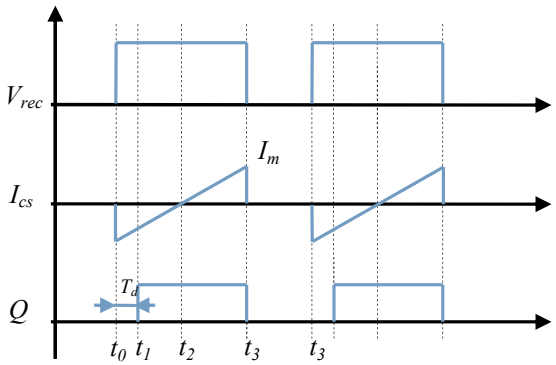


Fig. 4. Theoretical waveform of clamp circuit.

An active clamp circuit is adopted here to reduce the voltage spike and ringing effect. The clamp capacitance C_s is used to resonate with the leakage inductance L_{lk}. C_s absorbs voltage in the first half of the switching cycle and releases the energy to the load in the second half. The clamp capacitance C_s keeps its voltage unchanged in a cycle and its average charging and discharging current sums up to zero. The whole switching cycle can be seen in Fig. 4. It is advised to choose a clamp capacitance that is much larger than L_{lk} so that the resonant period is relatively long, as well as the charging and discharging current can be restrained.

The working cycle of Q_s (the secondary active clamp's switch) is divided into 4 operation modes. The modes are analyzed as follows.

1) Mode 1 (t_0-t_1) is shown in Fig. 5(a). The voltage V_{rec} is established at t_0. At the same time Q_s turns off. The leakage inductance of the transformer and the parasitic capacitor of the diode resonates with the clamp capacitor

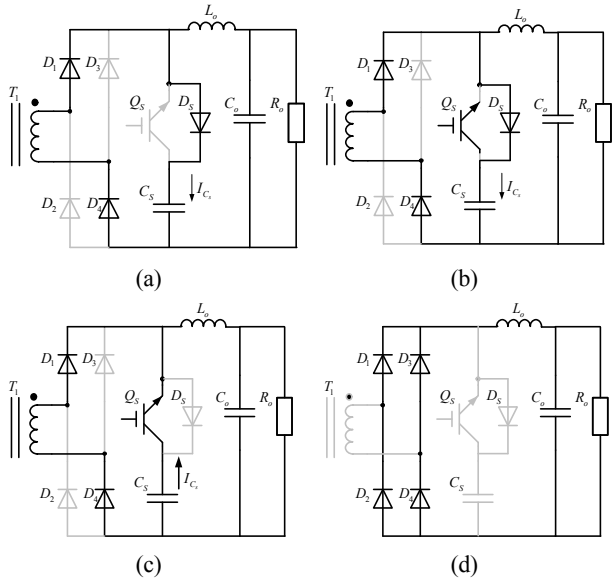


Fig. 5. Operation modes of the clamp circuit.

C_s, charging C_s at the same time.

2) Mode 2 (t_1-t_2) is shown in Fig. 5(b). Q_s turns on at t_1, and the charging current I_{Cs} drops to zero.

3) Mode 3 (t_2-t_3) is shown in Fig. 5(c). The current I_{Cs} changes its direction and gradually increases. C_s discharges at this period giving back the energy stored in mode 1 and 2 to the load.

4) Mode 4 (t_3-t_4) is shown in Fig. 5(d). V_{rec} and I_{Cs} drop to zero and Q_s is turned off.

III. The Digital Controller Design

A. Small Signal Circuit Model of a PSFB DC-DC Converter

The small-signal analysis of a PSFB converter has been carefully studied in paper [11] and paper [19]. The effective duty cycle of the transformer secondary voltage is:

$$d_{eff} = D_{eff} + \hat{d}_{eff} \tag{6}$$

Where D_{eff} is the duty of the operating point and $\hat{d}_{eff}$ is the duty cycle perturbation. $\hat{d}_{eff}$ depends on the duty cycle d of the primary voltage as well as the filter inductor current i_{LO}, the leakage inductance L_k, the input voltage V_{dc}, and the switching frequency f_s. Thus, the small-signal transfer function of this converter depends on L_k, f_s and the perturbations of the filter inductor current, $\hat{i}_{LO}$, the dc-link voltage $\hat{V}_{dc}$ and the duty cycle of the primary voltage $\hat{d}$.

The small signal circuit model of a PSFB dc-dc converter is shown in Fig. 6. The contributions of $\hat{d}_i$ and $\hat{d}_v$ are represented by two dependent sources. Here $\hat{d}_i$, $\hat{d}_v$ and R_d are represented by equation (7).

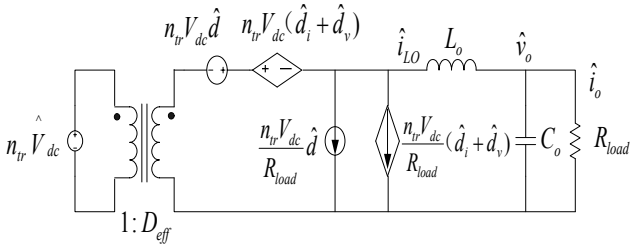


Fig. 6. Small-signal circuit model of PSFB DC-DC converter.

$$\hat{di} = -\frac{R_d}{n_{tr}V_{dc}}\hat{i}_{Lo}, \hat{d}_v = \frac{R_d i_{Lo}}{n_{tr}V_{dc}^2}\hat{V}_{dc}, R_d = 4n^2{}_{tr}L_k f_s \tag{7}$$

Thus, the open-loop transfer function is obtained as:

$$G_{vd} = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{n_{tr}V_{dc}}{s^2L_oC_o + s((L_o/R_{load}) + R_dC_o) + (R_d/R_{load}) + 1} \tag{8}$$

Where $\hat{v}_o$ is the perturbation of the output voltage. The parameters in this transfer function are listed as follows: V_{dc}= 650V, L_o= 284uH, C_o=75uF, n_{tr}=11/13, R_{load}=30Ω, f_s=20kHz, L_k=10uH, and R_d=0.573Ω. The designed PSFB converter has a phase margin of 1° and a bandwidth of 1847 Hz.

B. Self-Adaptive PI Controller Design

It is well known that switching DC-DC converters with parameter uncertainties and variable operating conditions are highly nonlinear systems. As a result, the conventional control method based on the averaging and linearization techniques will not provide good dynamic performance and can even make the system unstable [20], [21].

A self-adaptive PI control strategy is proposed here. The converter can work in either CC output mode or CV output mode as shown in Fig. 7 (a). When it is in CV mode, to make the output voltage quickly track the command voltage, the proportional factor K_p needs to vary in accordance with the actual output voltage. The proportional factor is defined as:

$$K_p = \frac{Duty}{\Delta V} \tag{9}$$

Where ΔV is the difference between the expected output voltage V_r and the actual output voltage V_o. D is defined as:

$$D = \frac{V_r}{V_{in}} \tag{10}$$

The integral factor K_I is then defined as:

$$K_I = \frac{K_P}{k} \tag{11}$$

Where k is an empirical coefficient and ranges from 3 to

30 according to the system's properties.

When the converter works in CC mode, the same way is used to define the self adaptive PI controller. Though the proposed controller is simple and effective, it is hard to determine the empirical coefficient *k* which usually requires a lot of experimental testing.

C. DSP Based Controller Design

A TMS320F2812 DSP is adopted here to serve as the control core of the system. The control block consists of two self adaptive PI controllers, two limiters and a PWM generator. v^*_o is the output voltage command; v_o is the output voltage; i^*_o is the output current command; i_o is the output current; and U' is the limited value form the limiter. Whether the PWM generator works in CC mode or CV mode is selected by the user at startup.

For voltage control, the PI voltage controller $G_{c1}(s)$ is shown in Fig.7 (b). Where $\hat{v}^*_o(s)$ is the perturbation of the output voltage command, $\hat{v}_o(s)$ is the perturbation of the output voltage, and $\hat{d}_1$ is the perturbation of the duty cycle for the transformer's primary side. The open loop transfer function $T_v(s)$ can be derived from Fig.7 (b):

$$T_v(s) = G_{c1}(s) \cdot G_{vd}(s) \tag{12}$$

The same way can be used to analyze the current PI control loop and the transfer function $T_i(s)$ can be derived from Fig.7(c):

$$T_i(s) = G_{c2}(s) \cdot G_{vd}(s) / R_{load} \tag{13}$$

For the required phase margin and bandwidth of the transfer function $T_v(s)$ and $T_i(s)$, the compensators $G_{c1}(s)$ and $G_{c2}(s)$ should be carefully designed.

The DSP hardware resources are distributed as shown in Fig.8 (a). The flow charts of the main program and the two ISRs, are depicted in Fig.8(b). The parameters and I/O initialization, the peripheral and interrupt settings and the main loop are included in the main program. The main loop deals with the procedure of self-adaptive PI control, PWM generation and the other controls in the converter. The AD interrupt service function handles the interrupt response and sampling value conversions. The AD sampling is triggered in the 25us interrupt service function, and the average values are calculated every 20 times. Then these average values are used in the self adaptive PI controller to produce the phase shift angle for the PWM generator.

D. Digitally Fulfilled Phase-Shifted Control

The duty ratios of the four switches' driving signals are 50%. The driving signals on the same arm are complementary, having a 180 degree phase lag. There is a phase lag between the leading arm and the lagging arm. The output voltage is regulated by adjusting this phase. This is the so called the phase-shifted control technique [22]-[24].

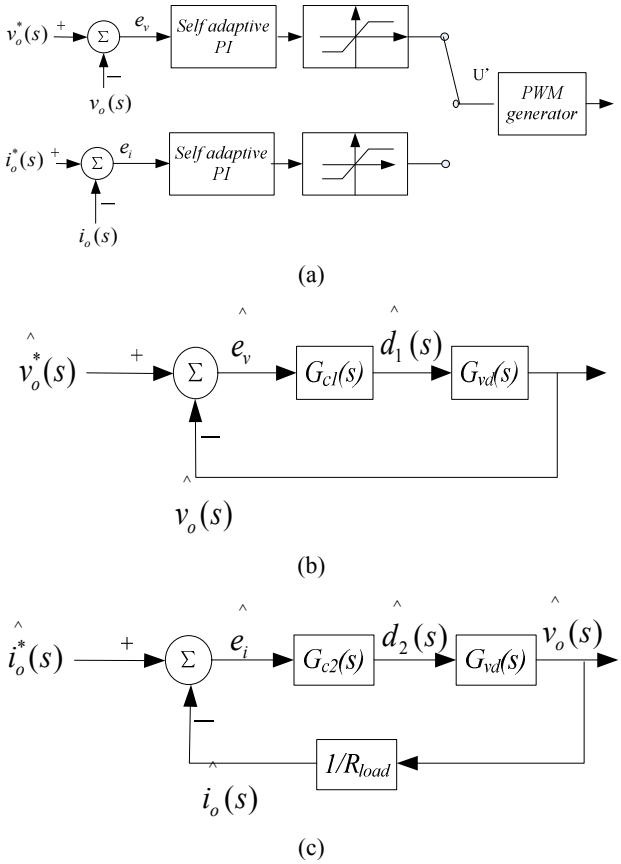


Fig. 7. Control blocks of PSFB converter. (a) Control scheme of PSFB converter. (b) Function block of voltage control. (c) Function block of current control.

A TMS320F2812 DSP controller owns two event manager modules (EVA and EVB). T_1 from EVA and T_3 from EVB are applied to generate PWM for the leading and lagging arms, respectively. T_XPR is used to configure the switching period, T_XCMP determines the duty ratio, while T_XCNT denotes the counter register values and is used to configure the phase-shifted angle.

The implementation steps include the following:

1) Configure the T_XPR and T_XCMP registers to generate two sets of PWM waves. The two PWM waves share the same switching frequency and both have a 50% duty ratio. PWM1/PWM2 are for the leading arms and PWM7/PWM8 are for the lagging arms.
2) Let the phase-shifted angle be α. Set $T_1CNT=0$ and $T_3CNT=T_3PR*\alpha/360°$ so that PWM7 lags PWM1 α degrees and PWM8 lags PWM2 α degrees.

E. Digital Realization of the Secondary Active Clamp

T_2 from the EVA module is used to create the PWM waveform for the clamp switch Q_s.

The details are represented as follows:

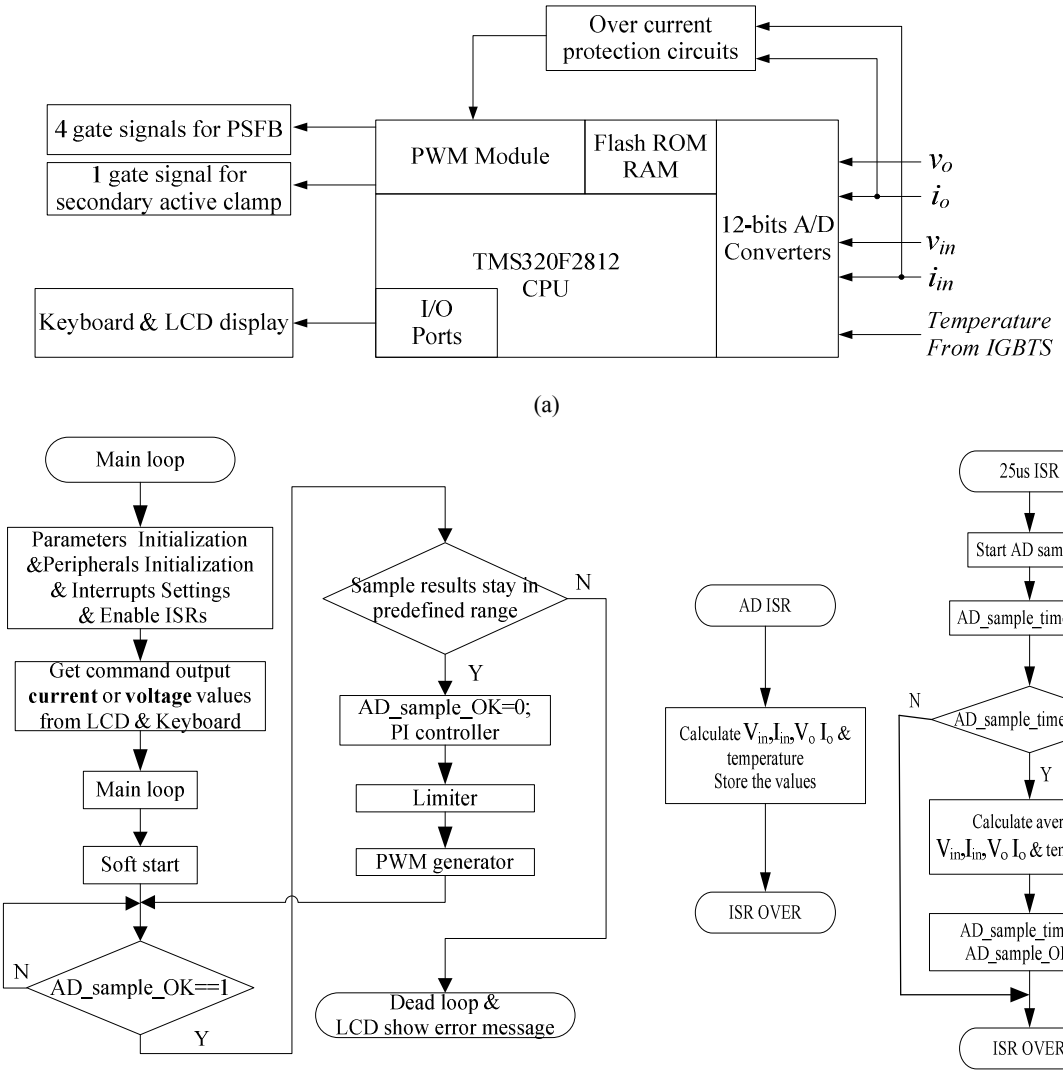


Fig. 8. DSP resources distribution and program flow chats.

1) Configure pin T_2CMP as the output pin for clamping the PWM. Make the switching frequency of T_2CMP two times that of PWM1. That is to define T_2PR =0.5* T_1PR.
2) T_2CMP's waveform should synchronize with PWM1's. That is to make: T_2CNT= T_1CNT.
3) After AD sampling, immediately update the phase angles (corresponding to registers T_1CNT and T_3CNT), the clamping PWM duty-ratio (corresponding to register T_2CMP) and the time delay factor Δt (corresponding to register T_2CMPR).

IV. Design Considerations

A. Realization of the ZVS

In order to realize ZVS in the PSFB converter, there should be enough energy to charge and discharge the paralleling capacitance in the IGBT. The criterion for ZVS is:

$$E = \frac{1}{2}LI_p^2 > \frac{1}{2}C_iV_{in}^2 + \frac{1}{2}C_iV_{in}^2 + \frac{1}{2}C_TV_{in}^2 \quad (14)$$

L is the equivalent inductance of the transformer's primary side. C_i is the junction capacitance of the leading leg (C_{lead} or lagging leg C_{lag}). C_T is the parasitic capacitance of the transformer's primary winding which is usually neglected.

The achievement of ZVS in the lagging leg is not as easy as that in the leading leg. The transformer's primary side and secondary side are coupled in the switching process as analyzed in mode 2. The inductance L_o and L_{lk} are connected in series and the current I_p remains approximately unchanged. The criterion for the leading leg's ZVS is:

$$t_{d(lead)} > 2C_{lead}V_{in} / I \quad (15)$$

Where $t_{d(lead)}$ is the dead time between Q_1 and Q_2.

The transformer's primary side and secondary side

decouple at the lagging leg's switching process. At this time only L_{lk} resonate with C_{s3} and C_{s4}. The lagging leg's ZVS is not realized if the energy stored in L_{lk} is not enough to charge C_{s3} and C_{s4}. As a result, the criterion for the lagging leg's ZVS is:

$$\frac{1}{2}L_{lk}I_p^2 > C_{lag}V_{in}^2 \tag{16}$$

Usually equation (15) is easy to satisfy but the lagging leg's ZVS realization needs carefully design.

B. Loss of Duty Cycle

The duty cycle on the transformer's secondary side (D_s) is smaller than that on the primary side (D_p). In addition, D_{loss} is the duty cycle loss.

$$D_{loss} = D_P - D_s \tag{17}$$

There are some reasons for the loss of the duty cycle: the transformer's primary side current I_p needs time to conduct from positive to negative. During this period the transformer's primary and secondary sides are decoupled. D_{loss} meets the following equation:

$$D_{loss} = \frac{t_{36}}{T_s/2} \tag{18}$$

$$t_{36} = \frac{L_{lk}[I_{t3} - I_o(t_6)/n]}{V_{in}} \tag{19}$$

$$D_{loss} = \frac{2L_{lk}[I_{t3} - I_o(t_6)/n]}{V_{in}\cdot T_s} \tag{20}$$

Time t_3, t_6 and t_{36} are expressed in Fig.2. To cope with the duty cycle loss, the saturated inductance solution is adopted here. The inductance grows to saturation when a large current flows through and exits saturation when the current drops [25].

C. Decision of Qs's Delay Time

As shown in Fig. 1, a secondary active clamp circuit has been added to the conventional PSFB converter to restrain the voltage overshot. The driving signal of the clamp switch Q_s should synchronize with the rectifier's output voltage V_{rec}. Otherwise, V_{rec} will be affected and the peak value of I_p will increase. Considering that a PSFB converter with ZVS has a duty cycle loss on transformer's secondary side, a Δt time-delay is needed to ensure that the clamp switch conducts before the arrival of V_{rec}'s rising edge. C_s has a linear charging current as shown in Fig.4. When the charging current I_c grows to zero, the voltage on the transformer's secondary side V_{rec} reaches its midpoint. Therefore, it is determined that Δt meets equation (21)

$$\Delta t \le \frac{d}{4f_s} \tag{21}$$

TABLE I
CONVERTER PARAMETERS

Maximum input voltage	650V(DC)
Maximum output voltage	500V(DC)
Nominal output power	10kW
Switching frequency	20kHz

TABLE II
SELECTIONS OF KEY COMPONENTS

DSP	TMS320F2812
IGBTs(Q1-Q4,)	F4-50R12KS4
IGBT (Qs)	FGL60N100BNTD
Diodes(D1-D4)	DSEI60-12A

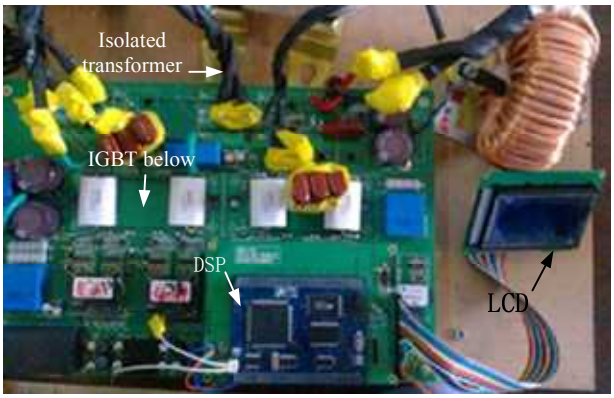


Fig. 9. A photo of the prototype (the converter's PCB board is the same size as a sheet of A4 paper).

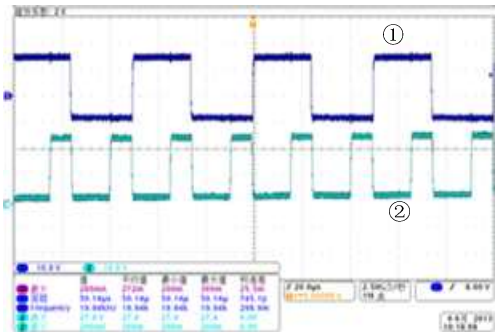
Where, d means the actual duty cycle of the voltage on the transformer's secondary side. f_s means the switching frequency of the IGBTs in a PSFB converter.

V. EXPERIMENTAL RESULTS

The digital control core is a TMS320F2812 DSP. A 10kW IGBT-based prototype has been built with the parameters listed in Table I. The selections of the IGBTs and diodes are listed in Table II. The prototype is shown in Fig.9. To test the performance of the PSFB converter, a high power switching mode DC power supply, a high power resistor and a Tektronix MSO4034 oscilloscope were applied.

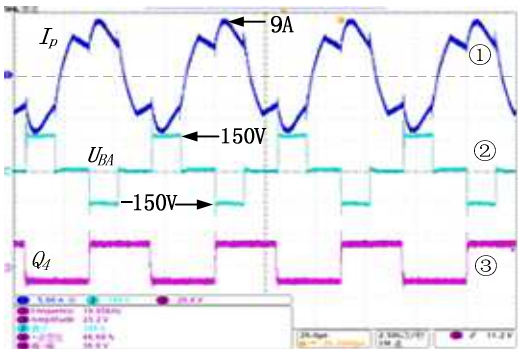
A. PSFB Converter's Operation Properties

The driving waveforms of the converter are shown in Fig. 10. The switching frequency of the IGBTs is 20 kHz and the switching frequency of the clamp switch is 40 kHz. Fig. 11 shows the voltage and current waveforms of the transformer's primary side. The current I_p and voltage V_{AB} trend is the same as the theoretical waveforms.



① PWM waveforms of Q_1 ② Active clamp switch Qs

Fig. 10. Driving waveforms.



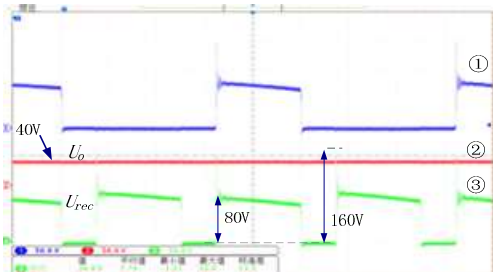
① Current waveform I_p of transformer's primary side
② Voltage waveforms U_{BA} of transformer's primary side
③ Gating signals of switch Q_4
U_{in}=300V DC V_o=160V DC R_{load}=13Ω

Fig. 11. Voltage and current waveforms of transformer's primary and secondary side.

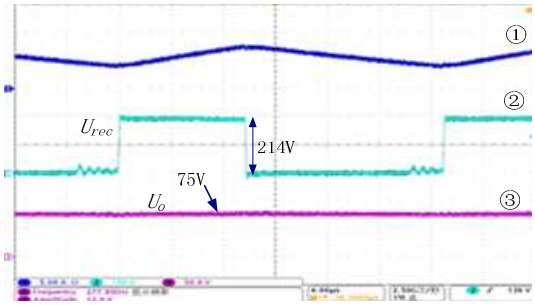
Fig. 12 depicts the effect of the secondary active clamp circuit. When the output voltage is 40V, the voltage overshoot and ringing effect on the rectifier bridge's output side can be seen clearly in Fig. 12(a). After adding the secondary active clamp circuit, the waveform is smooth without spikes or oscillations as shown in Fig. 12(b).

The converter's output waveforms are depicted in Fig.13. The converter firstly goes into the soft start. After that it is controlled by the closed-loop self-adaptive PI controller. As can be seen from Fig.13, the soft start-up lasts for 1.6 seconds and the whole start-up period is within 2 seconds without overshoots or vibrations.

The regulatory process of the conventional PI controller is about 160ms whereas that of the proposed PI controller is 97ms. The overshoot of the conventional PI controller is about 25%. However, there is hardly any overshoot with the propose PI controller. The good performance of the proposed PI controller is verified in many experiments. It has a faster respond speed, effectively suppressed vibrations and hardly any overshoot.

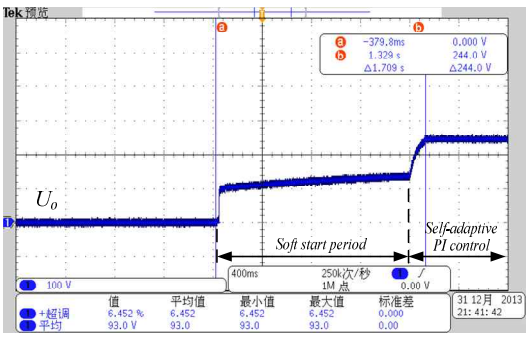


① Rectifier D_2's voltage waveform
② Converter's output voltage waveform U_o
③ Rectifier's output voltage waveform U_{rec}
U_{in}=60V DC U_o=40V DC R_{load}=13Ω
(a)



① Current waveform I_L of the output filter L_o
② Voltage waveform U_{rec} of rectifier's output side
③ Voltage waveform U_o of transformer's output
U_{in}=200V DC U_o=75 DC R_{load}=13Ω
(b)

Fig. 12. Phase-shifted full-bridge converter's output waveforms.



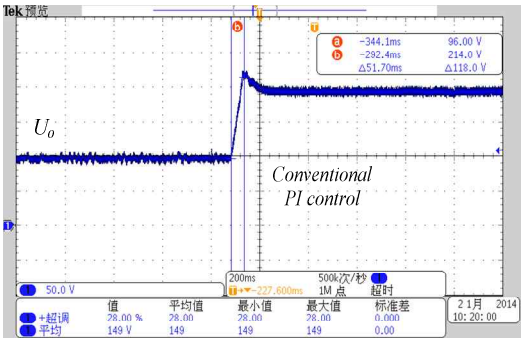
U_{in}=400V DC command U_o=245 DC R_{load}=13Ω

Fig. 13. The output waveforms of the converter.

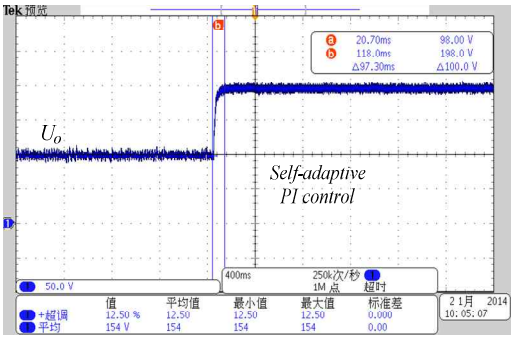
B. The Achievement of ZVS

Fig. 15 shows the waveforms of the ZVS. Fig. 15(a) shows the waveforms of the leading legs Q1 and Fig.15 (b) shows the lagging leg Q3. The waveforms of Q2 resemble Q1 and are neglected here. It is the same with Q4.

Fig.14 provides the dynamic response characteristics with the proposed self-adaptive PI controller, compared to a conventional PI controller under the same conditions.



(a) Using conventional PI controllers.



(b) Using proposed self-adaptive PI controller.

Fig. 14. Dynamic responses with 100V step voltage. (U_{in}=400V DC R_{load}=13Ω)

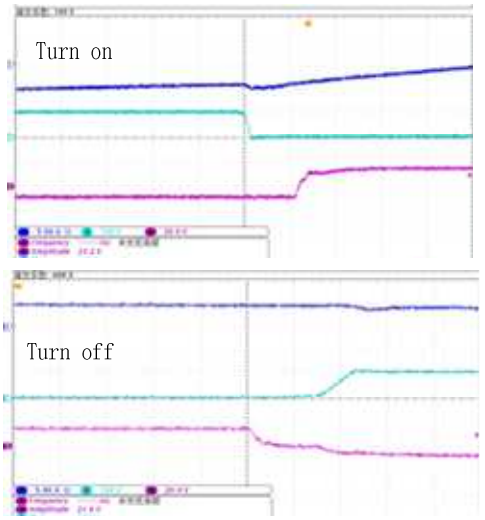
As can be seen in Fig.15, the time allowance for the leading legs' zero voltage turn-on is about 500ns and for the zero voltage turn-off it is about 200ns. The prototype achieves ZVS for the leading leg successfully which helps to reduce the switching loss and improve the converter's efficiency remarkably. The lagging leg does not achieve zero voltage turn-on because the resonant inductor L_{lk} is small and the load is light. However, it has an 800ns time allowance for the zero voltage turn-off.

C. The Converter's Efficiency

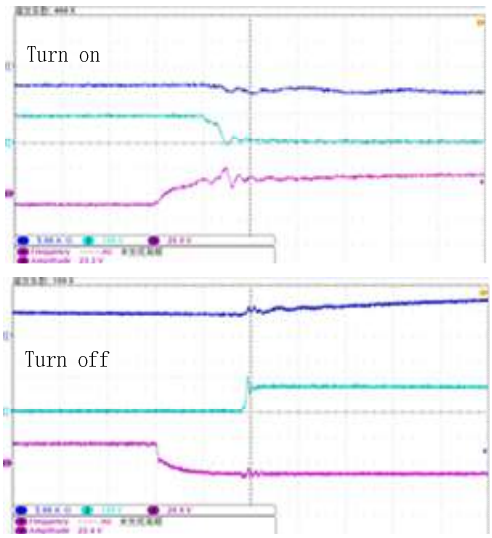
The efficiency of the converter has been tested and sketched in Fig.16. The input voltage U_{in} remained at 600V and the resistance load was 13Ω. The input current I_{in} was read from the DC source and the output voltage U_o was measured by a multi-meter. Finally the efficiency was calculated as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_o^2}{V_{in} \times I_{in} \times R} \tag{22}$$

Fig. 16 shows an upward trend of the efficiency before 6.5kW and a downward trend after about 8kW. The lowest efficiency is 0.86 when the output power level is 0.75kW while the highest efficiency is 0.945 when power level reaches 8.2kW. The efficiency stays above 0.92 after 3kW. There is a decline in the efficiency after 8.2kW. The main reason for this may be due to the fact that the converter generates a great deal of heat.



(a) Q1.



(b) Q3.

① Current I_p of transformer's primary side
② Voltage between switches' Collector & Emitter
③ Driving signals the IGBT

Fig. 15. The waveforms of ZVS.

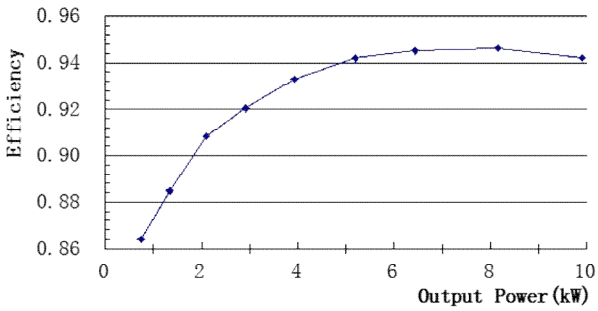


Fig. 16. PSFB converter's efficiency at U_{in}=600V & R_{load}=13Ω.

VI. CONCLUSIONS

A digitally controlled phase-shifted full-bridge DC/DC converter using a secondary active clamp has been designed and implemented in this paper. The converter's operation modes and the secondary active clamp circuit's working modes have been analyzed. The features are verified by a 10-kw IGBT based prototype. Many advantages make this converter promising for high-voltage and high-power applications. Its distinctive advantages include:

1) Simple circuit topology.
2) Achieving ZVS for the leading and lagging legs without adding any lossy components.
3) The self-adaptive PI controller provides a faster respond speed, effectively suppressed vibrations and has hardly any overshoot.

There is much more to be done with this prototype such as reducing the heat produced by the converter.

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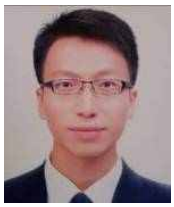

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