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Design and Fabrication of Super Junction MOSFET Based on Trench Filling and Bottom Implantation Process

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Abstract – In Super Junction MOSFET, Charge Balance is the most important issue of the trench filling Super Junction fabrication process. In order to achieve the best electrical characteristics, the N type and P type drift regions must be fully depleted when the drain bias approaches the breakdown voltage, called Charge Balance Condition. In this paper, two methods from the fabrication process were used at the Charge Balance condition: Trench angle decreasing process and Bottom implantation process. A lower on-resistance could be achieved using a lower trench angle. And a higher breakdown voltage could be achieved using the bottom implantation process. The electrical characteristics of manufactured discrete device chips are compared with those of the devices which are designed of TCAD simulation.

Keywords: Super junction MOSFET, Charge balance, Trench angle, Bottom implantation

1. Introduction

Power semiconductor devices based on silicon elements have been studied, including even the critical properties, as they have come to the fore as important parts to improve the performance for the power consumption area of electric cars and electric products. Since the power semiconductor devices have a trade-off relationship between on-resistance which is forward conducting loss resistance and breakdown voltage which is reverse blocking voltage, it is necessary to optimize the design. Since the breakdown voltage is standardized depending on the application that each device is used in, the design should be conducted in the direction of decreasing the on-resistance. To overcome the on-resistance of this electrical characteristic, Super Junction MOSFET has been proposed. When the charge balances of P region and N region is in complete agreement, Super Junction MOSFET can have a higher breakdown voltage while both P pillar region and N pillar region are fully depleted. Charge balance condition must be accompanied with SJ MOSFET due to optimization point of charge coupling structure. Thus, it can obtain a considerably lower on-resistance value than the conventional structure by raising the concentration of N pillar [1]. Though the conventional Super Junction structure have been available from CoolMOS™ fabricated in the multi-epi process [2-3], Super Junction MOSFET fabricated by using the trench filling process which can form narrower and deeper N pillar region has made an appearance [4, 17]. In comparison with the Super Junction structure fabricated in the conventional multi-epi process, Super Junction MOSFET using trench filling process can make the best use of the characteristics of elements by making more accurate charge balance. Super Junction MOSFET fabricated by using the trench filling process can get better on-resistance characteristics, unlike the multi-epi process, by changing the trench angle which is angle of silicon etching sidewall, in order to improve the on-resistance characteristics. It can be confirmed in Fig. 1. Lower trench angle can be retained wider cross-sectional area of the N pillar region than higher trench angle. In an SJ MOSFET, the effective cross-sectional area of the N pillar region has an effect on the on-resistance, because current flows through the N pillar region. Additionally, Super Junction MOSFET fabricated in the trench filling process can get the P pillar

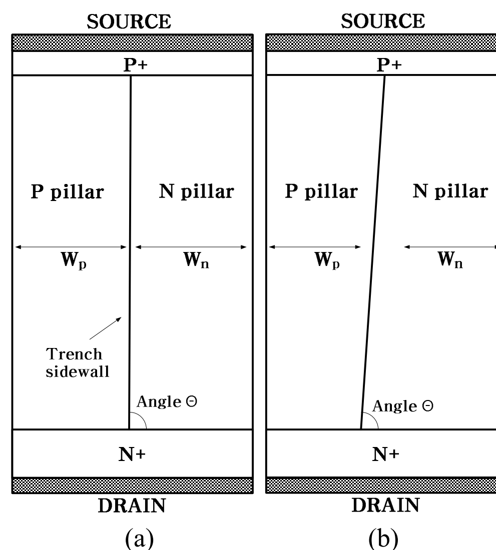

Fig. 1. Trench angle difference of super junction MOSFET: (a) higher trench angle; (b) lower trench angle

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depth above the depth etched by using the bottom implantation at P pillar bottom during P pillar trench etching prior to filling the inside of P pillar. Thus, it can get a higher breakdown voltage than the value aimed at during the design and, using this information, can raise the concentration of N pillar so that it may have a lower on-resistance value than the conventional device of not applying the bottom implantation. In this paper, after designing into a simulation Super Junction MOSFET based on the trench angle change and the bottom implantation process, the device was fabricated to compare fabrication and simulation data.

2. Electrical Characteristics of Super Junction MOSFETs

2.1 Analytic model for charge balance in super junction MOSFET

Theoretically, Super Junction MOSFET has the maximum breakdown voltage when the charge balance is in complete agreement between N pillar region and P pillar region. In case both P pillar width and N pillar width are the same, the charge balance value can be expressed in CD [%] as given by the following equation (1):

$$CD[\%] = (N_D - N_A)/N_D \times 100 \qquad (1)$$

In Super Junction MOSFET structure of Fig. 1, in case Wp and Wn are equal, theoretically, N_D, the concentration of N pillar, and NA, the concentration of P pillar, have the same values, which should give rise to the maximum breakdown voltage. As MOSFET structure is formed at the top, however, a discrepancy of about 3% is made depending on the additional amount of charge [3]. This Charge Balance modeling is simpler than other analysis [4]. Such charge balance theory was applied to Super Junction MOSFET fabricated by using the trench filling process, to analyze the electrical characteristics change of the designed Super Junction MOSFET.

2.2 The effect of trench angle on electrical characteristics change in super junction MOSFET

Super Junction MOSFET fabricated by using the trench filling process gets more limelight since the process is less expensive than the multi-epi process, can easily homonize P pillar concentration, and can easily form a high aspect ratio [4]. One of important parameters to compose Super Junction MOSFET by using the trench filling process is the trench angle. If the trench angle changes, both the breakdown voltage and the on-resistance characteristics change. Thus, in order to first understand the electrical characteristics related in the trench angle, the simulation due to the trench etching angle was conducted by using the elements of 600V Super Junction MOSFET of Fig. 1 structure. The half cell pitch of this structure is 6.5µm, and the width of P pillar and N pillar is the same, 3.25µm. The dosage of P base is $6.5 \cdot 10^{13}cm^{-2}$, and the characteristics were confirmed while N_A, the concentration of P pillar, was changed from $4.43 \cdot 10^{15}cm^{-3}$ to $6.13 \cdot 10^{15}cm^{-3}$ after N_D, the concentration of N pillar, was fixed at $4.73 \cdot 10^{15}cm^{-3}$. As shown in the graph of breakdown voltage change for the charge balance in Fig. 2, the axis of charge balance value is found to move with the trench angle. In addition, it is possible to confirm that the charge balance point, the optimum value of breakdown voltage, goes down as the trench angle decreases. If the trench angle decreases, the charge amount of P pillar region inside the real device decreases. Naturally, the breakdown voltage value at the charge balance point goes down since it is the value of the state at which the charge amount of N and P pillars is the same.

In addition, in the graph of Fig. 3, it is possible to confirm that the on-resistance decreases as the trench angle goes down. If the trench angle decreases, it is possible to confirm that the on-resistance tends to decrease while the effective cross-sectional area of N pillar region, the path for flow of current, increases. Since the specifications of the breakdown voltage are divided depending on the range of application, we should focus on the on-resistance. Since

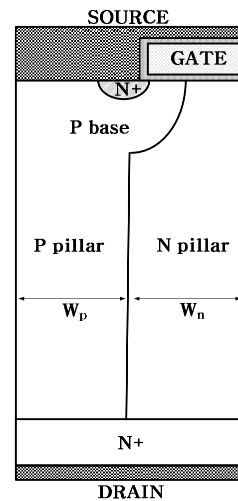

Fig. 2. Structure of super junction MOSFET

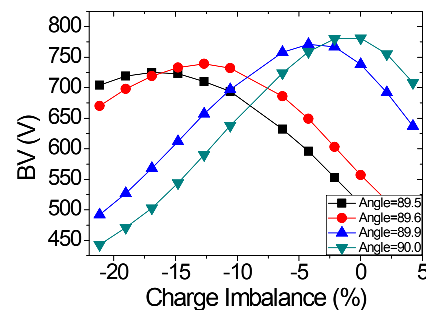

Fig. 2. Breakdown voltage characteristics of Trench angle.

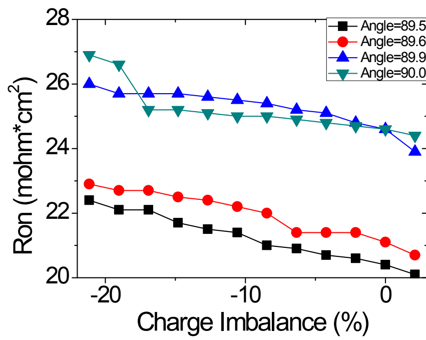

Fig. 3. On-resistance characteristics of Trench angle

the on-resistance tends to decrease as the trench angle decreases, the design should be conducted in the direction with a trench angle lower than 90 degrees. As confirmed in the simulation due to this trench angle, secured was the datum that the on-resistance value at 89.5°, the lowest angle that the process etching is possible at as the trench angle decreases, is the lowest point. Thus, for the future fabrication, the trench angle parameter was set at 89.5°. Fig. 4 shows the SEM picture of 89.5° P pillar Trench filling.

2.3 Bottom implantation process in trench filling super junction MOSFET

Super Junction MOSFET fabricated by using the trench filling process has a limit in P pillar depth since the trench depth may not be greater than the aspect ratio at which trench etching is possible in the aspect of process [5]. In order to overcome this depth limit to a certain level, the bottom implantation process was applied. The flow of this process is shown in Fig. 5. By doping boron at the bottom part after trench etching prior to progress of the trench filling process, it is possible to form a trench deeper than the P pillar depth attainable with the conventional process. In order to use a Mask during the bottom implantation after trench etching of N epi region in (a) of Fig. 5, SiO_2 deposition is made in (b) process. Since this

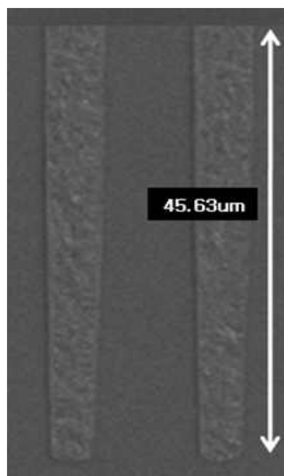

Fig. 4. SEM picture of 89.5° P pillar trench filling.

SiO_2 deposition, when seen vertically from the top, is made thicker than the real deposition thickness, this is used as the layer to prevent the characteristics from falling due to implantation toward the trench wall. The use of this oxide was proposed as a method to reduce a Mask during the bottom implantation. After this, if implantation is conducted in (c) process, boron is also implanted at N-epi top at the same time. Since this is a factor to deter the characteristics of elements, first, P doped silicon is filled inside the trench after implantation is completed. Then, the device top part which is contaminated by boron is removed by CMP process, to complete the bottom-implanted P pillar formation process. For design, the bottom implantation was applied to the structure in which the optimized trench angle secured through the simulation mentioned in the

The simulation was conducted by applying the values processwise available for the oxide thickness, implantation energy, and implantation dose required for implementation of the bottom implantation. As a result, it was possible to get a value (48 μm) deeper than the depth (46μm) of the no-bottom implanted structure. In addition, in the electrical characteristics, it was possible to confirm that, in comparison with the no-bottom implanted structure, the characteristics of the breakdown voltage rose from 671 V to 690 V, and

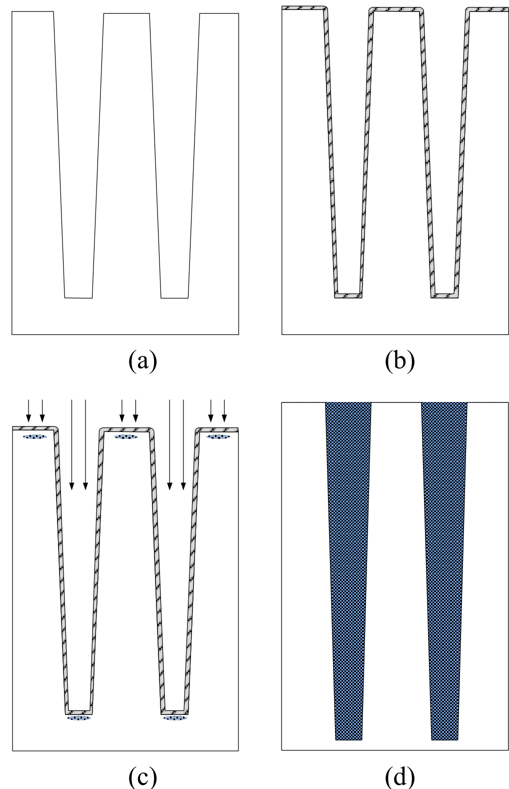

Fig. 5. Bottom implantation process in super junction MOSFET: (a) etching silicon epi layer to make Trench; (b) oxide layer deposition due to masking Trench sidewall; (c) Bottom Implantation process; (d) P type silicon filling Trench and CMP process earlier section was used.

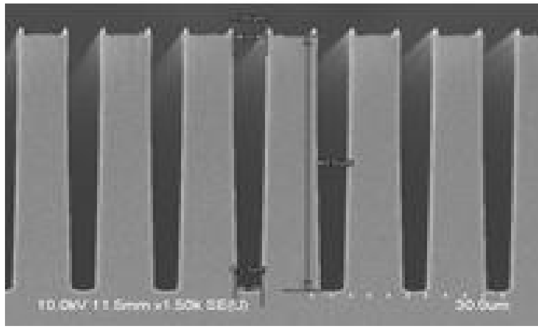

Fig. 6. SEM pictures of P pillar trench etching

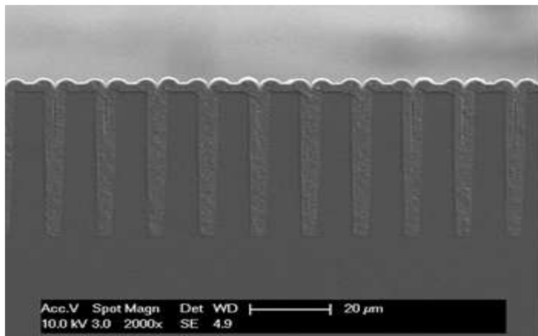

Fig. 7. SEM pictures of P pillar Trench filling

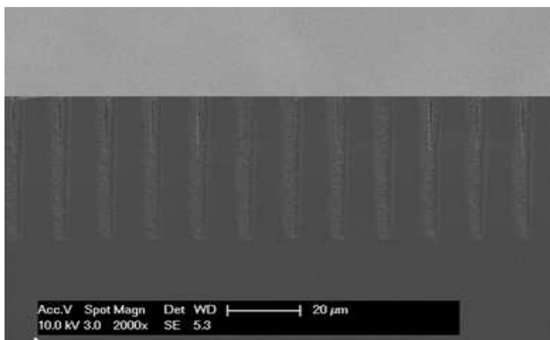

Fig. 8. SEM pictures of processing after CMP

in the on-resistance characteristic, it was confirmed that, in comparison with the no-bottom implanted structure, the acquired value (21mΩ·cm^2) was 22mΩ·cm^2 as measured data. Eventually, it was confirmed with the simulation data that the application of the bottom implantation improved the Breakdown Voltage characteristics. The SEM picture at the state of completing the process of Fig. 5 (a) is shown in Fig. 6. As shown in Figs. 7 and 8, it is possible to confirm in Fig. 7 the SEM picture at the time of completing the trench filling process just before CMP in the process of Fig. 5(d), and it is also possible to confirm in Fig. 8 the device structure with an even surface after CMP process. In the next section, the trench angle characteristic of earlier sections and the bottom implantation process were applied to comparative analysis of finding if the data obtained for direct fabrication of 2A device chip agreed with the simulation data.

3. Super Junction MOSFET Chip Data

3.1 Manufactured trench filling super junction MOSFET

On the basis of the data verified using the simulation of the previous section, a device was fabricated. As shown in the layout picture of Fig. 9, the entire area for fabrication of 1 Chip is 3180 μm · 2720 μm. The top layout of the device really fabricated may be confirmed in Figs. 10, and 11. The edge termination part excluding the active layer was fabricated by using 600V-class Super Junction Fieldring. As shown in Figs. 12 and 13, it is possible to confirm from SEM that P pillar with application of 89.5° angle and the bottom implantation is uniformly formed. The electrical characteristics of the fabricated device were measured on the spot and compared with the design data before fabrication.

3.2 Comparative analysis of simulation data and chip measurement data

The electrical characteristics of the chip fabricated were measured and the values were compared with the simulation data used for design prior to the fabrication. First of all, as confirmed in Fig. 9, the chip was fabricated with the 690V data acquired by applying, as base data for the breakdown voltage characteristics, the bottom implantation and the trench angle characteristics to the simulation, and the breakdown voltage on the fabricated

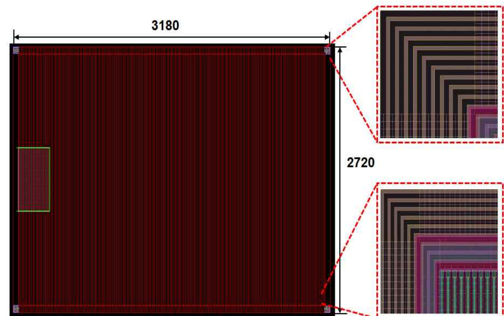

Fig. 9. 600V/2A super junction MOSFET layout.

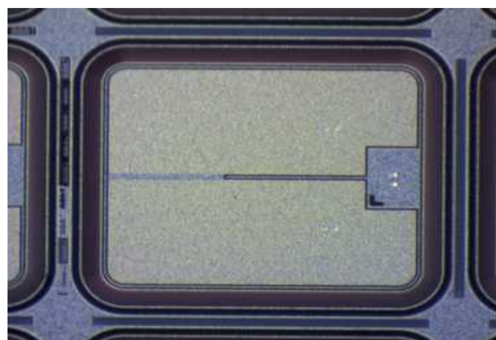

Fig. 10. 600V/2A trench filling super junction MOSFET.

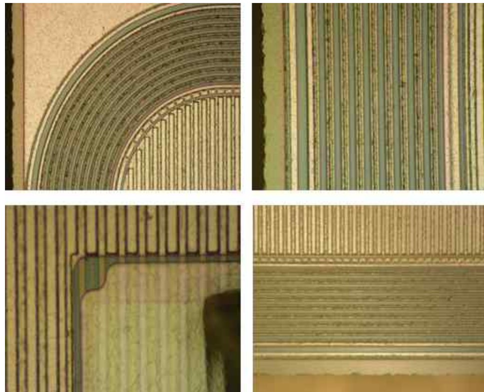

Fig. 11. Layout picture of 600V/2A trench filling super junction MOSFET.

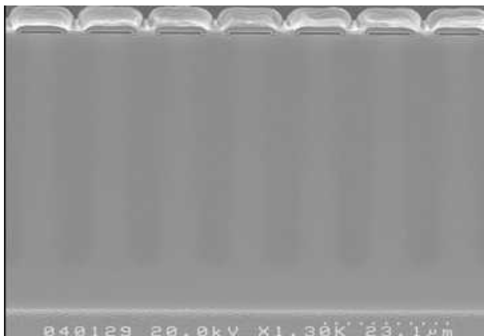

Fig. 12. SEM picture of 600V/2A Trench filling Super Junction MOSFET active area.

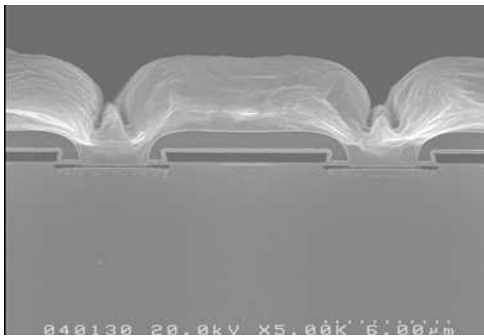

Fig. 13. Top view of SEM picture in active area

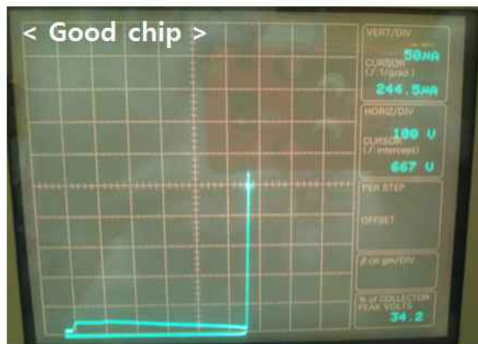

Fig. 14. Breakdown voltage measurement of 600 V/2A trench filling super junction MOSFET.

chip was measured at 667V with 5% margin of error. As for the on-resistance data, the conventional datum obtained through the simulation was 21mΩ·cm^2 and the measured datum was 22mΩ·cm2 with a low margin of error (4%). Since the margin of error for design of real power semiconductor devices is 10%, the fabricated chip was confirmed to obtain desired data in the aspects of the breakdown voltage and the on-resistance.

4. Conclusion

It is found that the on-resistance value decreases as the trench angle value, which should be considered to be an important parameter in Super Junction MOSFET fabricated by the trench filling process, goes down. The lowest on-resistance value was obtained through the simulation at the process-wise possible etch angle of 89.5°. In addition, as a method to increase P pillar depth which is limited due to the limit of the process aspect ratio, one of the disadvantages of the trench filling process, the bottom implantation was applied, and the follow-up increase in the P pillar depth and the breakdown voltage was confirmed. By using the simulation data with application of such two aspects, a discrete device chip was fabricated, and the breakdown voltage characteristic of the fabricated chip was directly measured and the results showed an error margin of about 5%. Since this value is within the basic design margin of 10% for power semiconductor devices, this chip was found to be fabricated by applying the methods of this paper well. The electrical characteristics due to the change of the variables to be considered during the bottom implantation will be analyzed for future paper.

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