Design of a CMOS Image Sensor Based on a 10-bit Two-Step Single-Slope ADC

Yeonseong Hwang and Minkyu Song

Abstract—**In this paper, a high-speed CMOS Image Sensor (CIS) based on a 10-bit two step Single Slope A/D Converter (SS-ADC) is proposed. The A/D converter is composed of both 5-bit coarse ADC and a 6-bit fine ADC, and the conversion speed is 10 times faster than that of the single-slope A/D convertor. In order to reduce the pixel noise, further, a Hybrid Correlated Double Sampling (H-CDS) is also discussed. The proposed A/D converter has been fabricated with 0.13um 1-poly 4-metal CIS process, and it has a QVGA (320 x 240) resolution. The fabricated chip size is 5 mm x 3 mm, and the power consumption is about 35 mW at 3.3 V supply voltage. The measured conversion speed is 10 us, and the frame rate is 220 frames/s.**

Index Terms—**Two-step single slope ADC, CMOS image sensor, hybrid correlated double sampling**

I. INTRODUCTION

CMOS Image Sensor (CIS) has been widely used in various applications such as digital cameras, digital camcorder, CCTV, car security cameras, medical equipment, and so on. CIS is normally composed of a pixel, a Correlated Double Sampling (CDS), an Analog-to-Digital Converter (ADC), a memory, a digital control block, and so on. Among them, ADC is the most important block to convert the analog pixel voltage into the digital code. From the view point of ADC, there exists a single channel ADC, a column parallel ADC, and a pixel ADC. Recently, a column parallel ADC is normally used at the high resolution CIS, because it has many advantages in terms of frame rate, chip area, and power consumption.

Among many kinds of column parallel ADCs, Single-Slope ADC (SS-ADC) is mostly adopted at each column of CIS due to its small chip area and low power consumption [1-6]. However, since the conversion speed of SS-ADC is very slow, the frame rate of CIS is also very low. Thus it is hard to use SS-ADC at the high speed systems like HDTV and high resolution cameras to request a frame rate of 30 frames/s or more at a high resolution. In order to overcome the disadvantage of SS-ADC, many approaches have been reported [5-9]. Among them, cyclic ADC or Successive Approximation Register(SAR) ADC are well-known technique for the high frame rate CIS. However, those methods require large chip area and huge power consumption rather than SS-ADC. Thus it is difficult to apply them for portable devices such as mobile phone, digital camera, and so on. In this paper, a two-step SS-ADC to improve the conversion speed is discussed. Because the proposed ADC is composed of both a 5-bit coarse ADC and a 6-bit fine ADC, the conversion speed is 10 times faster than that of SS-ADC. In order to minimize the Fixed Pattern Noise (FPN), further, a Hybrid Correlated Double Sampling (H-CDS) is also described. The proposed CIS has been fabricated with 0.13 um 1-poly 4-metal Samsung process, and it has a QVGA (320×240) resolution.

This paper is organized as follows. The architecture and the circuit description of the proposed CMOS image sensor are discussed in Section II and III, respectively.

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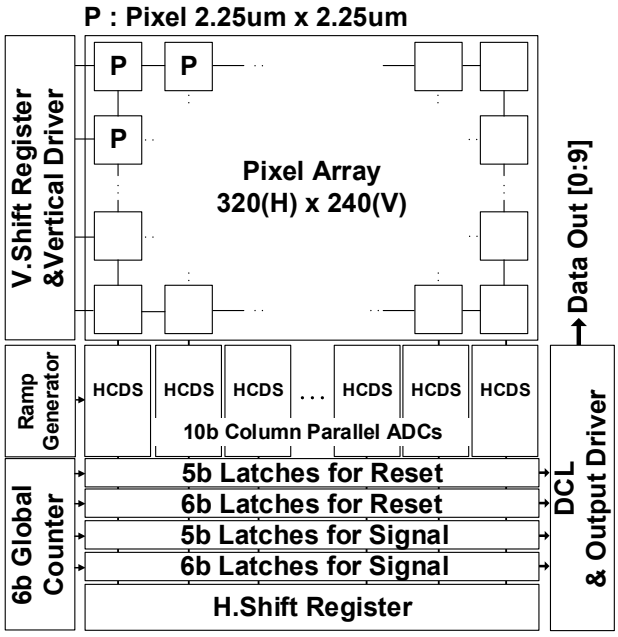


Fig. 1. The structure of the proposed CIS with two-step ADC.

The measurement results are described in Section IV. Finally, the conclusions are provided in Section V.

II. ARCHITECTURE

Fig. 1 shows the structure of the proposed CIS with a two-step SS-ADC. The proposed CIS is based on the scheme of column parallel ADC. It has a 320 x 240 QVGA resolution with a 2.25 um x 2.25 um 4–Tr Active Pixel Sensor (APS). In order to increase the minimum layout column pitch, even columns and odd column are divided into two parts of pixel array [6]. And each columns consist of a comparator, sync block, and 5-bit, 6-bit SRAM array for reset signal and pixel signal A/D conversion. Further, a 6-bit fine ramp is used to improve the boundary error of two-step SS-ADC, and a digital correction logic is also adopted to compensate the errors. Therefore, this structure consist of a 6-bit global counter, not a 5-bit global counter. By using a global counter, power consumption is reduced than using a column counter. A novel technique of hybrid correlated double sampling with a memory and a subtractor is proposed to reduce the Fixed Pattern Noise (FPN). We discuss them in section III one by one.

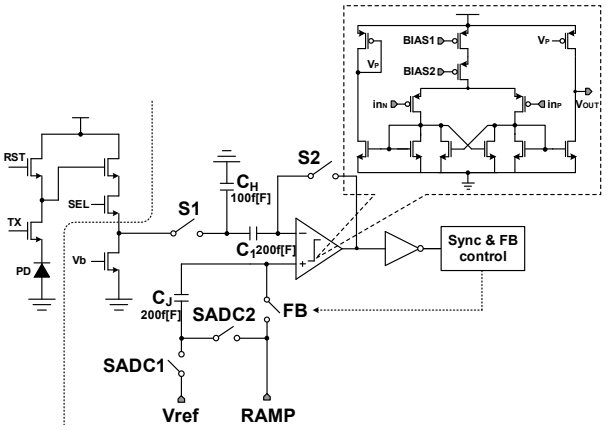


Fig. 2. Circuit diagram of a two-step SS-ADC.

III. CIRCUIT DESCRIPTION

1. The Principle of Two-step Single-slope ADC

When we implement a conventional 10-bit SS-ADC, the maximum number of counting is 1024(2^{10}). Thus the conversion time of SS-ADC is very slow. However, in case of two-step SS-ADC, only 64 ($2^5 + 2^5$) counting is enough to satisfy the 10-bit resolution, because ADC is divided into 5-bit coarse block and 5-bit fine block. Therefore, the conversion time of two-step SS-ADC is theoretically 16 times faster than that of the conventional SS-ADC. Two-step SS-ADC is suitable for high speed CIS systems [3-8]. Fig. 2 shows the circuit diagram of two-step SS-ADC. Two-step SS-ADC is normally divided into a coarse block and a fine block. A precise ramp generator is needed at each step.

Fig. 3 shows the principle and timing diagram of two-step SS-ADC. At the initial stage, a correlated double sampling between the pixel reset voltage and pixel signal voltage is starting with the switches S1, S2 and the capacitors C_H, C_1. The offset error of comparator and pixel FPN is almost removed with this CDS operation [7]. At the stage of coarse A/D conversion, then, a 5-bit resolution coarse ramp signal is driven to the comparator with the switch (SADC2) off, and the switches (SADC1, FB) on. When the pixel signal voltage and the coarse ramp voltage are the same, the output of comparator is changed and the digital code of ramp generator is stored at the first memory.

Simultaneously, the changed output of comparator turns off the switch FB. Thus the difference voltage (V_H)

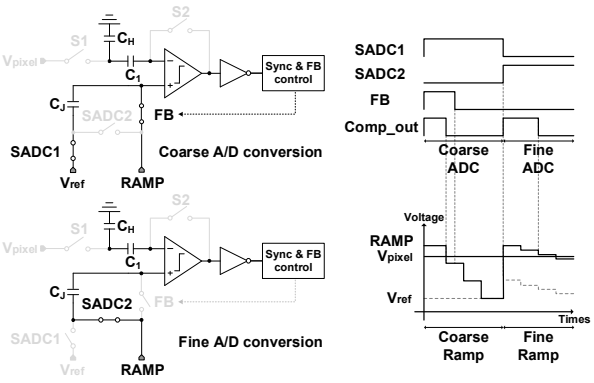


Fig. 3. Principle and timing diagram of two-step SS-ADC.

between V_{ref} and $V_{ramp.coarse}$ is stored at the capacitor C_J. Thus the coarse conversion is finished. At the stage of fine A/D conversion, a 5-bit resolution fine ramp signal is driven to the capacitor C_J with the switch (SADC2) on, and the switches (SADC1, FB) off. Since the fine ramp signal is driven to the capacitor C_J, the other side of C_J is $V_H + V_{ramp.fine}$. When the pixel signal voltage and the fine ramp voltage are the same, the output of comparator is changed and the digital code of fine ramp generator is stored at the second memory. Hence the fine conversion is finally finished.

However, some distortions of the difference voltage (V_H) are generated, due to charge injection error and clock feed through error of the switch SADC2. Fig. 4(a) shows the voltage error (V_{error}) of V_H. In this case, there exists a dead band where the comparison of fine ramp is not performed. Thus, an inevitable error is generated at the boundary of the coarse 1LSB, and SNR of two-step SS-ADC becomes lower than SS-ADC. In order to compensate the errors, as shown in Fig. 4(b), a 6-bit resolution fine ramp is used instead of 5-bit resolution ramp. The main idea of this technique is that the 1LSB voltage of coarse ramp (V_C) is added into the fine ADC block. In this case, there is no dead band where the comparison of fine ramp is not performed due to an error (V_{error}) of V_H. Therefore, the 6-bit fine ramp reduces the boundary error, as long as the maximum error is within 1 LSB of coarse ramp. Nevertheless, when the 5-bit coarse digital code (D_c) and the 6-bit fine digital code (D_f) are added, an overflow may be happened. To erase the overflow error, the digital code of half V_C is used at the digital block. This description is in Fig. 5.

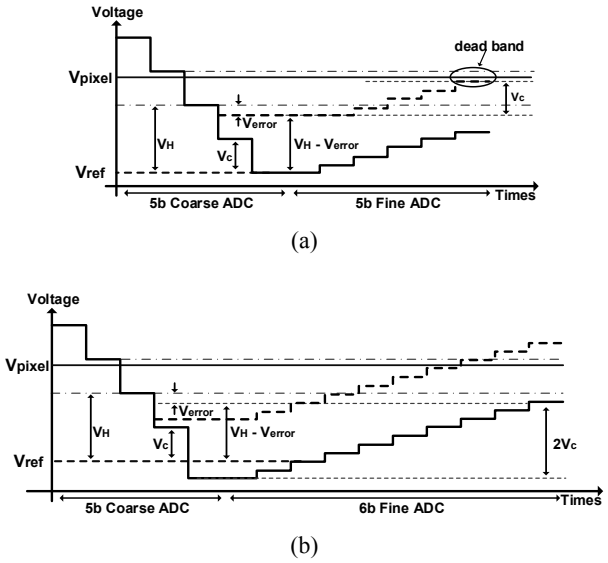


Fig. 4. (a) Error mechanism, (b) Error correction technique.

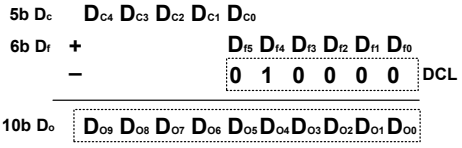


Fig. 5. Error correction algorithm at the boundary condition.

2. Hybrid Correlated Double Sampling (H-CDS)

Conventionally, an analog correlated double sampling (A-CDS) has been widely used to compensate the fixed pattern noise (FPN). However, the A-CDS has a lot of circuit noises generated from device mismatch, clock feed through error, and charge injection [9]. In this paper, a hybrid correlated double sampling (H-CDS) is discussed to reduce the circuit noises. Fig. 6 shows the timing diagram of the proposed H-CDS. Since the proposed technique includes the role of A-CDS and a new digital algorithm, we call it H-CDS. Thus H-CDS is different from a normal digital CDS.

Generally, the working procedure of H-CDS is divided into two parts, the reset mode, and the signal-capture mode. When the H-CDS is on the reset mode, the reset voltage of a pixel is converted into digital code by two-step SS-ADC. Using a 3-bit coarse ramp and 6-bit fine ramp, the digital code of reset voltage is obtained. The digital code of reset voltage is stored at the additional memory. In case of the reset mode, only 3-bit coarse ramp is enough to obtain the desired value. When the H-CDS is on the signal-capture mode, the signal voltage of

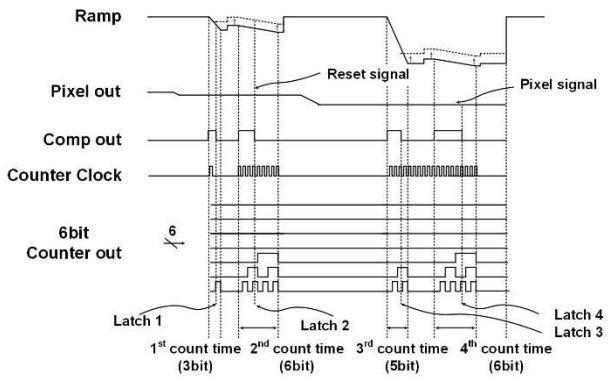


Fig. 6. Timing diagram of the proposed H-CDS.

Table 1. FPN error by Monte Carlo simulation

	Analog CDS only	Hybrid CDS
0 code error	50 %	77 %
+1 code error	19 %	10 %
-1 code error	20 %	13 %
+2 code error	6 %	0 %
-2 code error	5 %	0 %
Total average error	0.56 LSB	0.23 LSB

a pixel is converted into digital code by two-step SS-ADC. Using a 5-bit coarse ramp and 6-bit fine ramp, the digital code of signal-capture voltage is obtained.

The digital code of signal-capture voltage is also stored at the additional memory. In case of the signal-capture mode, 5-bit coarse ramp is required. Finally, the digital code of reset voltage and the digital code of signal-capture voltage are subtracted at the digital subtractor. Thus the working procedure of H-CDS is finished.

Table 1 shows the comparison data of FPN error between A-CDS only and H-CDS. The comparison data is based on the Monte Carlo simulation which makes a random mismatching at each column-parallel ADC. If all the columns are normal conditions, the output should be the same code. However, if there is a mismatch for all columns, code errors of up to ± 2 codes are generated in the case of using only the analog CDS. However, when using the H- CDS, code error is reduced to ± 1 code. As a result, the total average FPN error of H-CDS is smaller by 0.33 LSB than that of A-CDS only. Thus the FPN error of the proposed technique is smaller. Since the number of switches at the H-CDS is much smaller than that of A-CDS only, the clock feedthrough error and charge injection error are drastically reduced. Even though the chip area of H-CDS is bigger than that of A-CDS only, the proposed one has a low noise performance.

IV. Measurement Results

Fig. 7 shows the microphotograph of the proposed CIS with Samsung 0.13 um technology. The size of the chip is 5 mm x 3 mm, and the pixel resolution is 320 x 240 QVGA level. In order to use the chip area efficiently, even column and odd columns are divided into two parts. The upper side of CIS is the part of even columns, and the lower side of CIS is the part of odd columns. At the end of ADC, 5-bit / 6-bit memory are placed to satisfy the specifications of two-step single-slope ADC. Fig. 8 shows the photos of the CIS test environments. The test environments are composed of a CIS measured board with chip on board (COB) technique and a CIS control board with Xilinx-XEM3050 FPGA. The role of FPGA is generating a control input digital signal for CIS, and capturing the output signal of CIS from ADC. Then, the captured digital signals of ADC are transferred to the computer by USB interface. Finally the transferred signals are displayed at the monitor of computer. Form

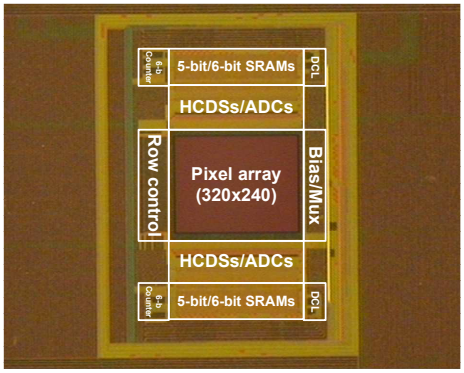


Fig. 7. Microphotograph of the proposed CIS.

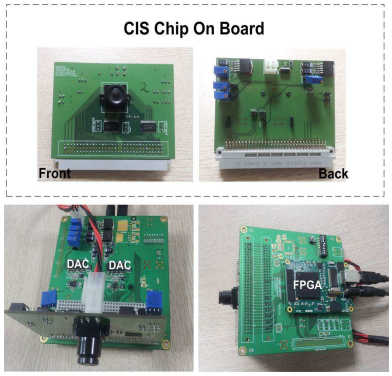
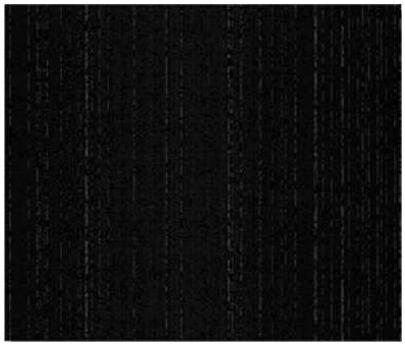


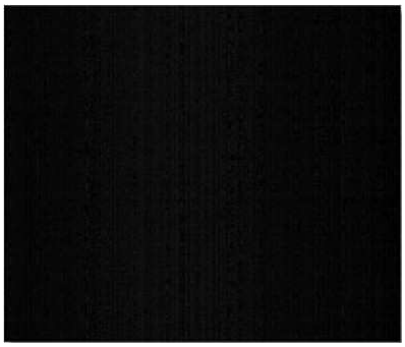
Fig. 8. CIS test environments.

the display of computer, the performance of CIS is measured.

Fig. 9 shows the measured results of the proposed CIS at a strong dark condition. Fig. 9(a) shows the measured results with A-CDS only, and (b) shows the results with H-CDS. In case of Fig. 9(a), there are many picture noises, but the noises are almost reduced at Fig. 9(b). Fig. 10 shows the measured images taken by the proposed CIS. The resolution of images satisfies the specifications of 10-bit and QVGA. The clock of CIS is 25 MHz and it has a high frame rate of 450 frames/s. Fig. 11 shows the measured column fixed pattern noise (CFPN) versus light intensity. In case of A-CDS only, the measured CFPN at the strong dark light intensity is about 1.5 LSB, and the maximum CFPN is about 5.3 LSB. The average CFPN from 0 [lux] to 500 [lux] is about 3.2 LSB. In case of H-CDS, the measured CFPN at the strong dark light intensity is about 0.8 LSB, and the maximum CFPN is about 2.7 LSB. The average CFPN from 0 [lux] to 500 [lux] is about 1.4 LSB. When we compare the average CFPN between A-CDS only and H-CDS, the average CFPN of H-CDS is reduced by about 55% than that of A-CDS only. Therefore, the proposed CIS has a performance of a low noise. Further, the measured power consumption is about 35 mW. With the 6-bit global counter to convert the reset voltage into digital code, the power consumption of proposed CIS is lower than the conventional two-step SS-ADC CIS.



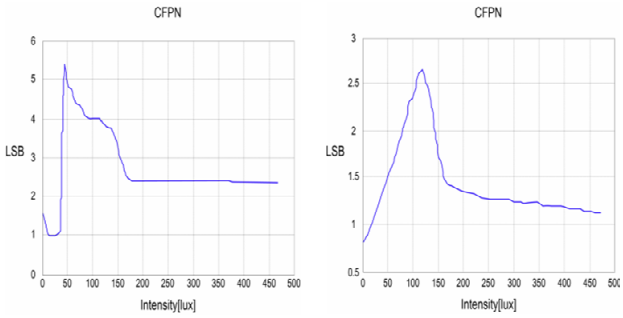
(a)



(b)

Fig. 9. The measured image at a strong dark condition (a) analog CDS only, (b) with hybrid CDS.

Fig. 10. Measured sample images (@25 MHz, 450 frames/s).



(a) (b)

Fig. 11. Measured result of CFPN vs intensity (a) A-CDS only, (b) H-CDS.

V. CONCLUSIONS

Table 2 shows the performance summary and comparison results between the proposed one and conventional two-step single-slope ADCs. Most of the performances are almost same as the conventional ones except column fixed pattern noise(CFPN). The CFPN is drastically reduced by about 55% or more, compared to that of analog CDS only. This is because the proposed H-CDS is designed with a new digital algorithm. The conversion speed of CIS with the proposed two-step single-slope ADC is 5us, while that of the conventional single-slope ADC is about 40us at 25 MHz reference clock. Thus the conversion speed of the proposed CIS is 8 times faster. Further, to improve the boundary error of two-step ADC, a novel error correction technique is also described. The technique is very useful to calibrate the errors.

Table 2. Summary of the measured performance and comparison

	[3]	[8]	This work
Pixel Resolution	400x330 pixels	320 x 240 pixels	320 x 240 pixels
Pixel size	7.4 um x 7.4 um	5.6 um x 5.6 um	2.25 um x 2.25 um
Chip size	5 mm x 5 mm	5 mm x 3 mm	5 mm x 3 mm
Dynamic range	N/A	64.8 dB	62 dB
Frame rate	142 fps	700 fps	450 fps
Column FPN	4.16 LSB	3.2 LSB	0.8 LSB
CDS Type	A-CDS only	A-CDS only	H-CDS
Power Supply	2.5 V	2.8 V	2.8 V(analog) 1.5 V(digital)
Power Dissipation	52 mW	36 mW	35 mW

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