An Enhanced Architecture of CMOS Phase Frequency Detector to Increase the Detection Range

Aby Thomas and Dr. P. T. Vanathi

Abstract—**The phase frequency detector (PFD) is one of the most important building blocks of a phase locked Loop (PLL). Due to blind-zone problem, the detection range of the PFD is low. The blind zone of a PFD directly depends upon the reset time of the PFD and the pre-charge time of the internal nodes of the PFD. Taking these two parameters into consideration, a PFD is designed to achieve a small blind zone closer to the limit imposed by process-voltage-temperature variations. In this paper an enhanced architecture is proposed for dynamic logic PFD to minimize the blind-zone problem. The techniques used are inverter sizing, transistor reordering and use of pre-charge transistors. The PFD is implemented in 180 nm technology with supply voltage of 1.8 V.**

Index Terms—**Phase locked loop, phase frequency detector, blind-zone**

I. INTRODUCTION

For the proper working of a PLL, the performance of the PFD is very crucial. The PFD detects the phase and frequency difference between the reference input signal and the VCO feedback signal to generate output pulses, whose average width is proportional to the phase difference of the two signals. The output of the PFD is fed to the charge-pump to generate the voltage signal that controls the frequency of the voltage-controlled oscillator (VCO) [1]. The advantage of PFD over the conventional phase detectors is that, it will virtually offer an unlimited pull-in range. In charge pump based PLLs; the loop gain is kept at a low value to reduce the noise sensitivity of the system. But it will increase the settling time. So the PFD should be designed in such a way to decrease the settling time and to increase the phase and frequency sensitivity [2].

The main drawbacks of a PFD are dead-zone and blind-zone. PFD based on dynamic CMOS logic, in which the output signals are used directly to reset the PFD, will virtually eliminate only dead-zone. The blind-zone causes missing edges and output polarity reversal which limits the detection range of PFDs and in turn it will deteriorate the PLL locking characteristics [3, 4].

Cheng Zhang et al. proposed a PFD architecture [5] that virtually eliminates blind-zone. The circuit diagram is given in Fig. 1. This paper presents modification of the dynamic-logic PFD proposed in [5] to eliminate the blind-zone, and hence, extend the detection range of the PFD. The various steps are inverter sizing, transistor reordering and inclusion of pre-charge transistors.

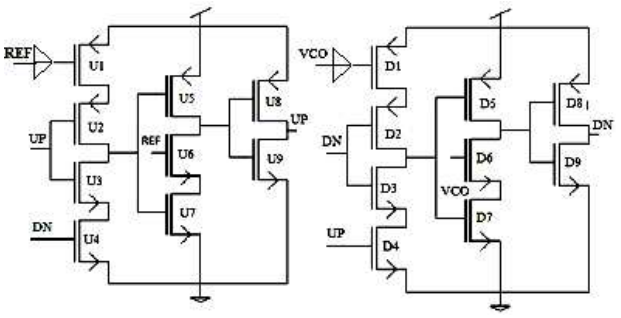

Fig. 1. Dynamic CMOS logic PFD with delay element.

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II. BLIND-ZONE ANALYSIS

The blind-zone problem occurs when the phase difference of two input signals is almost ±2π radians. The reset pulse is generated when both the UP and DOWN signals are high simultaneously. In this case, suppose, if the reference input signal is leading and its rising edge comes in the reset phase, the PFD wrongly indicates that the signal is lagging and vice-versa. It causes missing pulses and polarity reversal of the PFD output signal, in case the input phase difference is in between 2π-Δ to 2π, where Δ is blind-zone in phase domain. The relationship between the phase error and the PFD output for both ideal and real conditions are shown in Fig. 2. So during the circuit design, care should be taken to make sure that input signal rising edge does not occur during the reset phase. The blind-zone value in phase domain is Δ and it is given by Eq. (1). Here T_{rst} is the reset time of the PFD and T_{ref} is the time period of the reference input signal.

$$\Delta = 2\pi\,(T_{rst}/T_{ref}) \tag{1}$$

Using the design Eq. (1), the maximum detection range of the PFD can be obtained. It is equal to 2π (1 – Δ). In other words, the maximum detection range of a PFD, Φ_{max} can be given by Eq. (2).

$$\Phi_{max} = 2\pi\,(1 - T_{rst}/T_{ref}) = 2\pi\,(1 - T_{rst} \,.\, F_{ref}) \tag{2}$$

From the above equation it can be observed that, for increasing the detection range, either T_{rst} or F_{ref} should be reduced. As F_{ref} is not a design parameter, the only option left is to reduce T_{rst} [6].

Another point to be considered is that the pre-charge time of the internal nodes will also influence the blind-zone. For a dynamic logic circuit, the speed of operation is also determined by the pre-charge time of its internal nodes. Once the reset time is reduced to its maximum limit, pre-charge time occupies the major portion of the blind zone and so it cannot be ignored. So to increase the detection range of the PFD, the pre-charging of the internal nodes should be fast.

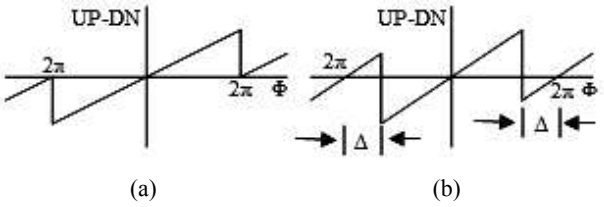

Fig. 2. Relationship with phase error and PFD output (a) Ideal, (b) Real.

III. ENHANCED PFD

The only way to increase the detection range of the PFD is to decrease the reset time of the PFD. The reset time of the PFD is actually given by the sum of the discharge time of pre-charge-node of first stage, the charging time of pre-charge-node of second stage and the discharge time of the output inverter. During the reset operation, the PFD can be considered as cascade connection of three inverter stages. It consists of transistors U2-U3 (D2-D3), U5-U6 (D5-D6) and U8-U9 (D8-D9). So by proper inverter sizing, the inverter delay is reduced [7]. The inverter sizing factor 'f' selected is 1.3. This will decrease the reset time and in turn increase the detection range of the PFD.

The next step is the modification of the circuit architecture to reduce the signal path length. This will increase the speed of the PFD. Looking into the circuit diagram given in Fig. 1; it can be observed that the transistor U6 (D6) causes increase in capacitance and resistance in the signal path. This will cause excess delay in the circuit which increases the reset time. By interchanging the transistors U6 and U7 (D6 and D7), the signal path length is reduced because the resistance and capacitance U6 (D6) will not come in the signal path. This will reduce the delay of the circuit and in turn, the reset time.

As the final step, pre-charge transistors are included to further increase the detection range of the PFD. Once reset operation is done, fast pre-charging of the internal nodes is to be done. At present, the pre-charging is done with only one transistor U1 (D1) with a delayed input signal. This will delay the pre-charging of the internal nodes. In order to rectify this problem, a pre-charge transistor U10 (D10), can be connected to the direct input signal as shown in Fig. 3. Thus even faster pre-charging of the internal nodes is achieved. This will further decrease the blind-zone. The only overhead of adding extra pre-charge transistors is increased area. The W/L ratio of the final circuit is given in Table 1.

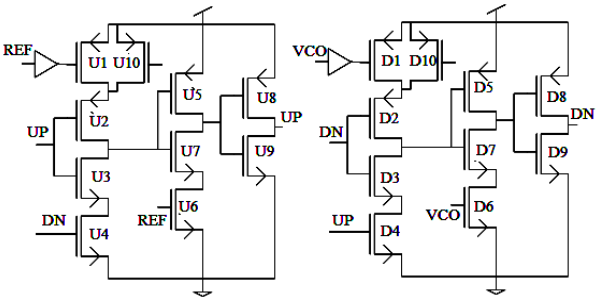

Fig. 3. PFD with pre-charge transistors (PFD T).

Table 1. W/L ratio of the final PFD

Transistor	W/L ratio	Transistor	W/L ratio
U1, D2, D1,D2	720 nm/180 nm	U8, D8	1200 nm/180 nm
U3, U4, D3, D4	240 nm/180 nm	U9, D9	410 nm/180 nm
U5, D5	940 nm/180 nm	U10, D10	720 nm/180 nm
U6, U7, D6, D7	320 nm/180 nm		

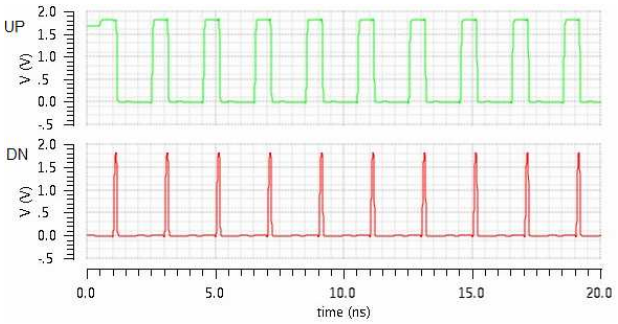

Fig. 4. UP and DN signals of the PFD T.

IV. Simulation Results

The five configurations of the PFD implemented are; PFD without delay (PFD P) [5], with delay (PFD Q) [5], with delay & inverter sizing (PFD R), with delay & inverter sizing & transistor re-ordering (PFD S) with delay & inverter sizing & transistor re-ordering & pre-charge transistors (PFD T). The PFDs are simulated with 500 MHz input using Cadence SpectreRF simulator in CMOS 180 nm technology with a supply voltage of 1.8 V. The UP and DN signals of the PFD is shown in the Fig. 4.

The waveform of the reset signal for different PFDs is shown in Fig. 5. For PFD P, the reset time is 146 ps. By introducing the different techniques, the reset time is reduced to 123 ps (PFD T). It is observed that the reset time has decreased much and thus the detection range of the PFD is improved. The amount of reduction in reset time is shown in Table 2.

Table 2. Reset time of the PFDs.

PFD	PFD P[5]	PFD Q[5]	PFD R	PFD S	PFD T
ResetTime(ps) @ 500 MHz	146	135	132	126	123
% of decrease	-	7.5	9.6	13.7	15.75

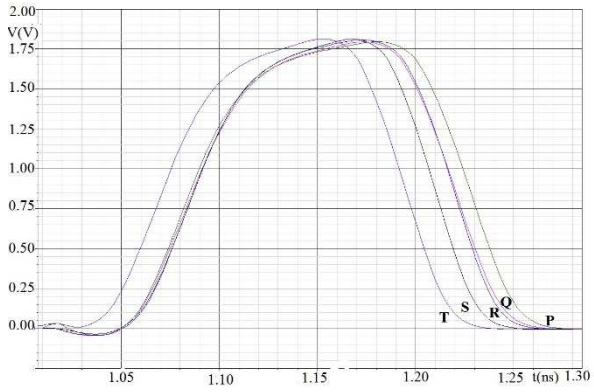

Fig. 5 Waveform of the reset signal for different PFDs.

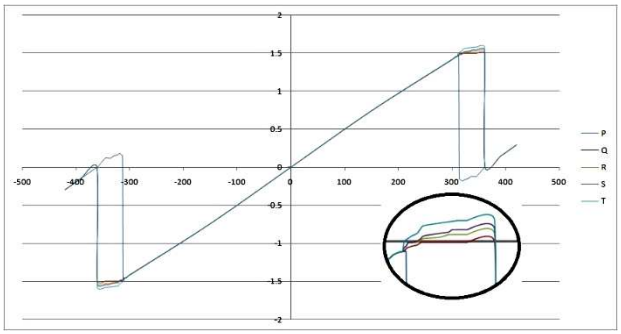

Fig. 6. UP-DN Vs Phase error plot of the PFDs.

The plot between UP – DN and phase error is given in the Fig. 6. From the figure it is seen that, for PFD P, there is a polarity reversal of the output. This is because the rising edges of the reference and VCO signals are occurring during the reset period. This will make the PFD to interpret the leading signal as lagging and vice-versa. Other PFDs doesn't have polarity reversal as the reference and VCO signals are pushed out of the reset period and also the UP-DN signal magnitude is increasing for higher values of phase error.

With the decrease in reset time the detection range of the PFD has increased. This is shown in the Table 3. From PFD P to PFD T, there is a continuous increase of 25.75^0 in the detection range.

All the five configurations of the PFD were simulated with different input frequencies. The plot for the detection range with different input frequencies is shown

Table 3. Detection range of the PFDs.

PFD	PFD P[5]	PFD Q[5]	PFD R	PFD S	PFD T
Detection range @ 500 MHz	312.2^0	321^0	335^0	337.25^0	338^0
% of improvement	-	2.8	7.3	8.0	8.3

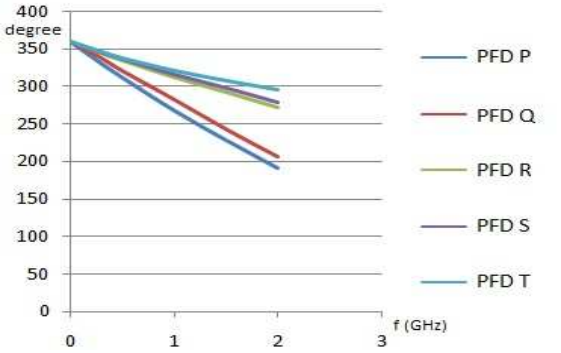

Fig. 7. Detection range with different input frequencies.

in the Fig. 7. It can be seen from the figure that the PFD T has maximum detection range, when compared with the other PFDs.

IV. CONCLUSION

This paper presents an enhanced dead-zone free PFD with near zero blind-zone. With the proposed modifications, the detection range of the PFD has increased about of 25.75^0 and this will in turn accelerate the PLL acquisition process. It will also reduce the settling time for large frequency steps in frequency synthesizer applications. The maximum theoretical input frequency has been increased by about 1 GHz by the enhanced architecture.

REFERENCES

[1] R.E.Best, Phase-locked loops: Design, Simulation and Applications, 4/e McGraw-Hill: New York, US, 1999.

[2] S.Soliman, F.Yuan and K.Raahemifar, "An overview of design techniques for CMOS phase detectors," IEEE Int Sym Circuits and Systems, May 2002 Pages:V-457 - V-460.

[3] G.B.Lee, P.K.Chan and L.Siek, "A CMOS Phase Frequency Detector for Charge Pump Phase-Locked Loop", Proc IEEE Midwest Symp on Circuits and Systems, 1999.

[4] S.Li and M.Ismail, "A High-Performance Dynamic_logic Phase- Frequency Detector", Chapter 28, C. Toumazou, G. Moschytz and B. Gilbert, Trade-offs in analog circuit design: the designer's companion, Kluwer Academic Publishers, 2002.

[5] Cheng Zhang, and Marek Syrzycki, "Modifications of a Dynamic-Logic Phase Frequency Detector for Extended Detection Range" 53rd IEEE Int Midwest Symposium on Circuits and Systems, Aug. 2010, Pages 105 – 108.

[6] T.Johnson, A.Fard and D.Aberg, "An Improved Low Voltage Phase-Frequency Detector with Extended Frequency Capability", Proc IEEE Midwest Symposium on Circuits and Systems, 2004.

[7] J.M.Rabaey, A.Chandrakasan and B.Nikolic, Digital integrated circuits 2/e: a design perspective, Pearson Education, New Jersey, 2003.

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