A 12b 100 MS/s Three-Step Hybrid Pipeline ADC Based on Time-Interleaved SAR ADCs

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Abstract—**This work proposes a 12b 100 MS/s 0.11 μm CMOS three-step hybrid pipeline ADC for high-speed communication and mobile display systems requiring high resolution, low power, and small size. The first stage based on time-interleaved dual-channel SAR ADCs properly handles the Nyquist-rate input without a dedicated SHA. An input sampling clock for each SAR ADC is synchronized to a reference clock to minimize a sampling-time mismatch between the channels. Only one residue amplifier is employed and shared in the proposed ADC for the first-stage SAR ADCs as well as the MDAC of back-end pipeline stages. The shared amplifier, in particular, reduces performance degradation caused by offset and gain mismatches between two channels of the SAR ADCs. Two separate reference voltages relieve a reference disturbance due to the different operating frequencies of the front-end SAR ADCs and the back-end pipeline stages. The prototype ADC in a 0.11 μm CMOS shows the measured DNL and INL within 0.38 LSB and 1.21 LSB, respectively. The ADC occupies an active die area of 1.34 mm^2 and consumes 25.3 mW with a maximum SNDR and SFDR of 60.2 dB and 69.5 dB, respectively, at 1.1 V and 100 MS/s.**

Index Terms—**Analog-to-digital converter (ADC), pipeline, time-interleaved, hybrid, SAR ADC**

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I. INTRODUCTION

The development of multimedia consumer electronics and communication systems enables the implementation of high-definition (HD) quality videos on mobile devices. Those systems require essentially analog-to-digital converters (ADCs) with a resolution of 12b level and a conversion rate exceeding 75 MS/s to convert analog signals including RGB information into digital signals. Pipeline ADCs have been used to meet these specifications [1-5]. In the conventional pipeline ADCs, a dedicated input sample-and-hold amplifier (SHA) has been employed to reduce a sampling-time mismatch between the first-stage multiplying digital-to-analog converter (MDAC) and the flash ADC. For low power and small chip area, various SHA-free pipeline ADCs have been proposed [6-12]. However, previously reported SHA-free ADCs partially resolve the problems by a sampling-time mismatch with extra digital logic or inventive layout techniques for sampling networks.

Successive-approximation register (SAR) ADCs properly process high-frequency input signals without a SHA due to the built-in sample-and-hold function. However, the internal clock speed for the SAR logic is proportionally increased with a required resolution. In conventional 12b SAR ADCs, the internal clock operates 13 times as fast as the conversion rate of the overall ADC. The resulting insufficient sampling, holding, and signal-settling times strictly limit the conversion rate [13-16]. Meanwhile, since the number of capacitors in the SAR ADCs is increased exponentially with a resolution, a unit capacitor size needs to be scaled down to reduce the die area. But using a small unit capacitor leads to linearity

degradation, caused by the parasitic capacitance and capacitor mismatch [13]. Recently, a two-step pipelined SAR ADC has been proposed to overcome the limitations of conversion rate and linearity, but it is still difficult to apply directly to high-speed conversion [17].

The proposed 12b 100 MS/s hybrid pipeline ADC employs dual-channel time-interleaved 4b SAR ADCs in the front-end stage for 4 most significant bits (MSBs) while single-channel pipeline back-end stages decide 8 least significant bits (LSBs). The dual-channel and time-interleaving configuration with a 4b resolution enables the SAR ADCs properly to process the Nyquist-rate input without a SHA during a half clock period of 100 MHz level. The proposed ADC employs and shares only one amplifier for the residue amplifiers of the first-stage SAR ADCs as well as the MDAC of the remaining pipeline stages. Particularly, the shared residue amplifier for the dual-channel SAR ADCs reduces performance degradation due to offset and gain mismatches between the channels with small chip area and low power consumption.

The input sampling clock for the dual-channel SAR ADCs is synchronized to a reference clock to minimize a sampling-time mismatch. However, the different operating frequencies of the front-end SAR ADCs and the back-end pipeline stages can result in disturbance of on-chip reference voltages. The reference disturbance is considerably relaxed by separating only reference voltage drivers, while other reference current and voltage functional blocks are shared to minimize a mismatch between two reference voltages. On-chip clock circuits generating 400 MHz for the SAR ADCs are internally implemented for various system applications.

This paper is organized as follows. The architecture and operation of the proposed hybrid pipeline ADC are briefly described in Section II. The proposed design techniques and detailed circuit implementation are discussed in Section III. The measured results of the prototype ADC are summarized in Section IV and the conclusion is given in Section V.

II. ARCHITECTURE

The proposed 12b 100 MS/s three-step hybrid pipeline ADC based on time-interleaved SAR ADCs is shown in Fig. 1. The proposed ADC consists of two 4b SAR ADCs, a single shared amplifier, 4b and 6b flash ADCs (FLASH1, FLASH2), a 4b MDAC, a digital correction logic (DCL), on-chip current and voltage references, a timing circuit, and an on-chip clock generator. The internally generated 400 MHz clock is used for SAR operation of the 50 MS/s SAR ADCs, to decide 4b digital codes during a half period of 50 MHz. The 4b 50 MS/s digital codes from the first-stage dual-channel SAR ADCs are combined into 4b 100 MS/s digital codes in the DCL.

An interpolation technique is applied to both of the two flash ADCs, and a two-step reference selection scheme is used in the back-end FLASH2 to enhance power efficiency and reduce chip area [18, 19].

The timing diagram of major circuit blocks such as SAR ADCs, an MDAC, and a shared amplifier is shown in Fig. 2. Since the first stage of the proposed ADC is implemented as the SAR ADCs with dual-channel, time-interleaving, and 4b-resolution characteristics, there is enough room for sampling and holding times compared to the conventional single-channel high-resolution high-speed SAR ADCs.

The shared amplifier operates for the second-stage

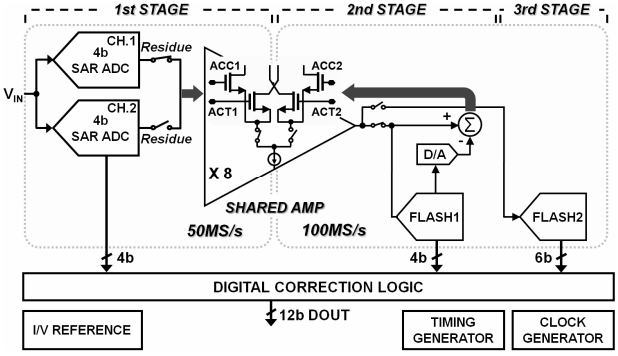


Fig. 1. Proposed 12b 100 MS/s hybrid pipeline ADC.

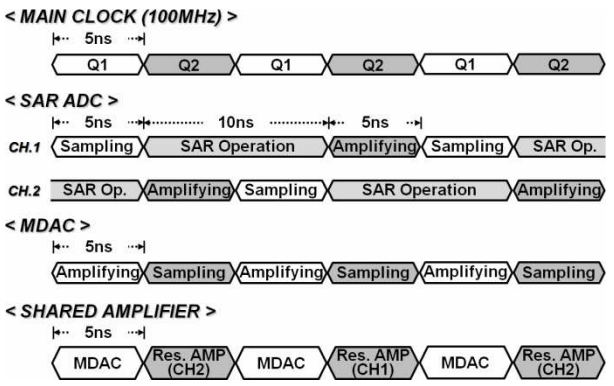


Fig. 2. Timing diagram of major functional circuit blocks.

MDAC during every Q1 phase, and as residue amplifiers for the first-stage dual-channel SAR ADCs alternately during Q2 phase. Since a single amplifier with the same operating condition is shared for residue amplification of the dual-channel SAR ADCs, performance degradation caused by offset and gain mismatches between channels is minimized.

Each channel of the SAR ADCs samples an analog input during Q1 phase by turns and converts the sampled analog input to 4b digital codes through SAR operation. A residue voltage of the first-stage SAR ADC is generated after SAR operation. The shared amplifier amplifies this residue voltage by 8, and transfers it to the second-stage FLASH1 and MDAC during Q2 phase. The other processes are the same as the conventional pipeline ADCs.

III. CIRCUIT DESCRIPTION

1. Proposed Time-Interleaved SAR ADCs

For sufficient sampling and holding times at 100 MHz, time-interleaved dual-channel SAR ADCs are employed in the first stage of the proposed ADC, as shown in Fig. 3.

The performance of time-interleaved ADCs tends to be degraded by a sampling-time mismatch between channels. To solve this drawback, the proposed SAR ADCs employ a single clock-edge sampling scheme which synchronizes the falling edge of a sampling clock in each channel with an external 100 MHz reference clock. A clock skew between the external 100 MHz reference clock and the internally generated 50 MHz clock is relaxed by well-matched symmetrical layout and circuit design strategy, instead of using additional delay control circuits as discussed in [20]. In addition, two pairs of reference voltages are selectively used for stable operation of the reference voltage circuits; one reference voltage pair (REFT_SAR, REFC_SAR) for low-resolution and high-speed SAR operation, the other (REFT_MF, REFC_MF) for high-resolution and nominal-speed residue amplification.

The input switches of the first-stage SAR ADCs with a gate-bootstrapping circuit sample a front-end analog input signal with low distortion and minimize a sampling mismatch between two channels. By adopting a pipeline topology at the back-end stages, the first-stage SAR ADCs only handle a 4b resolution. Thus, the number of the required unit capacitors is much smaller than that of the conventional high-resolution SAR ADCs. As a benefit of using the pipeline architecture, a sufficient large unit capacitor (100 fF) is used, considering the kT/C noise, instead of using an excessively small-sized unit capacitor for small chip area. As a result, the potential linearity degradation coming from the capacitor mismatch and parasitic capacitance of the SAR ADCs is alleviated.

A 400 MHz high-speed clock is needed in the proposed dual-channel SAR ADCs to decide 4b digital codes during a half period of a 50 MHz clock. The 400 MHz clock is internally generated by the on-chip clock generator, as shown in Fig. 4. Based on the 1/2 frequency divider, a 50 MHz clock, CKIN, is generated and synchronized to an external 100 MHz main clock. For the required SAR operation, a 400 MHz clock, CK_INT, is created by the CKIN, two simple delay cells of VDL1B and VDL2, and some digital logic gates. The 3b counter terminates clock generation immediately after detecting the fifth rising edge of the CK_INT, which

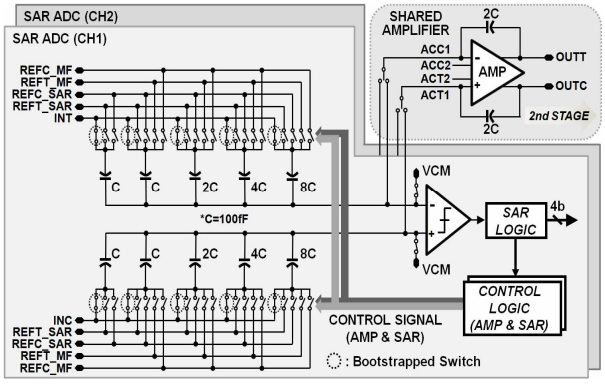


Fig. 3. Time-interleaved dual-channel SAR ADCs.

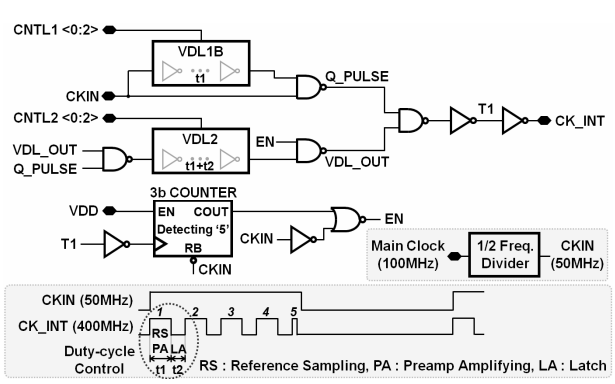


Fig. 4. Proposed on-chip clock generator for 4b SAR ADCs.

indicates the completion of SAR operation. Moreover, a reference-sampling (RS) and preamp-amplifying (PA) time, t_1, is configurable with the CNTL1<0:2>, while a time interval of the CK_INT, t_1+t_2, is controlled with the CNTL2<0:2> for more stable SAR ADC operation.

2. Single Shared Amplifier for two SAR ADCs and one MDAC

The shared amplifier in the proposed ADC has a two-stage folded-cascode topology with a swing range over 1 Vp-p, a high DC gain, and two input differential pairs to properly deal with three operation modes, as shown in Fig. 5. The three operation modes consist of two residue amplifications for the SAR ADCs and one residue amplification for the MDAC.

The matching characteristic is not so much critical between residue amplifiers in the first stage and an amplifier of the second-stage MDAC. However, the mismatch between two residue amplifiers in the first-stage SAR ADCs can cause some serious performance degradation. The mismatch in the time-interleaving structures primarily consists of offset and gain mismatches of amplifiers [8]. The problems are fairly removed in the proposed ADC by sharing a single amplifier with the same input differential pair. In the common case of using three input differential pairs for three different operation modes of two SAR ADCs and one MDAC, separate 50 MHz clock lines and switches are required to select each input pair with separate feedback capacitors. In the proposed ADC, only two input differential pairs are employed in the amplifier for three operation modes; one shared input differential pair for residue amplifications of the dual-channel SAR ADCs in the first stage (ACC1, ACT1), and the other input differential pair for the second-stage MDAC (ACC2, ACT2), as shown in Figs. 3 and 5. No more extra circuit is required in the shared amplifier, minimizing the mismatch that may occur between two channels. The input differential pairs of the shared amplifier are turned on and off alternately, by using the switches with slightly overlapped clocks, Q1B and Q2B, to prevent the input differential pairs from turning off simultaneously.

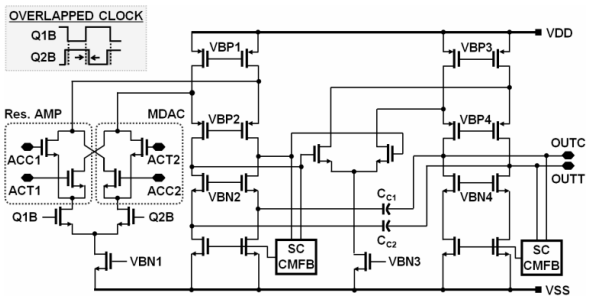


Fig. 5. Shared two-stage amplifier of the proposed ADC.

3. On-chip Reference with Separate Drivers to Isolate High-speed Switching Noise from the SAR ADCs

The proposed hybrid pipeline ADC operates with two different clock frequencies; one for the dual-channel SAR ADCs with high-speed operation of 400 MHz, and the other for residue amplifications with high-resolution and nominal-speed operation of 100 MHz. In the case of sharing a single reference voltage, as observed in usual pipeline ADCs, a reference disturbance problem can occur due to high-speed SAR switching noise during residue amplification, as shown in Fig. 6(a). The reference voltage during residue amplification needs to be settled within a half LSB of a 12b resolution in a half period of a 100 MHz clock. However, the switching noise by high-speed operation of the SAR ADCs directly affects the reference voltage for residue amplification. The proposed separate reference voltage techniques considerably reduce the reference disturbance, as shown in Fig. 6(b).

To minimize the mismatch between the reference voltages for SAR operation and residue amplifications, a current reference generator (IREF) and a level shifter are

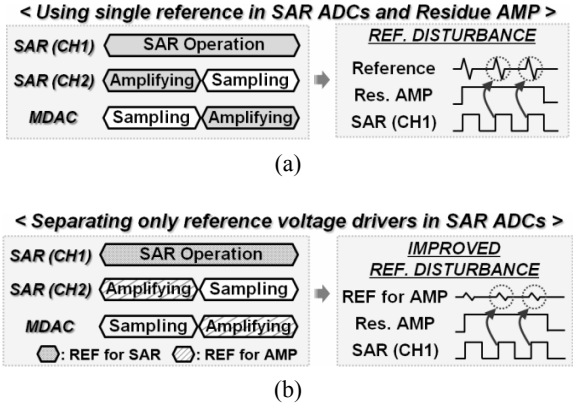


Fig. 6. On-chip reference with using (a) a single reference voltage, (b) separating reference voltage drivers.

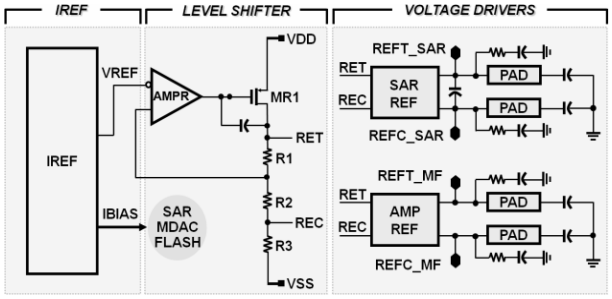


Fig. 7. On-chip reference circuit with separate voltage drivers.

shared, and only reference voltage drivers are separated, as shown in Fig. 7. The signal settling targets of the reference voltages for the SAR ADCs and the MDAC are much different, which are a 4b accuracy at 400 MHz and a 12b accuracy at 100 MHz, respectively. Considering the different operation targets, apart from a small-sized on-chip RC filter at each reference output node, an extra decoupling capacitor of 150 pF is added between the output nodes, REFT_SAR and REFC_SAR, of the reference voltage drivers for high-speed SAR operation.

IV. MEASUREMENT RESULTS

The prototype 12b 100 MS/s ADC is implemented in a 0.11 μm CMOS technology, as shown in Fig. 8. The ADC occupies an active die area of 1.34 mm^2, including on-chip MOS decoupling capacitances of 500 pF to stabilize supply and reference voltages. The proposed dual-channel SAR ADCs are laid out adjacently and symmetrically to minimize not only offset and capacitor mismatches, but also a sampling-time mismatch between channels without any calibration scheme.

An evaluation board to measure the performance of the prototype ADC is shown in Fig. 9. Passive filters and a transformer are employed just before an analog input terminal of the ADC to reduce the undesired noise and harmonics of a signal generator and to convert a single-ended input signal into a differential signal. Separate power supplies for analog and digital circuits are used to minimize the signal interference caused by the digital supply noise. The prototype ADC dissipates 25.3 mW at 100 MS/s with a 1.1 V supply voltage. The measured differential non-linearity (DNL) and integral non-linearity (INL) are within 0.38 LSB and 1.21 LSB, respectively, as shown in Fig. 10. Signal spectrums at 100 MS/s with an input sine wave of 4 MHz and 47.5 MHz, respectively, are plotted in Fig. 11. Digital outputs are down-sampled by a factor of 5 with the on-chip decimator to reduce the influence of noise from the measurement board during high-speed operation. The signal-to-noise-and-distortion ratio (SNDR) and the spurious-free dynamic range (SFDR) in Fig. 12(a) are

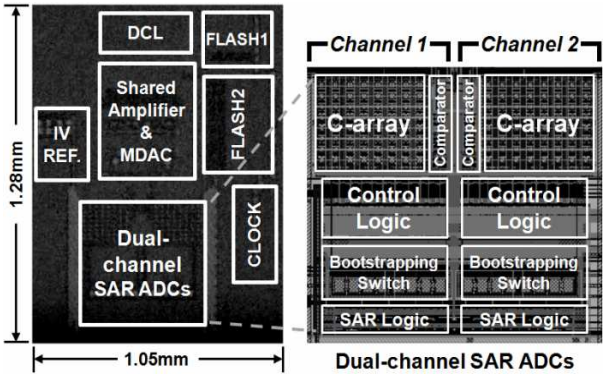


Fig. 8. Die photo of the prototype ADC and layout of the dual-channel SAR ADCs.

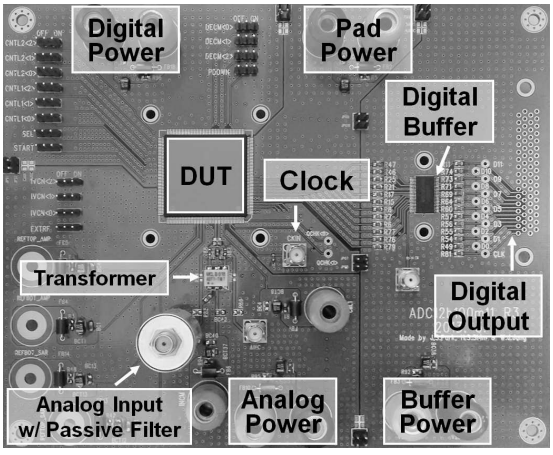


Fig. 9. Evaluation board for the prototype ADC.

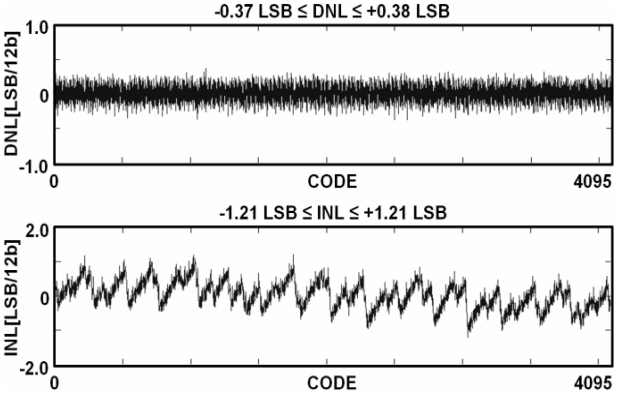
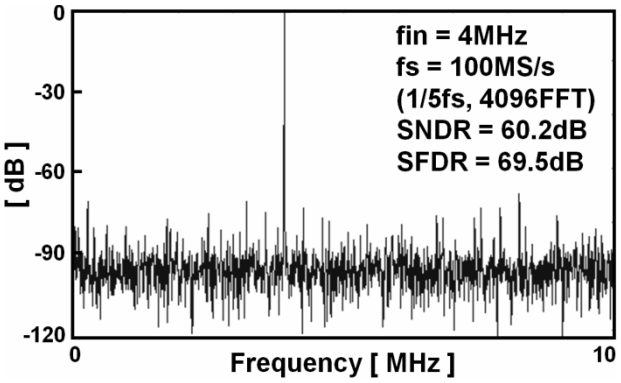
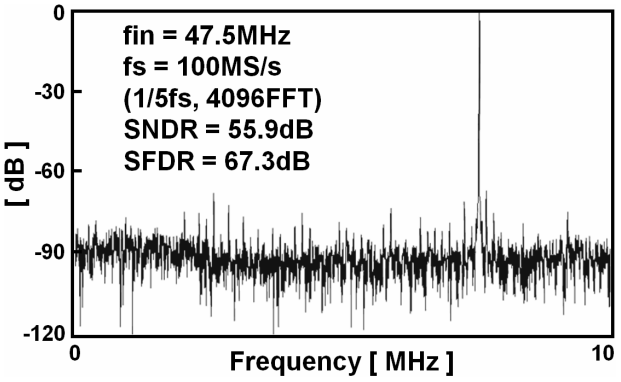


Fig. 10. Measured DNL and INL of the prototype ADC.

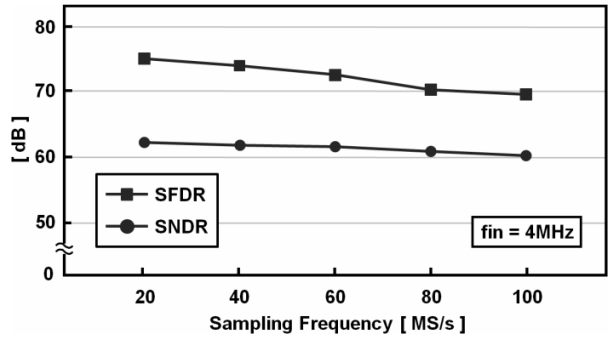


(a)

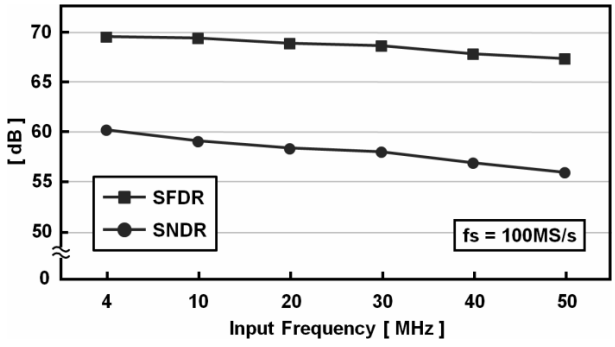


(b)

Fig. 11. Measured FFT spectrums of the ADC at 100 MS/s with (a) fin of 4 MHz, (b) fin of 47.5 MHz (1/5 fs down sampled).



(a)



(b)

Fig. 12. Measured SFDR and SNDR of the ADC versus (a) fs, (b) fin.

Table 1. Performance summary of the prototype ADC

Resolution	12b	
Conversion Rate	100 MS/s	
Process	Dongbu HiTek 0.11 μm CMOS	
Supply	1.1 V	
Input Range	1.0 Vp-p	
DNL	-0.37 LSB / +0.38 LSB	
INL	-1.21 LSB / +1.21 LSB	
SNDR / SFDR	60.2 dB / 69.5 dB (@ fin=4 MHz)	
	55.9 dB / 67.3 dB (@ fin=50 MHz)	
Power Consumption	with I/V Reference	without I/V Reference
	25.3 mW	21.8 mW
Active Die Area	1.34 mm^2 (= 1.05 mm × 1.28 mm)	

measured with sampling frequencies from 20 MS/s to 100 MS/s for a differential sinusoidal input frequency of 4 MHz. While a sampling frequency increases to 100 MHz, the SNDR and SFDR are maintained above 60.2 dB and 69.5 dB, respectively. The SNDR and SFDR variations with increasing input frequencies at a sampling rate of 100 MS/s are illustrated in Fig. 12(b). The SNDR and SFDR are maintained over 55.9 dB and 67.3 dB at the Nyquist input frequency. The SNDR decreases by approximately 4 dB at the Nyquist input frequency compared with the SNDR at the 4 MHz input. The main sources of the SNDR degradation are clock jitter, skew, or distortion caused by signal-dependent delay and finite aperture time [21].

The overall ADC performance is summarized in Table 1, and previously reported 12b SAR ADCs and pipeline ADCs are compared with the proposed hybrid pipeline ADC in Table 2. The figure of merit (FoM), defined as (1), of the prototype ADC is 0.50 pJ/conversion-step, including the power consumption of the on-chip reference generator.

$$FoM = \frac{Power}{2^{ENOB} \times f_S} \tag{1}$$

The sampling rate of the proposed ADC is higher than that of previously reported 12b SAR ADCs. The proposed hybrid pipeline ADC without an input SHA shows similar dynamic performances at the Nyquist input frequency with competitive power consumption compared to previously reported 12b pipeline ADCs. The dynamic performance of the proposed ADC is similar to

Table 2. Comparison of previously reported 12b ADCs

	Speed (MS/s)	Supply (V)	Power (mW)	SNDR @Nyq. (dB)	FoM (pJ/conv.)	Process	Structure
This work	100	1.1	25.3	55.9	0.50	0.11 μm CMOS	Hybrid Pipeline
[13]	45	1.2	3.0	67.1 (w/cal.)	0.04	0.13 μm CMOS	SAR
[17]	50	1.3	3.5 (w/o ref.)	64.4	0.05	65 nm CMOS	SAR-assisted Pipeline
[1]	100	1.0	24.0	56.0	0.47	0.13 μm CMOS	Pipeline w/ SHA (version 1)
			19.0	49.0	0.83		Pipeline w/o SHA (version 2)
[3]	100	1.2	42.0	58.0	0.65	0.13 μm CMOS	Pipeline
[4]	100	1.2	55.0	56.2	1.04	90 nm CMOS	Pipeline

that of the version 1 of [1] despite not employing the SHA. Even though both the proposed ADC and the version 2 of [1] are equally based on the SHA-less topology, the former shows a significant improvement of the dynamic performance compared to the latter. Moreover, the proposed design techniques are expected more effective particularly in nanometer CMOS processes where it is difficult to design a high-gain analog amplifier unlike easily obtainable digital logic.

V. CONCLUSIONS

This work proposes a 12b 100 MS/s hybrid pipeline ADC using SAR and pipeline topologies together. The first stage of the proposed ADC based on dual-channel time-interleaved SAR ADCs for 4 MSBs properly handles the Nyquist-rate input at high speed without a dedicated SHA while the remaining pipeline stages with high-speed flash ADCs decide 8 LSBs. Only one amplifier is employed and shared in the proposed ADC for the first-stage dual-channel residue amplifications and the MDAC of the remaining pipeline stages. The shared residue amplifier for the SAR ADCs prevents performance degradation caused by the amplifier mismatch between channels with low power consumption. A potential reference disturbance occurring from the operating speed difference of two SAR ADCs and one MDAC is much reduced by separating reference voltage drivers. The proposed hybrid pipeline ADC is implemented in a 0.11 μm CMOS and occupies an active die area of 1.34 mm^2. The measured DNL and INL are within 0.38 LSB and 1.21 LSB, respectively. The ADC shows a maximum SNDR of 60.2 dB and a maximum SFDR of 69.5 dB at 100 MS/s with a 4 MHz input. The proposed ADC consumes 25.3 mW at 100 MS/s and a 1.1 V supply voltage.

ACKNOWLEDGMENTS

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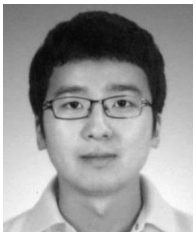

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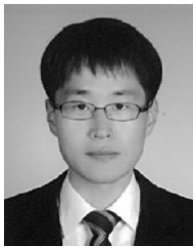

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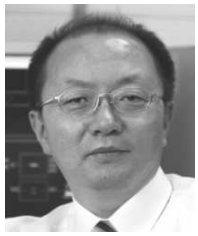

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