Real-time Sound Localization Using Generalized Cross Correlation Based on 0.13 μm CMOS Process

Jungdong Jin[1], Seunghun Jin[1], SangJun Lee[1], Hyung Soon Kim[2], Jong Suk Choi[3], Munsang Kim[3], and Jae Wook Jeon[1]

Abstract—**In this paper, we present the design and implementation of real-time sound localization based on 0.13 μm CMOS process. Time delay of arrival (TDOA) estimation was used to obtain the direction of the sound signal. The sound localization chip consists of four modules: data buffering, short-term energy calculation, cross correlation, and azimuth calculation. Our chip achieved real-time processing speed with full range (360°) using three microphones. Additionally, we developed a dedicated sound localization circuit (DSLC) system for measuring the accuracy of the sound localization chip. The DSLC system revealed that our chip gave reasonably accurate results in an experiment that was carried out in a noisy and reverberant environment. In addition, the performance of our chip was compared with those of other chip designs.**

Index Terms—**Sound signal processing, time delay of arrival, generalized cross correlation, application specific integrated circuit, microphone arrays**

I. INTRODUCTION

Important information for the analysis and recognition of an acquired sound signal can be obtained by detecting the direction of the sound signal. Accordingly, many studies on sound localization have been carried out. To achieve even more accurate and efficient sound localization, many studies have been conducted for a variety of platforms. The results of these studies can be applied as a preprocessing step of several applications such as speech recognition, human machine interaction [1, 2], and security surveillance.

Among the various methods of detecting the direction of a sound signal, TDOA estimation using the time difference between microphones is the most widely used. In TDOA estimation, there are two typical algorithms, generalized cross correlation (GCC) [3] and the average magnitude difference function (AMDF) [4]. GCC uses multiplication, and AMDF uses subtraction [5]. Also, many algorithms have been proposed for implementing TDOA estimation for sound localization [6-10].

Most of the algorithms proposed for improving the performance of sound localization implemented on a multipurpose computer require a high-performance processor for real-time processing. These platforms were large in size and consumed too much power, making them impractical for real applications. In order to overcome these limitations, sound localization implemented on a digital signal processor (DSP) has been proposed [11, 12]. DSP-based sound localization showed near real-time processing and reasonable accuracy in experiments.

Software-based sound localizations are processed with a sequential processing architecture. The problem of this type of processing is that real-time processing cannot be achieved when the complexity of the algorithm increases. To solve this problem, sound localization implemented on a field programmable gate array (FPGA) has been proposed recently [13-15]. This platform can deal with

Manuscript received Feb. 1, 2013; accepted Jan. 16, 2014
[1] Dep. ECE., Sungkyunkwan University, Suwon, Korea
[2] Dep. EE., Pusan University, Pusan, Korea
[3] Adv. Robotics Research Center, KIST, Seoul, Korea
E-mail : jwjeon@yurim.skku.ac.kr

highly complex algorithms by parallel processing through dedicated hardware architecture in real-time. Also, there have been several recent studies on sound localization implemented on the application specific integrated circuit (ASIC) for real-time processing, compact size, optimization, and efficient power consumption. D. Halupka et al. [16] proposed robust sound localization using two microphones based on 0.18 μm CMOS process. They made a circuit which applies the GCC phase transform (PHAT) algorithm, and measured its accuracy within 2.2° at one meter. The silicon area used was 6.25 mm^2, and the power consumption was approximately 30 mW. However, the sound localization range of their chip was only 180°. P. Julian et al. [17] developed a CMOS integrated circuit for calculating the direction of a signal in the low-audio range based on the 0.35 μm process. They applied a correlation derivative algorithm to their circuit, which used four microphones, to localize the sound signal with full range (360°). The silicon area of their chip was 2 mm by 2.4 mm and the power consumption was 600 μW. However, their circuit had a relatively high processing time (1 sec). S.-C. Lee et al. [5] designed an AMDF circuit using two microphones based on the 0.18 μm process. Although they could achieve an accuracy of 90% and average angle error within ±5° at up to five meters in an experiment, their chip only gave localization results of less than half the sound localization range (150°). Their chip occupied a silicon area of 2.86 mm by 3.56 mm and had an average power consumption of 43 mW. A. Gore et al. [18] developed a min-max stochastic optimization method for a regularized cost function circuit using four miniature microphones based on the 0.5 μm CMOS process. The measured resolution was less than 2°, and their chip occupied a smaller silicon area than other chips. In their experiment, they fixed the speaker (the sound source) and measured the direction of the sound source while rotating their sound localization system. Sound localization was carried out every 80 ms using an FPGA. Due to the small chip area, the measured power consumption was also less than 75 μW. J.-F. Wang et al. [19] proposed two novel hardware architectures, the folded architecture and the circular buffer, based on 0.18 μm CMOS process. They designed an AMDF circuit and obtained a localization accuracy rate of 90% with ±3° error on average. Their chip occupied a silicon area of 0.998 mm^2 and had a power consumption of approximately 1.3 mW. Even though they obtained efficient accuracy, the range of the measured sound localization was only 150°.

We propose real-time sound localization based on 0.13 μm CMOS process. We focused on two main factors: the processing speed and the range of sound localization based on ASIC. The sound localization hardware architecture based on FPGA of S. Jin et al. [14] was migrated into our chip, for which we changed all the IP cores of the FPGA to the macro/standard cells of an ASIC, and optimized modules to reduce the die area. We present the hardware architecture and performance of the proposed chip quantitatively.

This paper is organized as follows: Section II outlines the sound localization algorithm. The proposed hardware architecture and its implementation are presented in Section III and Section IV, respectively. Section V describes the experimental results. Finally, conclusions are provided in Section VI, together with a summary.

II. SOUND LOCALIZATION ALGORITHM

This section briefly introduces the proposed sound localization algorithm implemented on our chip. We applied the TDOA estimation of H.-D. Kim et al. [20], which fundamentally used the GCC algorithm. The algorithm consists of four steps: short-term energy calculation, delayed sample storage, cross correlation calculation, and azimuth calculation. Sound signals are obtained from microphones placed at different positions, and the sound signals are stored in corresponding buffers. Then, the short-term energy calculation is executed using the sound signal stored in each buffer. After that, cross correlation calculation is carried out for each pair of sound signals obtained from each microphone. Using the cross correlation results and the relational information between microphones, the azimuth of the sound signal is estimated. Fig. 1 shows a flow chart of the sound localization algorithm.

The cross correlation calculation is the most important step in the sound localization algorithm. Cross correlation is calculated to obtain the arrival delay time difference of the sound signals between each pair of microphones. After this calculation, the relational coefficients between microphones are obtained by the

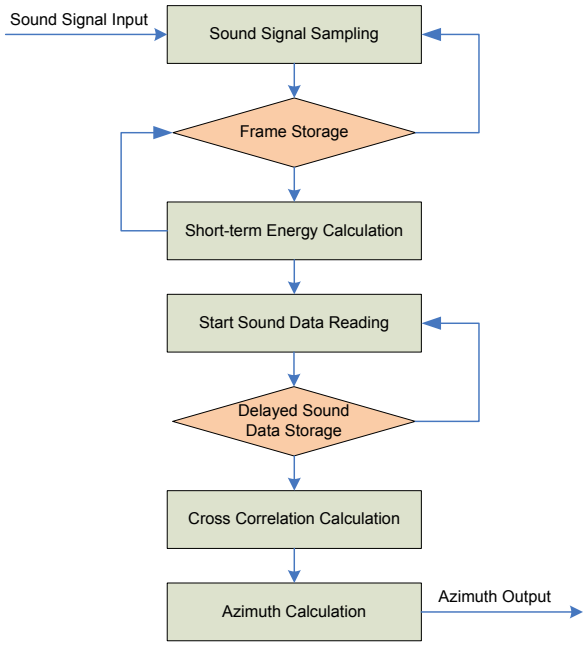


Fig. 1. Flow chart of sound localization algorithm.

following equation:

$$R_{xy}(k)=\frac{\sum_{n=0}^{N-1}x(n)y(n-k)}{\sqrt{\sum_{n=0}^{N-1}x^2(n)}\sqrt{\sum_{n=0}^{N-1}y^2(n-k)}},$$
$$\kappa=0,\pm1,\cdots,\pm ND$$

where $R_{xy}(k)$ is the relational coefficient corresponding to each pair of microphones, $x(n)$, and $y(n)$ are the sample addresses of each pair of sound signals, n is a natural number, k is the delayed sample number, and ND is the delayed maximum sample number.

III. Proposed Hardware Architecture

Our developed DSLC system consists of three separate parts: a sound sampling module, communication controller, and sound localization chip. Once analog sound signals enter the three microphones located uniformly in a triangle shape, these signals are converted to digital sound signals in the sound sampling module. Then, the converted signals are transferred to the communication controller sequentially. In the communication controller, these signals are separated by three channels and are passed to the sound localization chip in parallel. Using the received signals, the chip estimates the azimuth of the sound signal through calculation of the short-term energy, cross correlation and azimuth. Fig. 2 illustrates the overall hardware architecture of the DSLC system.

1. Sound Sampling Module

In the DSLC system, the nonlinear amplified board (NAB) developed by S. S. Yeom et al. [11] is used for sound signal sampling. The AD1836A codec IC of Analog Devices Inc. is used in the NAB. Using the codec IC, analog sound signals are converted to digital sound signals. A serial peripheral interface (SPI) is used for operation setting, and time-division multiplexing (TDM) is used for data transmission. Using this configuration, the digital sound signals converted by the codec IC are transferred to the communication controller through the TDM port at a sampling rate of 48 KHz.

2. Communication Controller

The communication controller acts as a connection channel between the sound sampling module and the sound localization chip. It consists of an SPI, TDM, universal asynchronous receiver/transmitter (UART), and an angle displayer. The SPI used for operating settings is the communication interface between the communication controller and the sound sampling module. The TDM receives the digital sound signals from the sound sampling module. The azimuth received from the sound localization chip is transferred to the computer using the UART. The angle displayer turns on the light emitting diode (LED) according to the azimuth obtained from the sound localization chip.

3. Sound Localization Chip

Our sound localization chip consists of four separate modules for data buffering, short-term energy calculation, cross correlation, and azimuth calculation. Each module performs calculations in real-time using parallel hardware architecture.

The azimuth obtained using this processing architecture is transferred to the communication controller for display. In the data buffering module, each channel's 16-bit sound data are stored in the corresponding memory at a 16-KHz sampling rate. The

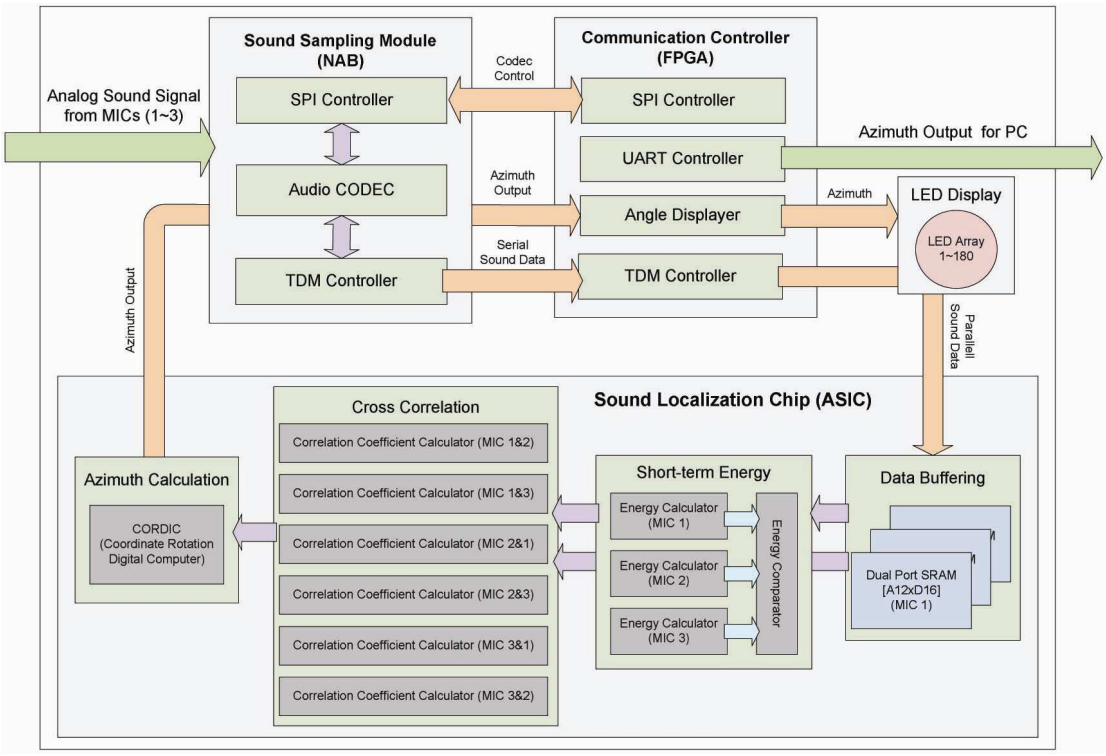


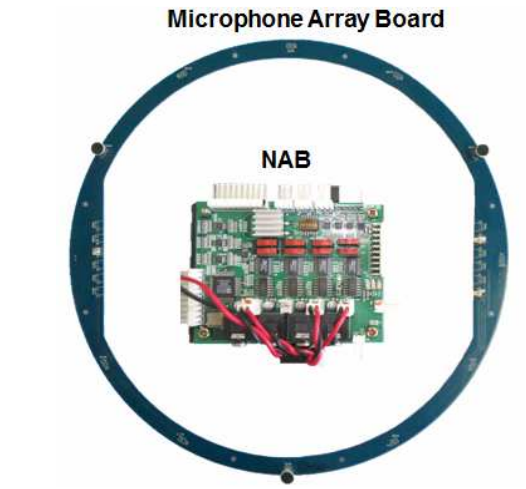
Fig. 2. Overall hardware architecture of the DSLC system.

data stored in each memory are read at a 12.5-MHz processing rate and then passed to the next module. This function is implemented by dual-port static random access memory (SRAM) for each channel. After 3200 sample data are stored in each memory in the first operation, these data are passed to the next module at the processing rate. Applying the sliding window method, data are passed rotationally per 10 ms. Thus, each dual-port SRAM works as a circular queue. In the short-term energy calculation module, the magnitudes of energies are calculated using 3174[3200(sampling data) – 26(*ND*)] for each channel in parallel. After the short-term energy calculation, the energy of the highest magnitude is compared with the threshold. If the energy is greater than the threshold, we move to the next module; otherwise, we wait for the next sound data in this module. In the cross correlation module, each cross correlation is calculated simultaneously using the parallel hardware architecture. Finally, using the correlation coefficients obtained from the previous module, the azimuth calculation module calculates the azimuth using the coordinate rotation digital computer (CORDIC). All computations are completed within 8 ms for 3200 sound data at the processing rate. After an initial latency, the result of sound localization is obtained every 10 ms.

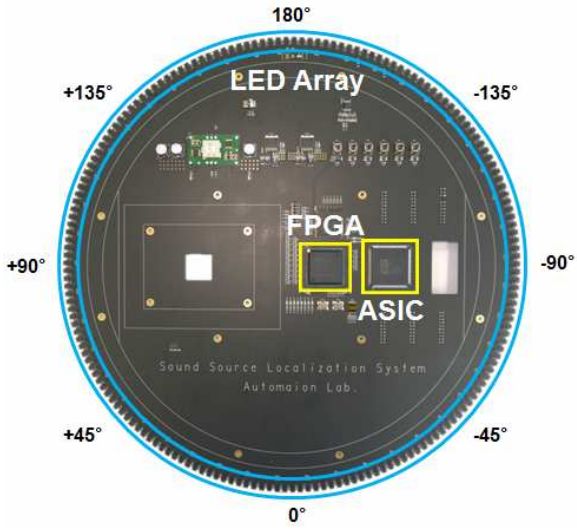
IV. IMPLEMENTATION

We developed a DSLC system to evaluate the sound localization chip. Space for mounting NAB and the microphone array board was prepared in the system. Some connectors for communication with other systems were established. The NAB and the microphone array board were loaded on the DSLC system. Therefore, the DSLC system can interact with the NAB, the microphone array board, and other systems. A Xilinx Spartan-6 XC6SLX75-3FGG676I FPGA with several communication controllers, a chip for implementing sound localization, and an LED array displaying the azimuth were loaded on the DSLC system. The package type of the sound localization chip was a 208-pin low-profile quad flat package (LQFP). Each LED was placed every 2° for a total of 180 LEDs on the DSLC system. Fig. 3 shows the components of the DSLC system, and Fig. 4 shows a photograph of the DSLC system.

Fig. 5 shows the die of the chip used to implement the sound localization algorithm. Our chip was designed based on the 0.13 μm 1-poly 6-metal CMOS process by



(a)



(b)

Fig. 3. Components of DSLC system (a) NAB and microphone array board, (b) main board of DSLC system.

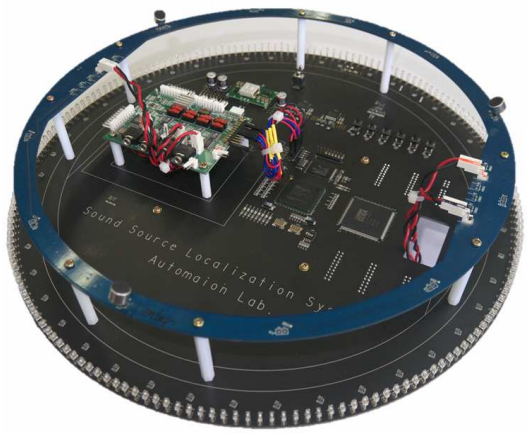


Fig. 4. Photograph of DSLC system.

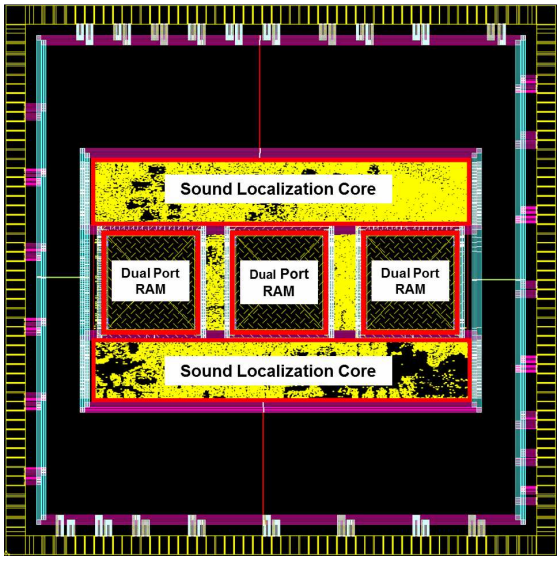


Fig. 5. Micrograph of chip die.

Samsung Electronics. We used the Synopsys Design Compiler, Prime Time, and Astro for synthesis, static timing analysis, and place and route, respectively. Also, we used Mentor Graphics ModelSim for pre-layout and post-layout simulations. Three independent dual-port SRAMs for sound data buffering were loaded on the die. Each dual-port SRAM has an address depth of 12 and data width of 16. We used 1.2 V for internal computation and 3.3 V for external communication. The entire die size was 16 mm^2. The total silicon area of the three dual-port SRAMs was 1.293 mm^2, and the sound localization core area was 2.649 mm^2. Thus, the total area of the sound localization chip was 3.943 mm^2. The power consumption of the chip was 5.628 mW, which was measured directly using a GoldStar DM-241 digital multimeter. The total gate count of the chip was 611240.

V. EXPERIMENTAL RESULTS

1. Experimental Setup

Our experiment was conducted in a seminar room approximately 6.9 m by 6.5 m in area. Several chairs and desks in rows were in the room, and a working computer was located in the upper right corner of the room. All windows and doors were closed. We installed the DSLC system on the desk located in the center of the room, and a speaker was installed one meter from the center of the DSLC system. A pre-recorded test speech signal was

Table 1. Experimental result of proposed sound localization chip

Speech Signal Position	Measured Position (deg.)										Success Accuracy	Standard Deviation	Total Success Accuracy
	1	2	3	4	5	6	7	8	9	10			
0°	-2	1	-1	0	0	3	1	1	1	-1	100%	1.45°	**92.5%**
+45°	43	47	44	44	**55**	44	42	45	45	48	90%	3.79°	
+90°	86	90	90	92	95	95	90	**102**	**82**	86	80%	5.72°	
+135°	136	137	136	137	131	136	133	133	137	138	100%	2.31°	
+180°	177	184	181	181	**171**	175	182	180	176	184	90%	4.58°	
-45°	-45	-41	**-23**	-50	-48	-48	-44	-40	-41	-44	90%	8.07°	
-90°	**-99**	-90	-91	-89	-89	-87	-87	-90	-89	-90	90%	3.38°	
-135°	-135	-134	-136	-130	-134	-139	-136	-137	-135	-134	100%	2.36°	

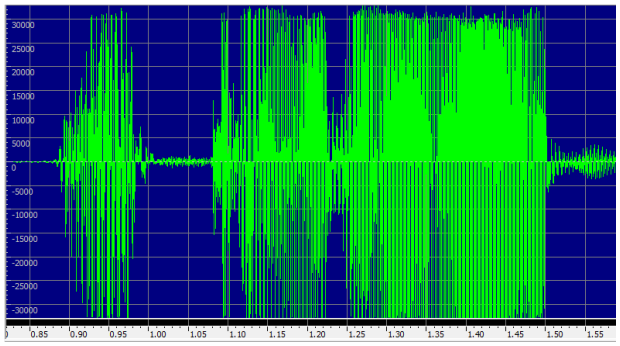


Fig. 6. The waveform of test speech signal "Autorot".

output from the speaker configuration. The azimuth was measured at each position and checked with a laptop through an RS-232C port.

2. Experimental Result

Table 1 shows the experiment results of the proposed sound localization chip. The experiment was conducted omnidirectionally at intervals of 45°. We measured the azimuth using a pre-recorded speech signal through a speaker, and the speaker was moved to each position. We repeated this measurement ten times per position. The waveform of the test speech signal, "autorot", is shown in Fig. 6. The X axis represents the time (sec), and the Y axis represents the amplitude (signed 16 bit) of the signal. This test speech signal was captured using GoldWave GoldWave v5.17, and the signal to noise ratio (SNR) ranged from 26 to 29. The average noise measured in the seminar room ranged from 34 to 37 db, and the average magnitude measured ranged from 78 to 83 db when the test speech signal was output. If the measured azimuth was less than ±5° compared to the original position, we considered the measurement a success. The measurement was considered to fail otherwise. The azimuth values in bold in Table 1 mean failures. In this experiment, we also calculated the accuracy and standard deviation of the azimuth at each position. We obtained a total accuracy of 92.5% within ±5° average error at one meter in the experiments of noise and reverberation in the indoor environment.

3. Chip Performance Comparison

Table 2 shows the performance of our chip compared to those of other chip designs. Some chips used four microphones to localize the sound signal with full range (360°) [17, 18]. However, our chip used only three microphones to localize with full range. The measurement ranges of the other chips in the experiment were smaller than those of our chip. Also, the localization output interval corresponding to the processing speed was much faster than those of the other chips.

VI. CONCLUSION

We have proposed a real-time sound localization based on the 0.13 μm CMOS process. All modules of sound localization were integrated in a single chip, which included data buffering, short-term energy calculation, cross correlation, and azimuth calculation modules. The results showed that our chip could finish all processing in real-time with full range using three microphones, making it suitable for real applications. Also, the accuracy of the proposed chip was evaluated in a noisy and reverberant experiment on a DSLC system. Although our experimental environment was quite challenging, our

Table 2. Performance comparison with other chip designs

Author	The number of microphone	Measured localization range in experiment	Localization range	Localization output interval
Proposed chip	3	360° (-180° - +180°)	360°	10 ms
Wang et al.[19] 2011	2	150° (-75° - +75°)	180° (Expectation)	-
Gore et al.[18] 2010	4	90° (0° - +90°)	360° (Expectation)	80 ms
Lee et al.[5] 2010	2	150° (-75° - +75°)	180° (Expectation)	-
Julian et al.[17] 2006	4	200° (-100° - +100°)	360°	1000 ms
Halupka et al.[16] 2005	2	180° (-90° - +90°)	180°	-

chip gave reasonably accurate results. In addition, we showed the advantages of our chip by comparison with other chip designs. In the future, we will improve the accuracy of our sound localization chip.

ACKNOWLEDGMENTS

This research was supported by PRCP through NRF of Korea, funded by MEST(2012-0005861), and in part by IDEC.

REFERENCES

[1] J.-M. Valin, F. Michaud, J. Rouat, D. Letourneau, "Robust Sound Source Localization Using a Microphone Array on a Mobile Robot," *IEEE/RSJ International Conference on Intelligent Robots and Systems*, vol. 2, pp. 1228-1233, October 2003.

[2] K.-C. Kwak, S.-S. Kim, "Sound source localization with the aid of excitation source information in home robot environments," *IEEE Transactions on Consumer Electronics*, vol. 54, No. 2, pp. 852-856, May 2008.

[3] C. H. Knapp, G. C. Carter, "The generalized correlation method for estimation of time delay," *IEEE Transactions on Sounds, Speech and Signal Processing*, vol. 24, No. 4, pp. 320-327, August 1976.

[4] M. J. Ross, H. L. Shaffer, A. Cohen, R. Freudberg, H. J. Manley, "Average magnitude difference function pitch extractor," *IEEE Transactions on Sounds, Speech and Signal Processing*, vol. 22, No. 5, pp. 353-362, October 1974.

[5] S.-C. Lee, B.-W. Chen, J.-F. Wang, K. Bharanitharan, C.-Y. Chen, "Far field-aware SOC design for sound source location based on 0.18-μm CMOS process," *International Symposium on Aware Computing*, pp. 111-115, November 2010.

[6] J. Huang, N. Ohnishi, N. Sugie, "Sound localization in reverberant environment based on the model of the precedence effect," *IEEE Transactions on Instrumentation and Measurement*, vol. 46, No. 4, pp. 842-846, August 1997.

[7] P. Julian, A. G. Andreou, L. Riddle, S. Shamma, D. H. Goldberg, G. Cauwenberghs, "A comparative study of sound localization algorithms for energy aware sensor network nodes," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, No. 4, pp. 640-648, April 2004.

[8] B. Mungamuru, P. Aarabi, "Enhanced sound localization," *IEEE Transactions on Systems, Man, and Cybernetics, Part B: Cybernetics*, vol. 34, No. 3, pp. 1526-1540, June 2004.

[9] C. Zhang, D. Florencio, D. E. Ba, Z. Zhang, "Maximum Likelihood Sound Source Localization and Beamforming for Directional Microphone Arrays in Distributed Meetings," *IEEE Transactions on Multimedia*, vol. 10, No. 3, pp. 538-548, April 2008.

[10] M. Raspaud, H. Viste, G. Evangelista, "Binaural Source Localization by Joint Estimation of ILD and ITD," *IEEE Transactions on Audio, Speech, and Language Processing*, vol. 18, No. 1, pp. 68-77, January 2010.

[11] S. S. Yeom, J. S. Choi, Y. S. Lim, M.-Y. Park, M.

Kim, "DSP implementation of sound source localization with gain control," *International Conference on Control, Automation and Systems*, pp. 224-229, October 2007.

[12] S. S. Yeom, J. S. Choi, Y. S. Lim, M. Park, "DSP implementation of probabilistic sound source localization," *IEEE Workshop on Signal Processing Systems*, pp. 204-209, October 2008.

[13] D. Nguyen, P. Aarabi, A. Sheikholeslami, "Real-time sound localization using field-programmable gate arrays," *International Conference on Multimedia and Expo*, vol. 2, pp. 829-832, July 2003.

[14] S. Jin, D. Kim, H. S. Kim, C. H. Lee, J. S. Choi, J. W. Jeon, "Real-time sound source localization system based on FPGA," *IEEE International Conference on Industrial Informatics*, pp. 673-677, July 2008.

[15] J.-F. Wang, Y.-C. Jiang, Z.-W. Sun, "FPGA implementation of a novel far-field sound localization system," *IEEE Region 10 Conference TENCON*, pp. 1-4, January 2009.

[16] D. Halupka, N. J. Mathai, P. Aarabi, A. Sheikholeslami, "Robust sound localization in 0.18 μm CMOS," *IEEE Transactions on Signal Processing*, vol. 53, No. 6, pp. 2243-2250, June 2005.

[17] P. Julian, A. G. Andreou, D. H. Goldberg, "A low-power correlation-derivative CMOS VLSI circuit for bearing estimation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 14, No. 2, pp. 207-212, February 2006.

[18] A. Gore, A. Fazel, S. Chakrabartty, "Far-Field Sound Source Localization and Bearing Estimation Using ΣΔ Learners," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, No. 4, pp. 783-792, April 2010.

[19] J.-F. Wang, C.-H. Chou, Y.-J. Huang, P.-C. Lin, B.-W. Chen, "An improvement of chip design for auditory source localization awareness," *International Conference on Awareness Science and Technology*, pp. 366-369, September 2011.

[20] H.-D. Kim, J.-S. Choi, C.-H. Lee, G.-T. Park, M.-S. Kim, "Sound's Direction Detection and Speech Recognition System for Humanoid Active Audition," *International Conference on Control, Automation and Systems*, pp. 633-638, October 2003.

Jungdong Jin was born in Hwa-Seong, Korea, in 1984. He received a B.S. degree in the Department of Control and Instrumentation Engineering from Seoul National University of Science & Technology, Seoul, Korea, in 2011 and the M.S. degree in the Department of Electrical and Computer Engineering from Sungkyunkwan University, Suwon, Korea, in 2013. In 2013, he joined LG Electronics, Seoul, Korea, as an R&D Staff Member. His research interests include image and speech signal processing, embedded systems, and real-time applications.

Seunghun Jin received the B.S., M.S., and Ph.D. degrees in the Department of Electrical and Computer Engineering from Sungkyunkwan University, Suwon, Korea, in 2005, 2006, and 2009, respectively. In 2010, he joined the Samsung Advanced Institute of Technology, Yongin, Korea, as a R&D Staff Member. His research interests include reconfigurable architecture, image and speech signal processing, embedded systems, and real-time applications.

SangJun Lee received the B.S. degree in Electronics Engineering from Korea Polytechmic University, Siheung, Korea, in 2006, and the M.S. degree in the Department of Electrical and Computer Engineering from Sungkyunkwan University, Suwon, Korea, in 2010. He is currently pursuing the Ph.D. degree in the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, Korea. His research interests include image and speech signal processing, embedded systems, and real-time applications.

Hyung Soon Kim received B.S. degree in Electronics Engineering from Seoul National University, Seoul, Korea, in 1983, and M.S. and Ph.D. degrees in Electrical Engineering from the Korea Advanced Institute of Science and Technology, Taejon, Korea, in 1984 and 1989, respectively. In 1992, he joined the Electrical Engineering, Pusan National University, Pusan, Korea, where he is currently Professor. His research interests include communication system and speech signal processing.

Jong Suk Choi received a B.S., M.S., and Ph.D. degree in Electrical Engineering from the Korea Advanced Institute of Science and Technology Taejon, Korea, in 1994, 1996, and 2001, respectively. In 2001, he joined the Intelligent Robotics Research Center, Korea Institute of Science and Technology (KIST), Seoul, Korea, as a Research Scientist and now is a Senior Research Scientist at Korea Institute of Science and Technology (KIST). His research interests include signal processing, human-robot interaction, mobile robot navigation and localization.

Munsang Kim received his B.S. and M.S. degrees in Mechanical Engineering from the Seoul National University in 1980 and 1982, respectively, and the Dr.-Ing. degree in Robotics from the Technical University of Berlin, Germany, in 1987. Since 1987, he has been working as a research scientist at the Korea Institute of Science in Korea. He leads the Advanced Robotics Research Center since 2000 and became the director of the Intelligent Robot-The Frontier 21 Program since 2003. His current research interests are the design and control of novel mobile manipulation systems, haptic device design and control, and sensor application in intelligent robots.

Jae Wook Jeon received B.S. and M.S. degrees in Electronics Engineering from Seoul National University, Seoul, Korea, in 1984 and 1986, respectively, and a Ph.D. degree in Electrical Engineering from Purdue University, West Lafayette, IN, in 1990. From 1990 to 1994, he was a Senior Researcher with Samsung Electronics, Suwon, Korea. Since 1994, he has been with the School of Electrical and Computer Engineering, Sungkyunkwan University, Suwon, first as an Assistant Professor, and currently as a Professor. His research interests include robotics, embedded systems, and factory automation.