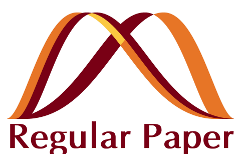
TRANSACTIONS ON ELECTRICAL AND ELECTRONIC MATERIALS
Vol. 15, No. 2, pp. 73-76, April 25, 2014



pISSN: 1229-7607 eISSN: 2092-7592
DOI: http://dx.doi.org/10.4313/TEEM.2014.15.2.73

Effect of Annealing Atmosphere on the La_2O_3 Nanocrystallite Based Charge Trap Memory

Zhenjie Tang[†], Dongqiu Zhao, and Huiping Hu
College of Physics and Electronic Engineering, Anyang Normal University, Anyang 455000, China

Rong Li
School of Mathematics and Statistics, Anyang Normal University, Anyang 455000, China

Jiang Yin
Department of Materials Science and Engineering, National Laboratory of Solid State Microstructures, Nanjing University, Nanjing 210093, China

Received February 7, 2014; Revised February 27, 2014Accepted March 4, 2014

$Pt/Al_2O_3/La_2Si_5O_x/SiO_2/Si$ charge trap memory capacitors were prepared, in which the $La_2Si_5O_x$ film was used as the charge trapping layer, and the effects of post annealing atmospheres (NH_3 and N_2) on their memory characteristics were investigated. La_2O_3 nanocrystallites, as the storage nodes, precipitated from the amorphous $La_2Si_5O_x$ film during rapid thermal annealing. The NH_3 annealed memory capacitor showed higher charge storage performances than either the capacitor without annealing or the capacitor annealed in N_2. The memory characteristics were enhanced because more nitrogen was incorporated at the $La_2Si_5O_x/SiO_2$ interface and interfacial reaction was suppressed after the NH_3 annealing treatment.

Keywords: Annealing atmosphere, La_2O_3 nanocrystallite, Memory

1. INTRODUCTION

With conventional floating gate type memories approaching their scaling limit, tremendous effort has been made to explore next generation nonvolatile memory devices [1-5]. Of the alternatives, nanocrystallite (NC)-based charge trap memory (CTM) devices have received much attention in the electronics industry because of their advantages such as lower operation voltage, higher endurance, and simple fabrication process compatible with standard complementary metal oxide semiconductor (CMOS) technology [6-9]. Numerous works have focused on developing charge trapping layers containing metallic or semiconducting NCs for use in nonvolatile memory devices [10-17]. However, researchers have been challenged by the poor thermal stability as well as the incompatibility with the metal oxide semiconductor (MOS) process of metallic or semiconducting NC memory devices [18,19].

In this work, we report enhanced charge trap memory characteristics by precipitation of NCs from the amorphous $La_2Si_5O_x$ (noted as LSO) charge trapping layer through rapid thermal annealing (RTA). In addition, the effects of post annealing in different atmospheres (NH_3 and N_2) on the memory characteristics of memory window and data retention are reported in this paper.

[†] Author to whom all correspondence should be addressed:
E-mail: zjtang@hotmail.com

Copyright ©2014 KIEEME. All rights reserved.
This is an open-access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (http://creativecommons.org/licenses/by-nc/3.0) which permits unrestricted noncommercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

2. EXPERIMENTS

La_2O_3 NC-based CTM capacitors with a $Pt/Al_2O_3/LSO/SiO_2/$ p-Si stack structure were fabricated. Prior to film deposition, p-type Si (100) substrates with a resistivity of 3~20 Ω·cm were

cleaned by the standard Radio Corporation of America (RCA) process to remove native oxide. Then, 3 nm SiO_2 was thermally grown in dry O_2 at 900℃ as the tunneling layer. An LSO charge trapping layer of ~6 nm thickness was deposited by pulsed laser deposition (PLD) at a substrate temperature of 350℃. Subsequently, 8 nm Al_2O_3 was deposited as the blocking layer by atomic layer deposition (ALD) using tri-methylaluminium ($Al(CH_3)_3$) precursors at a substrate temperature of 300℃. The fabricated memory device without post annealing was denoted as S1. After the above processes, the memory capacitors were rapid - thermal - annealed at 900℃ for 30 s in N_2 and NH_3 atmospheres, and were denoted as S2 and S3, respectively. Finally, platinum (Pt) gate electrodes (7.85×10^5 cm^2) with a patterned mask were deposited on the blocking layer by the magnetron sputtering technique at room temperature. The thermal stability of the LSO films was examined by X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS), and the cross sections and interface quality of the memory capacitors were revealed in high-resolution transmission electron microscope (HRTEM) images. The electrical characteristics of the memory capacitors were measured using a Keithley 4200 semiconductor characterization system (4200 SCS).

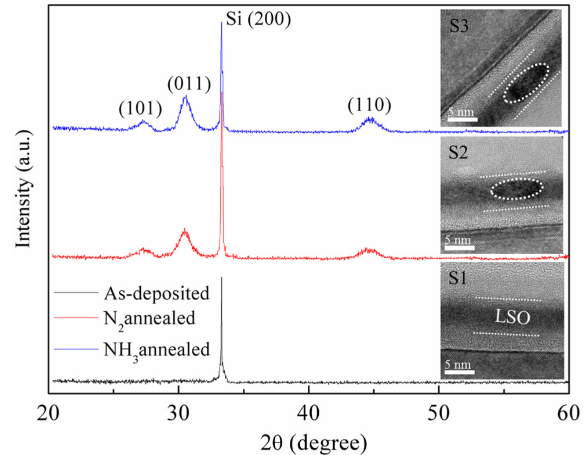


Fig. 1. XRD patterns of as-deposited and RTA treated LSO films. The insets show the cross sectional HRTEM images of the S1, S2, and S3 samples, respectively.

3. RESULTS AND DISCUSSION

The XRD patterns of as-deposited and RTA - treated LSO films are presented in Fig. 1. The as-deposited LSO films remain amorphous, but some crystalline peaks appear after RTA at 900℃ in N_2 and NH_3 atmospheres. These diffraction peaks correspond to the (101), (011) and (110) planes of cubic La_2O_3 [20], respectively. The results show that the crystalline La_2O_3 phase precipitated from the amorphous LSO matrix after RTA treatment. The inset of Fig. 1 shows the cross sectional HRTEM images of the S1, S2 and S3 samples, respectively. The La_2O_3 NCs, as indicated by the dotted circles, precipitated and became embedded in the LSO film matrix after the N_2 and NH_3 annealing treatments.

Figure 2(a) illustrates the high frequency (1 MHz) capacitance-voltage (C-V) hysteresis memory windows of the memory capacitors, measured under the same gate sweeping voltage. Memory window is defined as the difference in the flat band voltages between the program and erase states. The hysteresis memory windows of the S1, S2 and S3 samples were measured to be 1.5 V, 3.8 V, and 5.6 V, respectively. We programmed the above three memory capacitors to have the same initial flat band voltage (5.4 V) to compare their data retention characteristics at room temperature, as shown in Fig. 2(b). The charge losses of the S1, S2 and S3 samples were 15%, 10% and 2% after 1.2×10^4 s, respectively. In order to predict the long-term charge retention characteristics of the samples, the experimental results were extrapolated; the charge losses of the S1, S2 and S3 samples after 10 years would be 70%, 44% and 22%, respectively, which suggested that the N_2 and NH_3 annealing treatments could reduce the charge loss. The S3 has the optimum retention performance, which may be due to the nitrogen incorporation at the $La_2Si_5O_x/SiO_2$ interface and the effective suppression of interfacial reaction after the NH_3 annealing treatment, as discussed below.

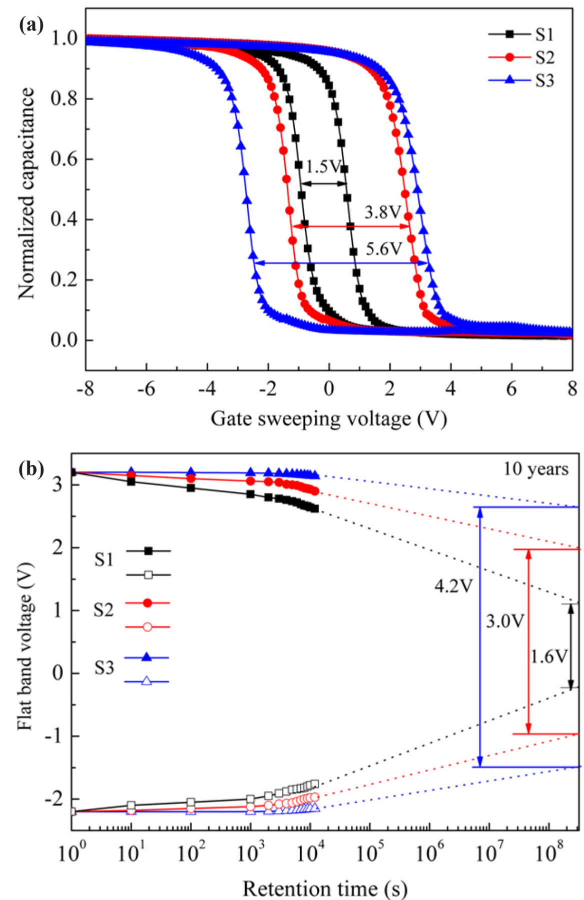


Fig. 2. (a) High frequency (1 MHz) capacitance versus gate voltage (C-V) curves, and (b) data retention characteristics of the S1, S2 and S3 samples.

To determine the effect of annealing atmosphere on memory characteristics, the LSO/SiO_2 interface before and after annealing treatment was evaluated by XPS analysis. Figure 3(a) shows the XPS spectra of the Si 2s for the S1, S2 and S3 samples, respectively. For the S1 sample, the peak located at 150.9 eV corresponds to the Si substrate, while the peaks located at 152.3 and 154.6 eV correspond to La-silicate and SiO_2, respectively. The weak La-silicate peak intensity means that there is no obvious interfacial layer at the LSO/SiO_2 interface before annealing. For the S2 and S3 samples, however, the intensity of the La-silicate peak increases, suggesting interfacial reaction at the LSO/SiO_2 interface during the post annealing process [21]. Moreover, the La-silicate peak position shifts to the high binding energy position, indicating that the Si content increases at the LSO/SiO_2 interface to form Si rich La-silicate. For the S3 sample, the relatively weaker La-

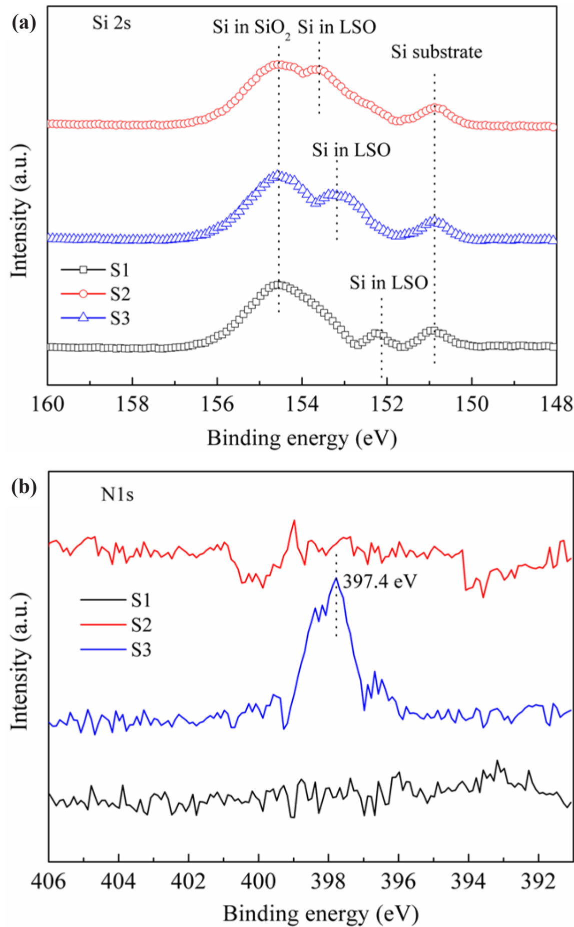


Fig. 3. XPS spectra of Si 2s (a) and N 1s (b) of the S1, S2 and S3 samples.

silicate peak intensity indicates that NH_3 annealing can suppress interfacial reaction, unlike N_2 annealing. In addition, the binding energies of the La-silicate peaks of the S2 and S3 samples are 153.7 and 153.3 eV, respectively. The lower binding energy of the S3 sample may be due to the presence of nitrogen in the film [22-25]. Figure 3(b) shows the N 1s XPS spectra of the S1, S2 and S3 samples, respectively: the N 1s peak of the S3 sample is at 397.4 eV, but those of the S1 and S2 samples cannot be observed. The results indicate that NH_3 annealing can effectively incorporate nitrogen at the LSO/SiO_2 interface, suppress interfacial reaction, and decrease charge loss to enhance memory performance. Therefore, a La_2O_3 NC - based CTM device after NH_3 annealing is a promising candidate for future nonvolatile memory applications.

4. CONCLUSIONS

We fabricated charge trap memory capacitors with a Pt/Al_2O_3/$La_2Si_5O_x$/SiO_2/Si stack structure, in which the $La_2Si_5O_x$ film was used for charge trapping. The effects of post annealing atmospheres (NH_3 and N_2) on their charge memory characteristics were investigated. The La_2O_3 nanocrystallites, as the storage nodes, precipitated from the amorphous $La_2Si_5O_x$ film during rapid thermal annealing. The NH_3 atmosphere annealed memory capacitor showed higher charge storage performance (i.e., larger memory window and optimal data retention) than either the capacitor without annealing or the capacitor annealed in N_2, This result could be due to the more nitrogen incorporation at the $La_2Si_5O_x$/SiO_2 interface and the effective suppression of interfacial reaction after the NH_3 annealing treatment.

ACKNOWLEDGMENTS

This work was financially supported by the Science Foundation of Educational Department of Henan Province of China (Grant No. 13A140021 and 14A140008), National Natural Science Foundation of China (Grant Nos. 11247318 and 11347186), the National Natural Science Foundation of China (Grant nos. 61176124, and 11174122), the State Key Program for Basic Research of China (Grant no. 2010CB934201).

REFERENCES

[1] X. D. Huang, Johnny K. O. Sin, and P. T. Lai, IEEE Electron Device Lett. 34, 499 (2013) [DOI: http://dx.doi.org/10.1109/LED.2013.2244557].

[2] C. H. Zhu, Z. L. Huo, Z. G. Xu, M. H. Zhang, Q. Wang, J. Liu, S. B. Long, and M. Liu, Appl. Phys. Lett. 97, 253503 (2010) [DOI: http://dx.doi.org/10.1063/1.3531559].

[3] M. Burkhardt, A. Jedaa, M. Novak, A. Ebel, K. Voitchovsky, F. Stellacci, A. Hirsch, and M. Halik, Adv. Mater. 22, 2525 (2010) [DOI: http://dx.doi.org/10.1002/adma.201000030].

[4] R. J. Tseng, J. X. Huang, J. Ouyang, R. B. Kaner, and Y. Yang, Nano Lett. 5, 1077 (2005)[DOI: http://dx.doi.org/10.1021/nl050587l].

[5] S. H. Lee, Y. Jung, and R. Agarwal, Nat. Nanotechnol. 2, 626 (2007) [DOI: http://dx.doi.org/10.1038/nnano.2007.291].

[6] H. I. Hanafi, S. T. Tiwari, and I. Khan, IEEE Trans. Electron Devices., 43,1553 (1996) [DOI: http://dx.doi.org/10.1109/16.535349].

[7] Y. L. Han, Z. L. Huo, X. K. Li , G. X. Chen, X. N. Yang , D. Zhang, Y. Wang, T. H. Ye, M. Liu, Electron Device Letters, 34, 870 (2013) [DOI: http://dx.doi.org/10.1109/LED.2013.2260853].

[8] C. C. Lin, Y. H. Wu, Y. S. Lin, M. L. Wu and L. L. Chen, Nanotechnology, 12,436 (2013) [DOI: http://dx.doi.org/10.1109/TNANO.2013.2253796].

[9] K. H. Lee, H. C. Lin and T. Y. Huang, Electron Device Letters, 34, 393 (2013) [DOI: http://dx.doi.org/10.1109/LED.2013.2237748].

[10] J. De Blauwe, IEEE Trans. Nanotechnol. 1, 72 (2002) [DOI: http://dx.doi.org/10.1109/TNANO.2002.1005428].

[11] Z. T. Liu, C. Lee, V. Narayanan, G. Pei, E. C. Kan, IEEE Trans. Electron Devices, 49, 1606 (2002) [DOI: http://dx.doi.org/10.1109/TED.2002.802618].

[12] E. Kapetanakis, P. Normand, D. Tsoukalas, K. Beltsios, J. Stoemenos, S. Zhang, and J. van den Berg, Appl. Phys. Lett. 77, 3450 (2000) [DOI: http://dx.doi.org/10.1063/1.1328101].

[13] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, Appl. Phys.Lett. 68, 1377 (1996) [DOI: http://dx.doi.org/10.1063/1.116085].

[14] J. Sarkar, S. Dey, D. Shahrjerdi, S. K. Banerjee, IEEE Electron Device Lett. 28, 449 (2007) [DOI: http://dx.doi.org/10.1109/LED.2007.895445].

[15] C. Lee, J. H. Kwon, J. S. Lee, Y. M. Kim, Y. Choi, H. Shin, J. Lee, and B. H. Sohn, Appl. Phys. Lett., 91, 153506 (2007) [DOI: http://dx.doi.org/10.1063/1.2798502].

[16] J. Mooney, M. M. Krause, J. I. Saari and P. Kambhampati, J. Chem. Phys. 138 , 204705 (2013) [DOI: http://dx.doi.org/10.1063/1.4807054].

[17] P. Dimitrakis, P. Normand, C. Bonafos, E. Papadomanolaki, and E. Iliopoulos, Appl. Phys. Lett. 102, 053117 (2013) [DOI: http://dx.doi.org/10.1063/1.4790439].

[18] X. D. Huang, P. T. Lai, and Johnny K. O. Sin, ECS Solid State Letters, 1,Q45 (2012) [DOI: http://dx.doi.org/10.1149/2.005206ss].

[19] S. K. Sahoo and D. Misra, Appl. Phys. Lett. 100, 232903 (2012) [DOI: http://dx.doi.org/10.1063/1.4726186].

[20] L. Shi, Y. Yuan, X. F. Liang, Y. D. Xia, J. Yin, Z. G. Liu, Applied Surface Science., 253,3731 (2007) [DOI: http://dx.doi.org/10.1016/j.apsusc.2006.08.006].

[21] S. Y. No, D. Eom, C. S. Hwang, and H. J. Kim, J. Appl. Phys., 100, 024111 (2006) [DOI: http://dx.doi.org/10.1063/1.2218465].

[22] M. R. Visokay, J. J. Chambers, A. L. P. Rotondaro, A. Shanware, and L. Colombo, Appl. Phys. Lett. 80, 3183 (2002) [DOI: http://dx.doi.org/10.1063/1.1476397].

[23] L. Wang, K. Xue, J. B. Xu, A. P. Huang, and P. K. Chu, Appl. Phys. Lett., 90, 122901 (2007) [DOI: http://dx.doi.org/10.1063/1.2715044].

[24] Z. J. Tang, R. Li, F. J. Yu, Vacuum. 99, 17 (2014) [DOI: http://dx.doi.org/10.1016/j.vacuum.2013.05.010].

[25] Z. J. Tang, D. Q. Zhao, R. Li, X. H. Zhu, Trans. Electr. Electron. Mater. 15,16 (2014) [DOI: http://dx.doi.org/10.4313/TEEM.2014.15.1.16].