JPE 14-2-12

http://dx.doi.org/10.6113/JPE.2014.14.2.315
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

# An Optimized Control Method Based on Dual Three-Level Inverters for Open-end Winding Induction Motor Drives

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**Abstract**

An optimized space vector pulse width modulation (SVPWM) method with common mode voltage elimination and neutral point potential balancing is proposed for an open-end winding induction motor. The motor is fed from both of the ends with two neutral point clamped (NPC) three-level inverters. In order to eliminate the common mode voltage of the motor ends and balance the neutral point potential of the DC link, only zero common mode voltage vectors are used and a balancing control factor is gained from calculation in the strategy. In order to improve the harmonic characteristics of the output voltages and currents, the balancing control factor is regulated properly and the theoretical analysis is provided. Simulation and experimental results show that by adopting the proposed method, the common mode voltage can be completely eliminated, the neutral point potential can be accurately balanced and the harmonic performance for the output voltages and currents can be effectively improved.

**Key words:** Balancing control factor, Common mode voltage elimination, Neutral point potential balancing, Open-end winding induction motor, Quasi circular locus

## I. INTRODUCTION

The multi-level inverters have the advantages of higher output quality, smaller withstand voltage of the switching devices and lower harmonic distortion. Thus, they have been widely used in the fields of large-power static var compensators, large-capacity uninterruptible power supplies, high-voltage speed regulation of motor drives, etc. [1]-[3]. On the basis of the withstand voltage rating of the switching devices, a motor drive system based on the dual three-level inverter topology has been proposed, in order to obtain a higher output voltage [4]. The motor stator windings are opened and two identical inverters which share one DC link supply power for the motor from both the ends of the stator windings, is shown in Fig. 1. This topology can use switching devices with a voltage rating of 4.5kV so that the rated output voltage of the inverters is 6kV, the output level is 5, the voltage harmonics are low and the capacity of the required filter is small. Moreover, there is no problem with the voltage sharing brought by the series connection of the switching devices and the equivalent switching frequency is only one half of the conventional three-level inverter topology. If one inverter fails, when compared to the three-level inverter topology, this topology is more suitable for fault-tolerant control and the system is of higher reliability [3]-[5].

There is a large common-mode voltage in the open-end winding induction motor drives fed with a dual three-level inverter. In order to reduce its damage to the motor and its influence on the quality of the output current waveforms and to ensure that the motor operates reliably, reliability measures should be adopted to suppress or eliminate it [6]-[9]. In conventional dual-inverter drive systems, connecting a zero-sequence reactor in series or adopting isolated DC power sources to supply the two inverters will increase the number of elements and the cost of system manufacturing, lower the utilization of the DC voltage and the rapidness of the current response [4], [10]-[13]. In addition, motor drive systems with isolated DC power sources are not conducive to four-quadrant operation. In three-level inverter controls, it is also necessary to consider the neutral point potential unbalance caused by fluctuations of the neutral point potential to avoid distortion

Manuscript received Sep. 4, 2013; accepted Dec. 12, 2013
Recommended for publication by Associate Editor Trillion Q. Zheng.
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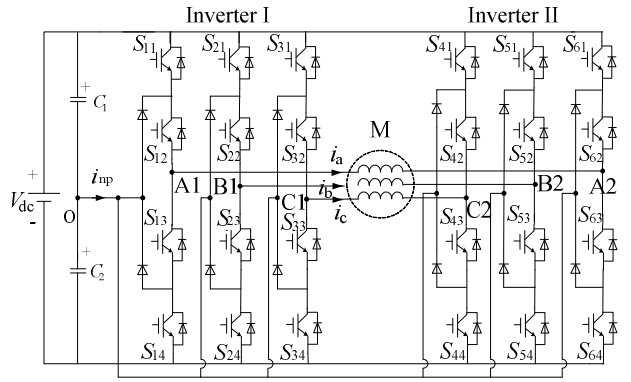


Fig. 1. Schematic of the open-end winding induction motor drive system fed with two NPC three-level inverters.

of the output voltage waveforms and damage to the switching devices along with the DC-link capacitors [14], [15].

For the dual three-level inverter fed with a single DC power source in [4], a direct self-control of the induction machines is adopted and the torque ripple and harmonic content of the stator currents are effectively reduced. However, the common mode voltage in the system is suppressed by the reactors in series. A SVPWM method with common mode voltage elimination and neutral point potential balancing has been proposed in [16], which adopts redundant voltage space vectors with opposite effects on the DC-link capacitor voltage in adjacent switching cycles. This method can, to some extent, implement neutral point potential balancing, and it is only suitable for situations where the motor is in the electric state. In [17], improvements have been made so that another set of SVPWM methods is used when a motor is in the electric state. In addition, real-time detection of the transmission direction of the power is used to determine which set of SVPWM methods should be adopted. However, the amount of program code is increased and the transmission direction of the power is hard to detect accurately. In [10] and [11], a synchronous optimal PWM method is proposed. Under the condition of ensuring the total harmonic distortion of the motor current, this method enables the switching frequency to be very low and reduced to 200Hz, which effectively reduces the switching losses. This method has application prospect in the fields of high-power drive situations. However, the common mode voltage needs to be suppressed through reactors in series.

For the advantages and disadvantages of the above methods, an optimized SVPWM method is proposed in this paper. Firstly, zero common mode voltage space vectors are adopted to eliminate the common mode voltage. The corresponding diagram of the voltage space vectors is provided. Secondly, according to the diagram of the voltage space vectors and the topology of the dual three-level inverter for open-end winding induction motor drives, the influences of different voltage space vectors on the neutral point potentials are analyzed to determine the starting vector. The time duration of the redundant small voltage vector is changed by adjusting the balancing control factor in order to make the fluctuations of the neutral point potential be zero in a switching cycle. Finally, it is analyzed how to place the space vectors in a switching cycle to achieve the best output harmonic characteristics. The proposed method is based on a simplified SVPWM algorithm [18], [19], which can identify the desired switching combinations of the synthetic reference voltage vectors and the time durations of the space vectors without complex judgment of the sectors or calculation of the time duration. Simulation and experimental results verify the proposed method.

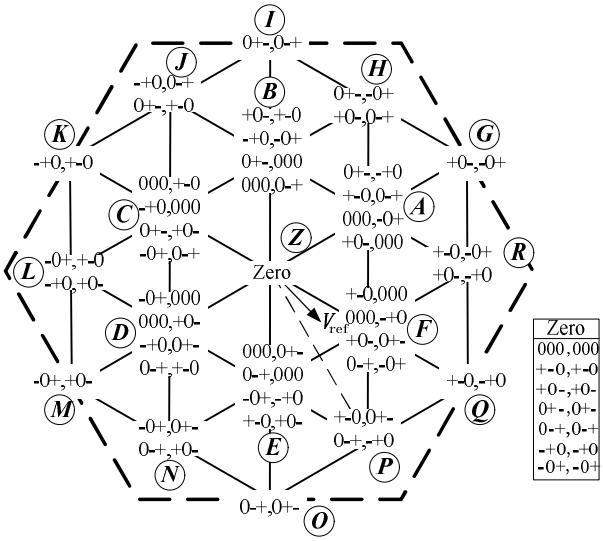


Fig. 2. Diagram of switching combinations and voltage space vectors for the dual-three inverter with common mode voltage elimination.

## II. Strategy for Common Mode Voltage Elimination

The common mode voltage output by the PWM inverter is defined [8] as:

$$V_{com} = (V_a + V_b + V_c)/3 \tag{1}$$

According to (1), the common mode voltage of open-ended winding induction motor drives is defined as:

$$V_{com} = (V_{A1} + V_{B1} + V_{C1} - V_{A2} - V_{B2} - V_{C2})/3 \tag{2}$$

where $V_{A1}$ denotes the pole voltage of the A phase bridge arm of Inverter I in Fig. 1, that is, the voltage difference between point A1 and point O. Similarly, $V_{A2}$, $V_{B1}$, $V_{B2}$, $V_{C1}$ and $V_{C2}$ denote the corresponding pole voltages of the corresponding bridge arms of the corresponding inverters, respectively. Only the zero common mode voltage vectors, which do not generate any common mode voltage at the inverter poles, are adopted [16]. A diagram of the switching combinations and

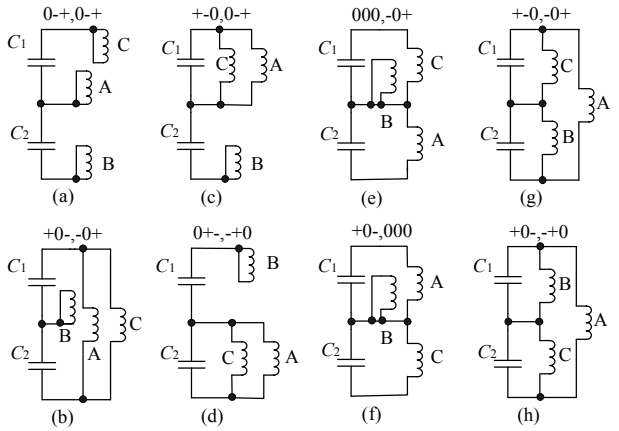


Fig. 3. Phase winding connections to the DC-link capacitors for various vector groups. (a) ZV. (b) LV. (c) USV. (d) LSV. (e) NSV. (f) NSV. (g) MV. (h) MV.

TABLE I
EFFECT OF VARIOUS VECTOR GROUPS ON CAPACITOR VOLTAGES

| Voltage vectors | Capacitor $C_1$ | Capacitor $C_2$ |
|---|---|---|
| ZV | No effect | No effect |
| NSV | Less effect of charging and discharging | Less effect of charging and discharging |
| USV | Discharging | Charging |
| LSV | Charging | Discharging |
| MV | Less effect of charging and discharging | Less effect of charging and discharging |
| LV | No effect | No effect |

voltage space vectors is shown in Fig. 2. The switching states "+", "0" and "-" in the figure indicate the inverter pole voltage level of $V_{dc}/2$, 0 and $-V_{dc}/2$, respectively. The first switching state (before the comma) in each switching combination indicates the switching state of Inverter I, and the second indicates the switching state of Inverter II. Taking voltage vector ***G*** (+0-, -0+) as an example, according to (2), the common mode voltage generated by ***G*** is as follows:

$$V_{com} = [V_{dc}/2 + 0 - V_{dc}/2 - (-V_{dc}/2) - 0 - (V_{dc}/2)]/3 = 0$$

Similarly, for the other voltage vectors in the figure, the common mode voltages generated by them are also zero.

Since the common mode voltage is eliminated, two inverters in Fig. 1 can share one DC power supply, which simplifies the circuit topology, reduces the equipment cost and provides convenience in terms of the four-quadrant operation of the system.

## III. ZERO COMMON MODE VOLTAGE VECTORS AND THEIR IMPACT ON NEUTRAL POINT POTENTIAL

According to the classification method of the traditional three-level voltage vectors, the space voltage vectors in Fig. 2 can be divided into four categories [17]: namely, zero voltage vectors (ZV), small voltage vectors (SV), middle voltage vectors (MV) and large voltage vectors (LV). In addition, the small voltage vectors can be divided into three categories: upper small voltage vectors (USV), lower small voltage vectors (LSV) and normal small voltage vectors (NSV). There are two kinds of switching combinations in each normal small voltage vector. Thus, each small voltage vector has four kinds of switching combinations, each middle voltage vector has two kinds of switching combinations and each large voltage vector has only one switching combination. The connections between the three-phase windings of the motor and the DC-link capacitors are shown in Fig. 3.

Since the deviation of the neutral point potential is only affected by the current flowing through the neutral point [14], Fig. 3 shows that the ZV and LV have no effect on the neutral point potential, while the USV and LSV have the opposite effect on the neutral point potential. The two kinds of switching combinations in Fig. 3(e) and (f) of the same NSV have the opposite effect on the neutral point potential. Two kinds of switching combinations of the same MV also have the opposite effect on the neutral point potential. When a large current flows through the DC-link neutral point, the USV and LSV have a greater impact on the neutral point potential. When there is a difference in the current on the two windings connected with the upper and lower capacitors flowing through the neutral point, the NSV will have an impact on the neutral point potential. Therefore, when compared with the USV and LSV, the NSV have less impact on the neutral point potential. Comparing the phase winding connections to the capacitors for the MV and NSV, the MV and NSV have the same degree of influence on the neutral point potential. In summary, when the motor is in the electric state, the effects of various vectors on the neutral point potential (DC-link capacitor voltages) are shown in Table I.

## IV. STRATEGY FOR NEUTRAL POINT POTENTIAL BALANCING CONTROL

### *A. Analysis of the Neutral Point Potential Balancing Principle*

Neutral point potential balancing is measured by the voltage difference between the upper and lower DC-link capacitors, namely, $\Delta u_C = u_{C1} - u_{C2}$. If $\Delta u_C = 0$, the neutral point potential has no deviation. Referring to the direction of the DC-link neutral point current in Fig. 1, the fluctuations of the neutral point potential are jointly determined by the neutral point current $i_{np}$ and the value of the DC capacitor $C$ ($C = C_1 = C_2$) [17] and it can be expressed as:

$$\Delta u_C = \frac{1}{C}\int i_{np}(t)dt \tag{3}$$

The reference directions of the load current $i_a$、$i_b$ and $i_c$ are shown in Fig. 1. The neutral point current $i_{np}$ is expressed as:

$$\begin{aligned} i_{np} &= [1 - abs(S_a)]\cdot i_a + [1 - abs(S_b)]\cdot i_b \\ &+ [1 - abs(S_c)]\cdot i_c - [1 - abs(S_{aa})]\cdot i_a \\ &- [1 - abs(S_{bb})]\cdot i_b - [1 - abs(S_{cc})]\cdot i_c \end{aligned} \tag{4}$$

TABLE II
SELECTION OF REDUNDANT SWITCHING COMBINATIONS FOR VARIOUS VECTORS

| Conditions | $\lvert \Delta u_C \rvert \le U$ | | $\lvert \Delta u_C \rvert > U$ | |
|---|---|---|---|---|
| **Within switching cycle $T_S$** | **The first selection** | **The second selection** | **The first selection** | **The second selection** |
| ***Z*** | 000,000(ZV) | | | |
| ***A*** | +0-,000(NSV) | 000,-0+(NSV) | +-0,0-+(USV) | 0+-,-+0(LSV) |
| ***B*** | 0+-,000(NSV) | 000,0-+(NSV) | -+0,-0+(USV) | +0-,+-0(LSV) |
| ***C*** | -+0,000(NSV) | 000,+-0(NSV) | 0+-,+0-USV) | -0+,0-+(LSV) |
| ***D*** | -0+,000(NSV) | 000,+0-(NSV) | 0-+,+-0(USV) | -+0,0+-(LSV) |
| ***E*** | 0-+,000(NSV) | 000,0+-(NSV) | -0+,-+0(USV) | +-0,+0-(LSV) |
| ***F*** | +-0,000(NSV) | 000,-+0(NSV) | +0-,0+-(USV) | 0-+,-0+(LSV) |
| ***G*** | +0-,-0+(LV) | | | |
| ***H*** | 0+-,-0+(MV) | +0-,0-+(MV) | 0+-,-0+(MV) | +0-,0-+(MV) |
| ***I*** | 0+-,0-+(LV) | | | |
| ***J*** | 0+-,+-0(MV) | -+0,0-+(MV) | 0+-,+-0(MV) | -+0,0-+(MV) |
| ***K*** | -+0,+-0(LV) | | | |
| ***L*** | -+0,+0-(MV) | -0+,+-0(MV) | -+0,+0-(MV) | -0+,+-0(MV) |
| ***M*** | -0+,+0-(LV) | | | |
| ***N*** | -0+,0+-(MV) | 0-+,+0-(MV) | -0+,0+-(MV) | 0-+,+0-(MV) |
| ***O*** | 0-+,0+-(LV) | | | |
| ***P*** | 0-+,-+0(MV) | +-0,0+-(MV) | 0-+,-+0(MV) | +-0,0+-(MV) |
| ***Q*** | +-0,-+0(LV) | | | |
| ***R*** | +-0,-0+(MV) | +0-,-+0(MV) | +-0,-0+(MV) | +0-,-+0(MV) |

where *abs*(·) is the function for obtaining the absolute value; while $S_a$, $S_b$, $S_c$, $S_{aa}$, $S_{bb}$ and $S_{cc}$ denote the switching states of the three-phase bridge arms for Inverter I and II, respectively. Taking $S_a$ as an example, the values "1", "0" and "-1" correspond to the switching states "+", "0" and "-" shown in Fig. 2. By substituting the switching states of each vector in Fig. 2 into (4) and combining with (3), the same conclusion can be obtained, as shown in Table I.

Therefore, the redundant switching combinations of the SV and MV can be fully used to control the neutral point potential. Since the small voltage vectors are involved in the composition of the reference voltage vectors in each switching cycle, adjusting the time duration of the redundant SV within a switching cycle can make the fluctuations of neutral point potential become zero.

### *B. Method of Controlling the Neutral Point Potential Balancing*

According to the balancing control principle analyzed above, a control method based on the balancing control factor can be adopted to regulate the time duration of the redundant SV [20].

Assume the terminal point of the reference voltage vector $\boldsymbol{V}_{ref}$ is in the ZAB triangle area, as is shown in Fig. 2. The three interaction vectors involved in the composition of $\boldsymbol{V}_{ref}$ are ***Z***, ***A***, and ***B***, respectively. Suppose vector ***A*** is the starting small voltage vector. Each voltage vector is placed in a seven-segment pattern where there are seven switching combinations involved in each switching cycle, as is shown in Fig. 4(a). When the terminal point of the reference voltage vector $\boldsymbol{V}_{ref}$ is within the AGH triangle area, suppose vector ***A*** is the starting small voltage vector and the sequence of each vector is shown in Fig. 4(b).

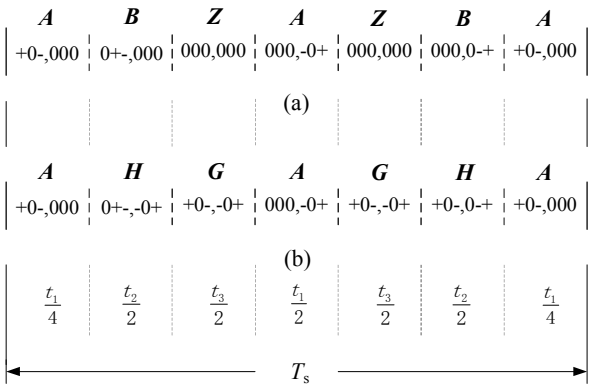


Fig. 4. Sequence and time durations of various vectors within one switching cycle.

The time durations of the three interaction vectors in Fig. 4 are $t_1$, $t_2$ and $t_3$, respectively. From left to right, suppose the corresponding neutral point currents, when each switching combinations works, are $i_{np1}$, $i_{np2}$, $i_{np3}$, $i_{np4}$, $i_{np5}$, $i_{np6}$ and $i_{np7}$, respectively. It can be obtained from (4) that $i_{np1} = i_{np7} = -i_{np4}$. To achieve a redistribution of the time duration of the SV, a neutral point potential balancing control factor $f$ is introduced. Taking the sequence in Fig. 4(a) as an example, suppose the time durations of the two switching combinations "+0-, 000" and "000, -0+" are respectively as follows:

$$t_1' = \frac{1+f}{2} t_1 \tag{5}$$

$$t_2' = \frac{1-f}{2} t_1 \tag{6}$$

According to the principle of charge conservation, the balancing control factor of the neutral point potential is derived as follows:

$$f = \frac{-C(u_{C1} - u_{C2})}{i_{\text{np1}} \cdot t_1} \tag{7}$$

It should be noted that $f$ is used to control the time durations of the redundant SVs. It can be obtained from (5) and (6) that $f$ must be constrained in [-1, 1], avoiding that the time duration could be negative. Therefore, when the calculated value for $f$ exceeds the constraint, the neutral point potential unbalancing cannot be completely controlled and it can only be improved to some extent.

To enhance the ability of the balancing control factor to the balance neutral point potential and to make the value of $f$ within the constraints as much as possible, the requirements for this SVPWM algorithm are as follows:

(a) If there are two SV involved in the composition of the reference voltage vectors, select the one whose angle with the reference vector is smaller as the starting small voltage vector. Taking the reference vector $\boldsymbol{V}_{\text{ref}}$, shown in Fig. 2, as an example, since the time duration of the small voltage vector $\boldsymbol{F}$ is larger than that of $\boldsymbol{E}$. Then select $\boldsymbol{F}$ as the starting small voltage vector, which can enhance the regulation ability of the balancing control factor $f$.

(b) The USV and LSV have a greater impact on the neutral point potential than the NSV. Thus, when the fluctuation $\Delta u_{\text{C}}$ is small, select the NSV as the interaction voltage vector, which will not make the fluctuations of the neutral point potential become too large. When $\Delta u_{\text{C}}$ is larger than the setting value $U$, select the USV and LSV as interaction voltage vectors, then a smaller value for $f$ can be used to balance the neutral point potential.

According to the above requirements, the selection of the redundant switching combinations for each voltage vector is shown in Table II. From Table II it can be seen that for the SV and MV, the effect of the switching combinations of the first selection and second selection on the neutral point potential balancing is different within a switching cycle $T_{\text{S}}$, while the ZV and LV have no impact on the neutral point potential. After a switching cycle by this mode of action, the deviation of the neutral point potential is very small. Thus, it is only needed to slightly adjust the time duration of the redundant switching combinations of the starting small voltage vector to balance the neutral point potential. The required value of $f$ is small. The value of $U$ in Table II is 2.

However, it can be known from (4) and (7) that when the load current is zero or approaching zero, $f$ becomes large. When it goes beyond the constraints, it will be constrained to within 1 or -1. It can be seen from Fig. 4 that the seven-segment pattern degenerates into a six-segment or five-segment pattern. This deteriorates the harmonic characteristics of the output waveforms. Thus, it needs to be further optimized. To improve the harmonic performance of the output waveform, the balancing control factor should be adjusted to obtain an optimized harmonic performance according to the theory of the quasi circular locus [21].

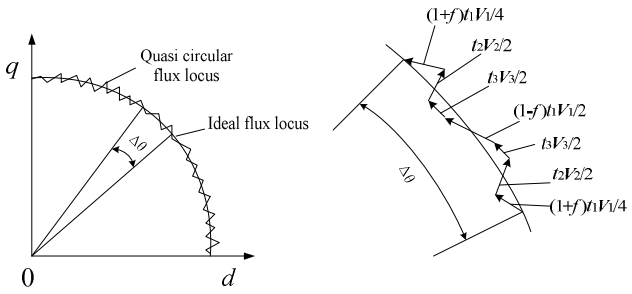


Fig. 5. Flux locus.

TABLE III

SELECTION OF VALUE FOR $f$

| Conditions | Selected value for $f$ |
|---|---|
| $f \geq 0.2$ | 0.2 |
| $0.1 < f < 0.2$ | 0.1 |
| $-0.1 \leq f \leq 0.1$ | $f$ |
| $-0.2 < f < -0.1$ | −0.1 |
| $f \leq -0.2$ | −0.2 |

## V. QUASI CIRCULAR LOCUS METHOD

Fig. 5 shows the locus of the time-voltage integral (i.e. flux) in the $d$-$q$ coordinate system. The ideal flux locus of the sinusoidal output voltage is a circle. However, the switching characteristics of the converter make the real locus become a quasi-circular locus as shown in Fig. 5. $\Delta\theta$ is an angle corresponding to a switching cycle, and the area between the flux locus of the voltage vectors and the ideal flux locus needs to be minimized. The smaller the area, the closer the quasi-circular flux locus is to the ideal flux locus.

Suppose voltage vectors $\boldsymbol{V}_1$, $\boldsymbol{V}_2$ and $\boldsymbol{V}_3$ are adopted and their corresponding time durations are $t_1$, $t_2$ and $t_3$, respectively. Then the time durations of each redundant switching combination for the various voltage vectors are described as follows:

$$\begin{aligned} T_{V_1(1)} &= \frac{1+f}{2} t_1 \qquad T_{V_1(2)} = \frac{1-f}{2} t_1 \\ T_{V_2(1)} &= T_{V_2(2)} = \frac{t_2}{2} \qquad T_{V_3(1)} = T_{V_3(2)} = \frac{t_3}{2} \end{aligned} \tag{8}$$

where $f$ is the balancing control factor, two redundant switching combinations of $\boldsymbol{V}_1$ occupy the first, the seventh, and the fourth segment of the switching cycle.

The deviation between the quasi circular locus and the ideal circular locus in each switching cycle provides a means to measure the harmonic distortion. In addition, the deviation can be obtained through calculating the area between the two loci of each switching cycle. Thus, the optimization problem becomes an approach to find a value for $f$, which will cut the area to a minimum to achieve an optimal modulation strategy.

According to [22], the optimum value of $f$ fluctuates

slightly around zero. Therefore, when the neutral point potential is balanced, the value of $f$ should be decreased as much as possible to obtain better harmonic performances. The selection of the value for $f$ is shown in Table III. The flowchart of the proposed control method is presented in Fig. 6.

## VI. Simulation and Experimental Results

In order to validate the correctness and effectiveness of the proposed SVPWM method with common mode voltage elimination and neutral point potential balancing, simulations and experiments have been implemented. The experimental parameters are listed in Table IV. A Texas Instruments TMS320F28335 floating point DSP (Digital Signal Processor) and an Altera FPGA (Field Programmable Gate Array) are adopted as the main algorithm controller. Vector control is adopted for the open-end winding induction motor drive to regulate the speed. The parameters for the simulation model are consistent with those in the experiments.

Figs. 7(a) and 7(b) show the waveforms of the common mode voltage both before and after eliminating the common mode voltage, respectively. According to (2), the common mode voltage can be expressed by the voltage difference between two DC links. After eliminating the common mode voltage, one DC power supply can be used to replace two DC power supplies in a dual-inverter drive system without increasing the output harmonic contents. Therefore, zero-sequence reactors are not needed to suppress the output common mode voltage. However, after elimination of the common mode voltage, whose value is zero in theory, the value of the common mode voltage in the dual-inverter system fluctuates around zero (Fig. 7(b)), due to the fact that the switching devices are not selected as the ideal switching devices in the simulation.

Fig. 8 shows the experimental results of the common mode voltage, whose value is not zero, with the proposed control method (Fig. 8(b)). There are several factors contributing to this phenomenon in the experiments and practical applications. Firstly, all of the switching devices, which have a time-delay problem of turning on and off, are not ideal switches. As a result, the switching operations of these switches are not completely consistent with the gating pulses generated by the DSP for the switching devices. Secondly, the deadband time, which is used to prevent the DC power supply from the short-circuit operation, is added to the gate signals generated by the DSP for the switches. Finally, the time delay of the gate signals received by the switching devices may exist in the drive system due to the control and main circuit design. However, as previously mentioned, the former two cases as are unavoidable. With a sensible design of the control and main circuit, such as making all of the gate signals completely consistent with the ideal signals produced by the proposed SVPWM method, except for the delay of deadband time, with the timing control module in the FPGA, and ensuring that all of the electronic elements involved in the transmission of the gate signals have the same specifications, the impact caused by the last factor can be eliminated. It can be seen from Figs. 7(b) and 8(b) that the

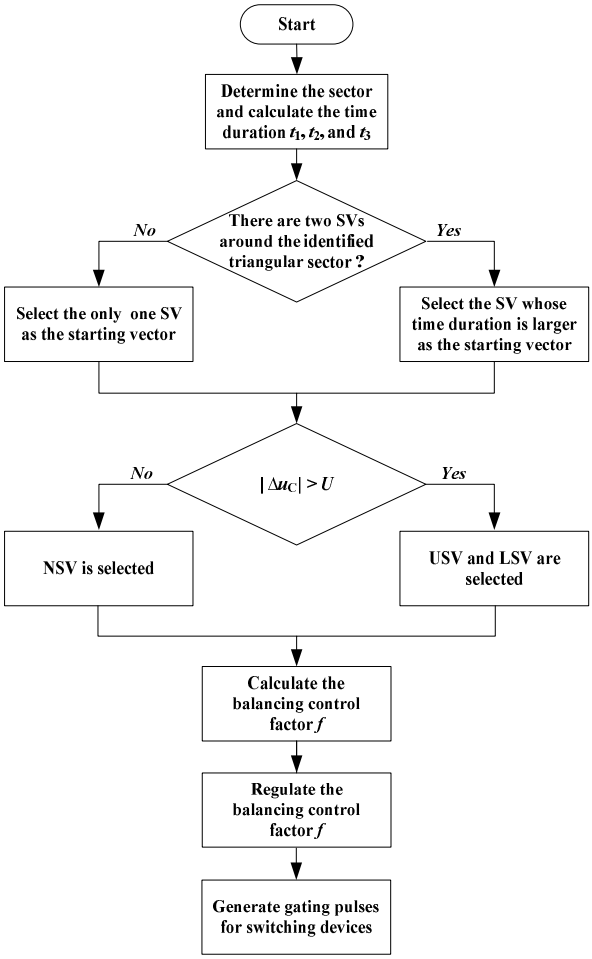


Fig. 6. Control block diagram of the proposed scheme.

TABLE IV

Experimental Parameters

| | |
|---|---|
| DC-link voltage | 400 V |
| DC-link capacitor | $C_1$=$C_2$=2200μF |
| Rated speed of motor | 1420 rpm |
| Number of pole-pairs | 2 |
| Rated power of motor | 5 kW |
| Rotor resistance of motor | 1.45 Ω |
| Stator resistance of motor | 1.91 Ω |
| Rotor inductance of motor | 0.24939 H |
| Stator inductance of motor | 0.24939 H |
| mutual inductance between stator and rotor | 0.23507 H |
| Load torque | 7.5 N·m |
| frequency of output voltage | 50 Hz |
| Carrier frequency | 5 kHz |
| Deadband time for gating pulses | 4 μs |

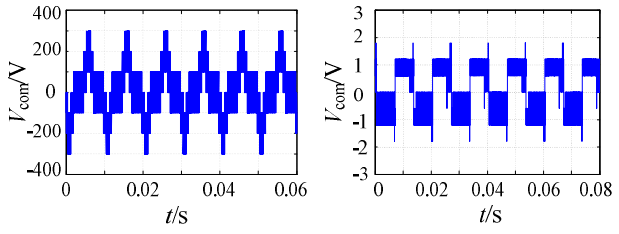


Fig. 7. Simulation waveforms of common mode voltage in the dual-inverter system. (a) before the elimination of common mode voltage. (b) after the elimination of common mode voltage.

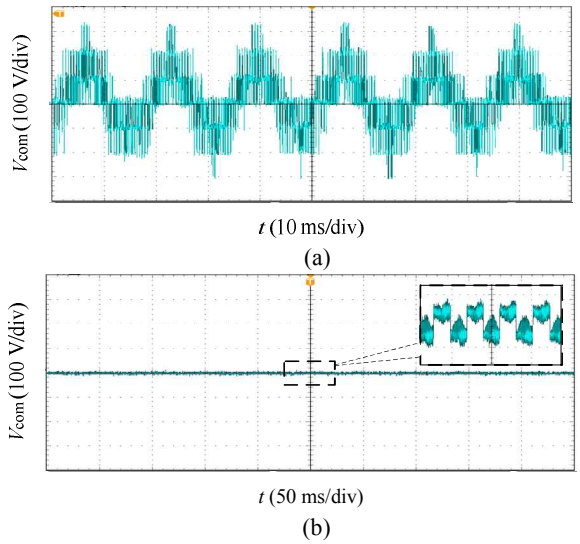


Fig. 8. Experimental waveforms of common mode voltage in the dual-inverter system. (a) before the elimination of common mode voltage. (b) after the elimination of common mode voltage.

common mode voltage caused by several inevitable factors is so small that it can be ignored.

Fig. 9(a) shows the volatility curve of the DC-link neutral point potential when the motor starts up and operates stably. When the motor starts up, the fluctuation of the neutral point potential is larger than that of the stable operation. The motor reaches the rated speed at around 0.75s. During stable operation, the neutral point potential fluctuates within a range of ±0.3V. The neutral point potential balancing control is not adopted at 1.2s and recovered at 1.4s. After recovering the control, the neutral point potential soon regains balancing. Fig. 9(b) presents the experimental waveforms of the two DC-link capacitor voltages, when the motor operates at the rated speed. When the neutral point potential balancing control is adopted, the waveforms of the two capacitor voltages are basically coincident. Otherwise, they will respectively shift in the opposite direction. After regaining control, the two capacitor voltages tend to be equal. Therefore, the effectiveness of the neutral point potential balancing proposed in this paper is verified.

Fig. 10 shows the simulation waveforms of the phase voltage and phase current before and after optimization, respectively. Fig. 11 presents the corresponding experimental

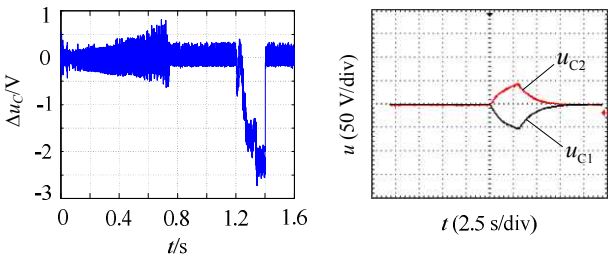


Fig. 9. Volatility curves of the DC-link neutral point potential. (a) simulation waveform of the difference of two DC-link capacitor voltages. (b) experimental waveforms of two DC-link capacitor voltages.

waveforms. By comparison, it can be seen that the total harmonic content of the optimized phase voltage has been reduced from 28.19% to 20.10%. The current waveform becomes smoother and the harmonic characteristics of voltage and current are improved. Thus, the correctness of the quasi circular locus theory is verified.

By appropriately adjusting the balancing control factor $f$ according to the quasi circular locus theory within each switching cycle, it can be seen that it does not need to be very precise to select the value of $f$. For example, when the calculated value of $f$ is greater than 0.2, $f$ will be forced to be 0.2. Taking into account that the calculation of $f$ needs load current, the control system will lower the accuracy requirements for the sampling current, which is the advantage of the method proposed in this paper. The simulation verification has been implemented and a high-frequency oscillator signal is added to the sampling signals of the load current to simulate the interference signal. Fig. 12 shows the phase current waveforms before and after adding the interference signal. A sinusoidal signal with an amplitude of 2 and a frequency of 1000Hz is added at 1.2s. A triangular wave signal with an amplitude of 2 and a frequency of 1000Hz is added at 1.24s. By comparison, it can be seen that the output current waveforms are almost the same after adding the interference signals. Fig. 13 shows the corresponding experimental waveforms. The interference method applied to the experiment adjusts the gain and offset values of the sampling current signals, to reduce the accuracy. The gain does not affect the neutral point potential balancing and the quality of the output waveforms in a wide range of variation. However, the change of the offset value should not be too large. An extreme situation would make the current sampling signal become a DC signal. Thus, the method proposed in this paper has a certain capability for anti-interference.

## VII. Conclusions

The configuration of a dual NPC three-level inverter for open-end winding induction motor drives can be equivalent to a five-level inverter topology and the output waveforms

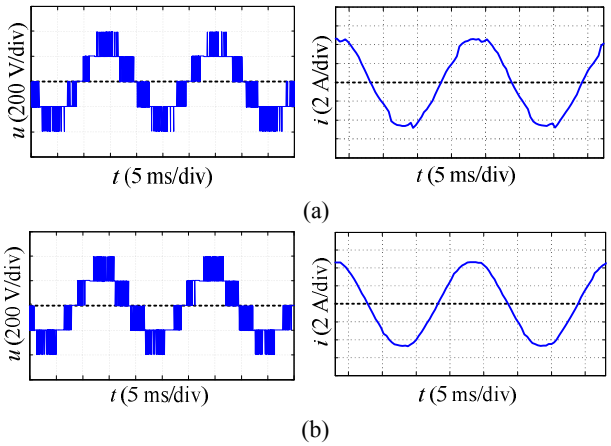


Fig. 10. Simulation waveforms of motor-phase voltage and current. (a) before the optimization. (b) after the optimization.

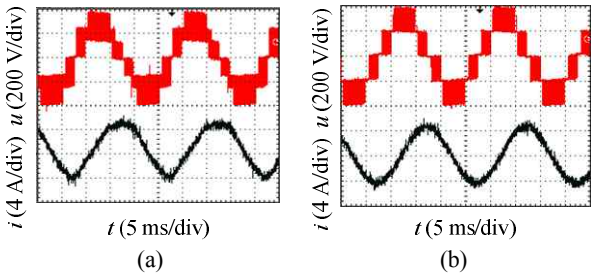


Fig. 11. Experimental waveforms of motor-phase voltage and current: (a) before the optimization, (b) after the optimization.

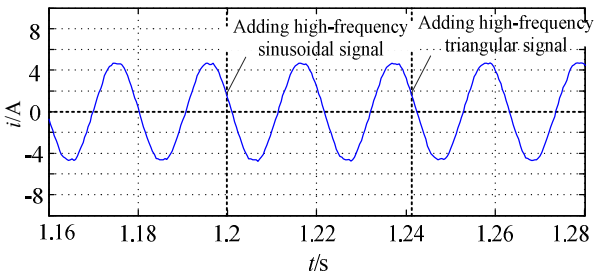


Fig. 12. Phase-current waveform of motor before and after adding interference signals to current sampling signals.

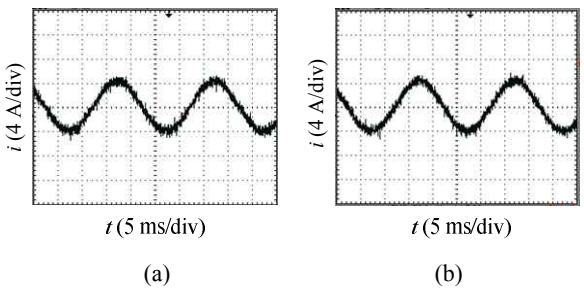


Fig. 13. Phase-current experimental waveforms of motor: (a) before adding interference, (b) after adding interference.

contain low harmonic components. On the basis of the same voltage rating of the switching devices, a higher output voltage can be obtained. In terms of this topology, the advantages of the method proposed in this paper are as follows:

1) Only zero common mode voltage vectors are adopted to achieve the purpose of common mode voltage elimination. Two inverters share one common DC power supply to supply power and zero-sequence reactors are not needed, which simplifies the topology, reduces the cost of the drive system and makes the four-quadrant operation of the motor easier.
2) Based on the complete elimination of common mode voltage, by reasonably arranging the action sequences of the redundant switching combinations in each switching cycle, both the ability of the balancing control factor to regulate the neutral point potential balancing and the minimization of the fluctuations in the neutral point potential are developed.
3) The method of the quasi circular locus is adopted to adjust the balancing control factor, which optimizes the output waveforms and reduces the requirements for the accuracy of the sampling signal of the current in the system.

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