Design and Implementation of a New Multilevel DC-Link Three-phase Inverter

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Abstract

This paper presents a new configuration for a three-phase multilevel voltage source inverter. The main bridge is built from a classical three-phase two-level inverter and three bidirectional switches. A variable DC-link employing two unequal DC voltage supplies and four switches is connected to the main circuit in such a way that the proposed inverter produces four levels in the output voltage waveform. In order to obtain the desired switching gate signals, the fundamental frequency staircase modulation technique is successfully implemented. Furthermore, the proposed structure is extended and compared with other types of multilevel inverter topologies. The comparison shows that the proposed inverter requires a smaller number of power components. For a given number of voltage steps N, the proposed inverter requires $N/2$ DC voltage supplies and $N+12$ switches connected with $N+7$ gate driver circuits, while diode clamped or flying capacitor inverters require $N-1$ DC voltage supplies and $6(N-1)$ switches connected with $6(N-1)$ gate driver circuits. A prototype of the introduced configuration has been manufactured and the obtained simulation and experimental results ensure the feasibility of the proposed topology and the validity of the implemented modulation technique.

Key words: Fundamental frequency staircase modulation, Multilevel DC-link, Multilevel inverter, Unequal DC voltage supplies

I. INTRODUCTION

Due to their significant role in improving power quality, various multilevel inverter topologies and a wide variety of modulation and control strategies have been suggested in the recent literature [1]-[3]. Lower voltage distortion, lower common mode voltages and reduced dv/dt are the main advantages of multilevel inverters. Multilevel technology started with the three-level converter followed by numerous multilevel converter topologies. Diode-clamped or neutral-point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) converters were introduced to take the place of classical two-level inverters [4]-[6]. In addition to

these three basic topologies, other multilevel inverter configurations have been reported in [7]-[9]. Symmetrical and asymmetrical cascaded multilevel inverters and hybrid multistage topologies have become some of the most popular research areas. When compared with symmetrical topologies, the asymmetrical cascaded topologies which use unequal DC voltage supplies offer a good opportunity to increase the number of levels with reduced THD%, switching losses, cost and size. Hybrid multistage converters consist of different multilevel configurations with unequal DC voltage supplies [10]-[17]. Furthermore, for some applications such as photovoltaic power systems and adjustable speed drives where the current is flowing in both directions, bidirectional switches are preferred. Different ways of constructing these types of switches are presented and employed in single-phase and three-phase converters [18]-[22]. Bidirectional switches play an integral role in multilevel converters since they help in reducing the number of switches and capacitors and achieving the maximum output voltage steps with a minimum standing voltage on the switches. The high numbers of required switches, clamping diodes, clamping capacitors and gate driver circuits

as well as the deviating voltage at the neutral-point remain distracting features in NPC and FC multilevel inverters. As a result of increasing the number of voltage steps N, the number of utilized DC voltage supplies increases to N-1 and the required number of switches increases to $6(N$-1) connected with a similar number of gate driver circuits in these inverters. In this paper, a new type of multilevel inverter based on a combination of the conventional two-level bridge and three bidirectional switches is suggested. A variable DC-link using two unequal DC voltage supplies and four switches is arranged to feed the main inverter bridge. When compared with NPC and FC inverters, the proposed inverter can considerably reduce the required number of DC voltage supplies to $N/2$ and the required number of switches to N+12 connected with N+7 gate driver circuits. This paper is organized as follows: the proposed inverter power circuit with its operation principle is presented in section II. In section III, different methods for determining the magnitudes of the utilized DC voltage supplies in the extended structure are suggested. The experimental results are verified and comprehensively discussed in section IV. Finally, some conclusion are given in section V.

II. PROPOSED TOPOLOGY AND OPERATION PRINCIPLE

Fig. 1 shows the configuration of the proposed three-phase four-level multilevel inverter. The proposed topology is made of two circuits. The main circuit is a combination of a conventional three-phase two-level bridge (Q1, Q2, Q3, Q4, Q5, Q6) and three bidirectional switches (S1, S2, Da1, Da2), (S3, S4, Db1, Db2), (S5, S6, Dc1, Dc2). Each bidirectional switch consists of two IGBT switching devices and two diodes. The function of these switches is to block high voltage levels and to conduct the load current in both directions. A multilevel DC-link makes use of two unequal DC voltage supplies ($Vmain = 3Vdc$, $Vaux = Vdc$) and four switches (T1, T2, T3, T4) are connected to the +, - and mid-point (o) bridge terminals. The voltage rating of the conventional bridge switches is $3Vdc$, while the voltage rating of the bidirectional switches is $2Vdc$. T1 and T2 have a voltage rating of $2Vdc$, while T3 and T4 have a voltage rating of Vdc.

The inverter line to ground voltage Vag and the conducting devices for all of the possible current directions are listed in Tables I and II, respectively. It is well known that the inverter line to ground voltages Vag, Vbg and Vcg are given by:

$$\begin{bmatrix} Vag \\ Vbg \\ Vcg \end{bmatrix} = \frac{3Vdc}{N-1} * \begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} \qquad (1)$$

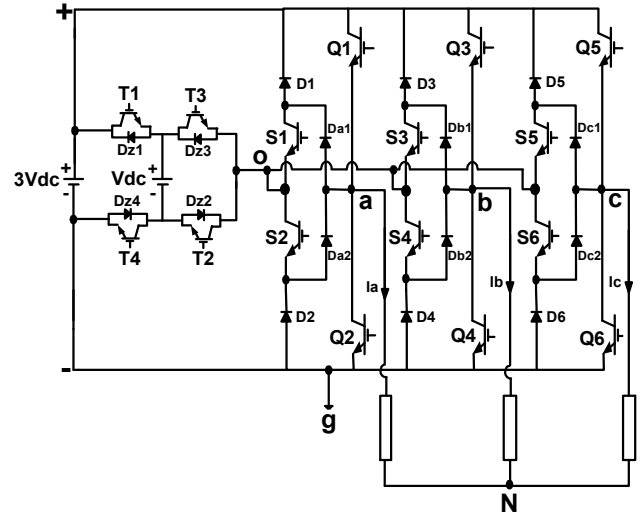And the inverter line to neutral (phase) voltages are related to line to the ground voltages by:

Fig. 1. Circuit diagram of the proposed three-phase four-level inverter.

TABLE I

SWITCHING STATE S_A AND INVERTER LINE TO GROUND VOLTAGE V_{AG}

Sa	Q1	S1	S2	Q2	T1	T2	T3	T4	Vag
3	on	off	off	off	on	on	off	off	+3Vdc
2	off	on	on	off	on	on	off	off	+2Vdc
1	off	on	on	off	off	off	on	on	+Vdc
0	off	off	off	on	off	off	on	on	0

TABLE II

CURRENT DIRECTIONS AND CONDUCTING DEVICES (LEG A)

Current	Conducting devices	Vag
Ia > 0	Q1	+3Vdc
	T1, Dz2, S2, Da2	+2Vdc
	Dz4, T3, S2, Da2	+Vdc
	D2, Da2	0
Ia < 0	D1, Da1	+3Vdc
	Dz1, T2, S1, Da1	+2Vdc
	T4, DZ3, S1, Da1	+Vdc
	Q2	0

$$\begin{bmatrix} VaN \\ VbN \\ VcN \end{bmatrix} = \frac{1}{3} * \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} * \begin{bmatrix} Vag \\ Vbg \\ Vcg \end{bmatrix} \qquad (2)$$

Where: $N = 4$ is the number of voltage levels and Sa, Sb and Sc are the switching states of phases a, b and c, respectively.

With the inverter switching states defined and the inverter line to neutral voltages determined, the next step is to arrange the switching sequence. The switching sequence and the corresponding inverter line to neutral voltages based on a three-phase balanced system are illustrated in Table III. It is

TABLE III

SWITCHING STATES SEQUENCE AND TRUTH TABLE OF THE PROPOSED INVERTER WITHIN ONE CYCLE

Sa Sb Sc	Q1	S1 S2	Q2	Q3	S3 S4	Q4	Q5	S5 S6	Q6	T1	T2	T3	T4	VaN	VbN	VcN
300	1	0	0	0	0	1	0	0	1	0	0	1	1	6Vdc/3	-3Vdc/3	-3Vdc/3
310	1	0	0	0	1	0	0	0	1	0	0	1	1	5Vdc/3	-Vdc/3	-4Vdc/3
320	1	0	0	0	1	0	0	0	1	1	1	0	0	4Vdc/3	Vdc/3	-5Vdc/3
330	1	0	0	1	0	0	0	0	1	1	1	0	0	3Vdc/3	3Vdc/3	-6Vdc/3
230	0	1	0	1	0	0	0	0	1	1	1	0	0	Vdc/3	4Vdc/3	-5Vdc/3
130	0	1	0	1	0	0	0	0	1	0	0	1	1	-Vdc/3	5Vdc/3	-4Vdc/3
030	0	0	1	1	0	0	0	0	1	0	0	1	1	-3Vdc/3	6Vdc/3	-3Vdc/3
031	0	0	1	1	0	0	0	1	0	0	0	1	1	-4Vdc/3	5Vdc/3	-Vdc/3
032	0	0	1	1	0	0	0	1	0	1	1	0	0	-5Vdc/3	4Vdc/3	Vdc/3
033	0	0	1	1	0	0	1	0	0	1	1	0	0	-6Vdc/3	3Vdc/3	3Vdc/3
023	0	0	1	0	1	0	1	0	0	1	1	0	0	-5Vdc/3	Vdc/3	4Vdc/3
013	0	0	1	0	1	0	1	0	0	0	0	1	1	-4Vdc/3	-Vdc/3	5Vdc/3
003	0	0	1	0	0	1	1	0	0	0	0	1	1	-3Vdc/3	-3Vdc/3	6Vdc/3
103	0	1	0	0	0	1	1	0	0	0	0	1	1	-Vdc/3	-4Vdc/3	5Vdc/3
203	0	1	0	0	0	1	1	0	0	1	1	0	0	Vdc/3	-5Vdc/3	4Vdc/3
303	1	0	0	0	0	1	1	0	0	1	1	0	0	3Vdc/3	-6Vdc/3	3Vdc/3
302	1	0	0	0	0	1	0	1	0	1	1	0	0	4Vdc/3	-5Vdc/3	Vdc/3
301	1	0	0	0	0	1	0	1	0	0	0	1	1	5Vdc/3	-4Vdc/3	-Vdc/3

worth noticing that, the proposed inverter operates in eighteen different modes within a full cycle of *VaN*, *VbN* and *VcN*. Among these eighteen modes, the three bidirectional switches only operate in twelve. Each of these bidirectional switches operates in four modes but their operating modes are totally different from each other. When the multilevel DC-link switches T1 and T2 are turned on, the other switches T3 and T4 operate in a complementary manner. As a result, they are turned off. Therefore, two different voltage levels *Vdc* and *2Vdc* are obtained at the mid-point with respect to the ground. Moreover, since some IGBT switching devices (for instance: S1 and S2 in leg a) always receive the same switching gate signals, the suggested configuration significantly contributes to a reduction in both the number of gate driver circuits and the system complexity. The inverter line to line voltages based on the line to neutral voltages are calculated as:

$$\begin{bmatrix} Vab \\ Vbc \\ Vca \end{bmatrix} = \begin{bmatrix} VaN - VbN \\ VbN - VcN \\ VcN - VaN \end{bmatrix} \quad (3)$$

Typical inverter staircase waveforms of seven consecutive line to line voltage levels (+3Vdc, +2Vdc, +Vdc, 0, -Vdc, -2Vdc, -3Vdc) and their corresponding switching gate signals are shown in Fig. 2(a). Fig. 2(b) depicts a set of simulated waveforms for the proposed inverter where: *VxN* is the inverter line to neutral voltage, *Vxo* is the voltage at phase *x* with respect to the mid-point (o), *Vog* is the voltage at the mid-point with respect to the ground and *Vxg* is the inverter line to ground voltage. *x* represents the corresponding phase (a, b or c).

The fundamental frequency staircase modulation technique can be easily implemented for the proposed inverter. In order to generate the appropriate switching gate signals, a simple method based on determining the switching states *Sa, Sb* and *Sc* is used. According to Equation (1), there is a direct relationship between the inverter line to ground voltages and *Sa, Sb* and *Sc*. Therefore, the basic idea of the proposed method is to determine the switching state for each phase, which is based on the instantaneous inverter line to ground voltages. It is well known that, the reference line to ground voltages may be expressed as:

$$\begin{bmatrix} Vag\_ref \\ Vbg\_ref \\ Vcg\_ref \end{bmatrix} = \frac{Ma*3Vdc}{2} * \begin{bmatrix} \cos(wt) \\ \cos(wt - \frac{2\pi}{3}) \\ \cos(wt + \frac{2\pi}{3}) \end{bmatrix} + \frac{3Vdc}{2}\begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (4)$$

Where: *Ma* is the modulation index and (*wt*) is the electrical angle. Or:

$$\begin{bmatrix} Vag\_ref \\ Vbg\_ref \\ Vcg\_ref \end{bmatrix} = \frac{Ma*3Vdc}{2} * \begin{bmatrix} \cos(wt) \\ \cos(wt - \frac{2\pi}{3}) \\ \cos(wt + \frac{2\pi}{3}) \end{bmatrix} + \frac{3Vdc}{2} * \left[1 - \frac{Ma}{6}\cos(3wt) \right] * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (5)$$

According to Equation (5), it can be seen that the third harmonic component is added to the reference line to ground voltages. This addition may maximize the output voltage. The switching state for each phase is then determined by:

Fig. 2. (a) Switching gate signals and the inverter line to line voltages Vab, Vbc and Vca, (b) VxN, Vxo, Vog and Vxg.

Fig. 3. Sa, Sb and Sc determination.

$$\begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} = \operatorname{int} eger \left(\frac{N-1}{3Vdc} * \begin{bmatrix} Vag\_ref \\ Vbg\_ref \\ Vcg\_ref \end{bmatrix} \right) \qquad (6)$$

The inverter switching states and the switching sequence based on the proposed method are shown in Fig. 3. It is clearly shown that, the switching sequence is arranged with eighteen different modes leading the proposed inverter to achieve the required output voltage waveforms as designed in Table III.

The operation of the proposed inverter can be represented using a space vector diagram, where the magnitude and the location of each voltage vector are determined based on the magnitude of the d and q voltage components. For given

Fig. 4. Switching state vectors of the proposed inverter in d-q reference frame.

switching states, Vd and Vq are basically given as:

$$Vq = \frac{3Vdc}{3(N-1)}(2Sa - Sb - Sc) \qquad (7)$$

$$Vd = \frac{3Vdc}{\sqrt{3}(N-1)}(Sc - Sb) \qquad (8)$$

$$V = Vq - jVd \qquad (9)$$

The space vector trajectory of the proposed inverter is shown in Fig. 4.

III. EXTENDED STRUCTURE

The extended structure of the proposed inverter is shown in Fig. 5. It consists of two circuits: the main bridge and multilevel DC-link. The main bridge is built similar to the one discussed and shown in Fig.1, while the multilevel DC-link circuit is extended by adding (n) auxiliary DC voltage supplies and ($2n+2$) switches. This arrangement leads the proposed inverter to operate at higher power rates and more output voltage levels. Based on the desired number of voltage levels, three different methods can be followed to determine the magnitudes of the utilized DC voltage supplies.

1) First method:

The magnitudes of the auxiliary DC voltage supplies used in the multilevel DC-link circuit are determined as follows:

$$Vdc1 = Vdc \qquad (10)$$

$$Vdc2 = 2Vdc \qquad (11)$$

$$Vdcn = nVdc \qquad (12)$$

The magnitude of the main DC voltage supply is then adjusted at:

$$Vmain = (N-1)Vdc = (2n+1)Vdc \qquad (13)$$

With the staircase modulation technique, the number of operating modes that leads the proposed inverter to achieve the desired output voltages is given by:

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TABLE IV

DC VOLTAGE SUPPLIES REQUIREMENT AMONG THE PROPOSED METHODS

n	N	M	$Vmain$	1st Method $Vdc1, Vdc2,..Vdcn$	2nd Method $Vdc1, Vdc2,..Vdcn$	3rd Method $Vdc1, Vdc2,..Vdcn$
1	4	18	$3Vdc$	Vdc	Vdc	$2Vdc$
2	6	30	$5Vdc$	$Vdc, 2Vdc$	$Vdc, 3Vdc$	$2Vdc, 4Vdc$
3	8	42	$7Vdc$	$Vdc, 2Vdc, 3Vdc$	$Vdc, 3Vdc, 5Vdc$	$2Vdc, 4Vdc, 6Vdc$
4	10	54	$9Vdc$	$Vdc, 2Vdc, 3Vdc, 4Vd$	$Vdc, 3Vdc, 5Vdc, 7Vdc$	$2Vdc,4Vdc, 6Vdc, 8Vdc$
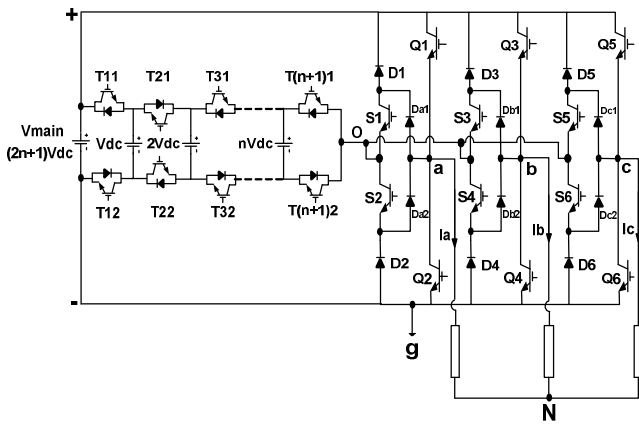
Fig. 5. Circuit diagram of the proposed three-phase N-level multilevel inverter (first method).

$$M = 6(N - 1) \qquad (14)$$

2) Second method:

$$Vdc1 = Vdc \qquad (15)$$

$$Vdc2 = Vdc + 2Vdc \qquad (16)$$

$$Vdcn = Vdc + 2(n-1)Vdc \qquad (17)$$

$$Vmain = (N-1)Vdc = (2n+1)Vdc \qquad (18)$$

$$M = 6(N-1) \qquad (19)$$

3) Third method:

$$Vdc1 = 2Vdc \qquad (20)$$

$$Vdc2 = 2Vdc + 2Vdc \qquad (21)$$

$$Vdcn = 2Vdc + 2(n-1)Vdc \qquad (22)$$

$$Vmain = (N-1)Vdc = (2n+1)Vdc \qquad (23)$$

$$M = 6(N-1) \qquad (24)$$

It can be seen that the maximum number of voltage levels N is equal to the total number of switches used in the multilevel DC-link circuit as:

$$N = 2n + 2 \qquad (25)$$

Table IV compares the DC voltage supplies requirements among the proposed methods at the same number of output voltage levels.

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TABLE V

SIMULATION STUDY PARAMETERS

Nominal Frequency	R-L Load	Vdc
50 Hz	23 Ohm – 3 mH	30 V

TABLE VI

COMPARISON OF THE PROPOSED N-LEVEL INVERTER WITH THE EXISTING INVERTERS

| Converter type	NPC	FC	CHB	Proposed
No. Switches	$6(N-1)$	$6(N-1)$	$6(N-1)$	$N+12$
No. Diodes	$6(N-1)$	$6(N-1)$	$6(N-1)$	$N+12$
No. Clamping diodes	$6(N-2)$	0	0	0
No. Gate drivers	$6(N-1)$	$6(N-1)$	$6(N-1)$	$N+7$
No. DC supplies	$N-1$	$N-1$	$3(N-1)/2$	$N/2$
No. Balancing capacitors	0	$3(N-2)$	0	0
No. Control signals	$6(N-1)$	$6(N-1)$	$6(N-1)$	$N+7$

Based on Table IV above, it is can be seen that:

1) For all of the methods, the required number of DC voltage supplies is the same, resulting in the same number of voltage levels.

2) For all of the methods, the magnitudes of $Vmain$ are same.

3) Among these possible methods, the method with lowest DC voltage magnitudes (the first method) is preferred. For the purpose of verifying the validity of the proposed structure, a prototype for ($n = 2, 3$ and 4) is simulated. MATLAB software has been used for the simulation. The system parameters in the simulation are listed in Table V. The simulation results of six-level, eight-level and ten-level inverter line to line voltage waveforms based on the proposed structure and their corresponding switching gate signals are shown in Figs. 6(a), (b) and (c), respectively. Moreover, the voltage waveforms of VxN, Vxo, Vog and Vxg (x: a, b or c) for ($n = 2, 3$ and 4) are also shown in Figs. 6(d), (e) and (f), respectively.

It is clear that the proposed three-phase N-level inverter significantly reduces the required number of power components. For the same number of output voltage levels $N \in [4,6,8,...(2n+2)]$, Table VI and Fig. 7 summarize the required number of DC voltage supplies, switches, gate driver circuits, diodes, clamping diodes, and balancing capacitors for the proposed N-level inverter when compared with three existing inverter topologies NPC, FC and CHB. From Fig. 7, it can be seen that nearly half of the power components can be eliminated as N increases. For instance: for $N = 8$, seven voltage DC supplies, forty two switches and forty two gate
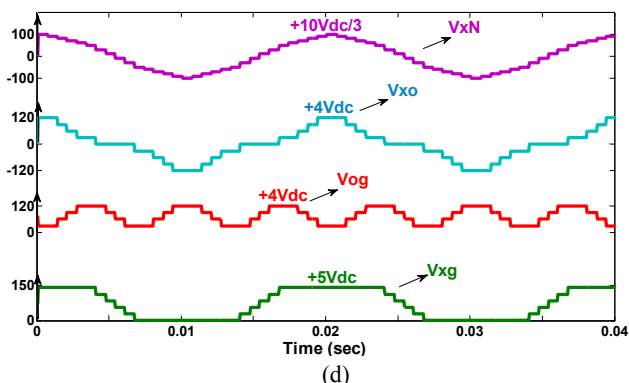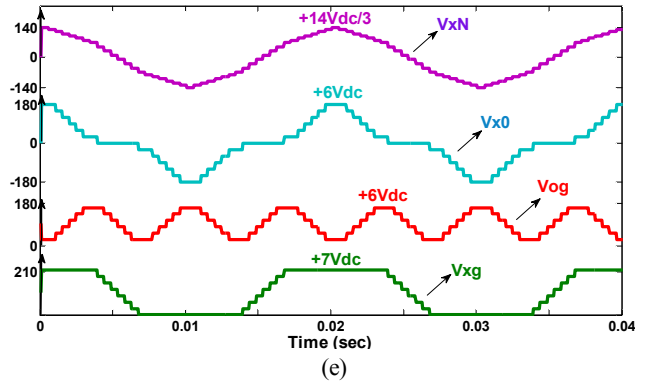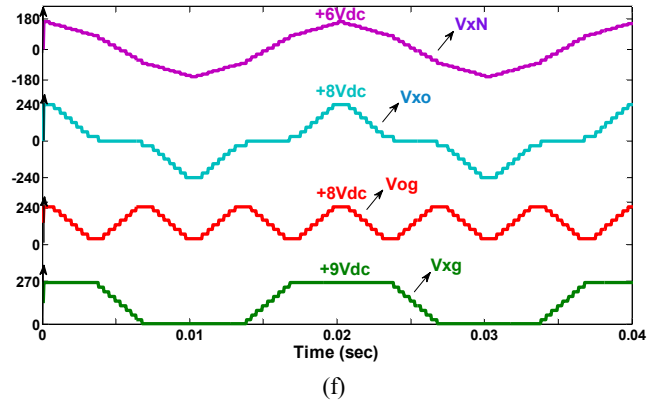
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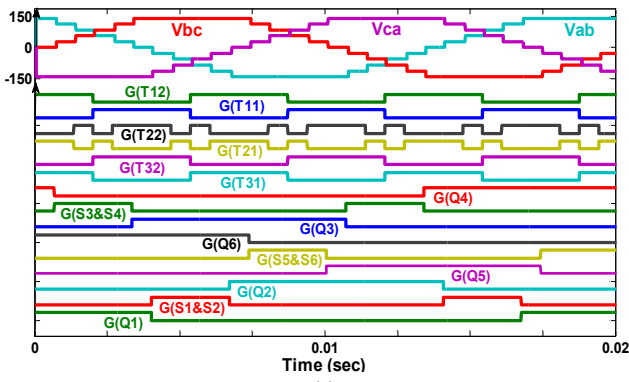
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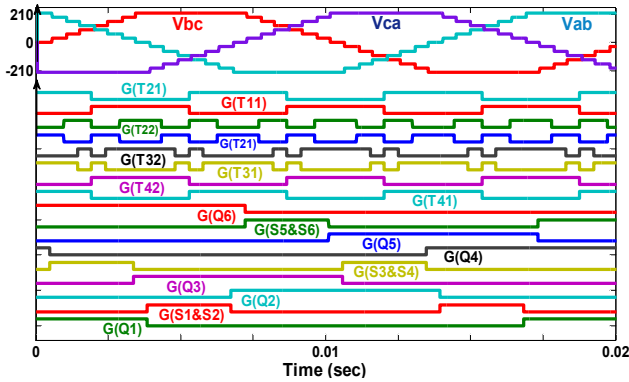
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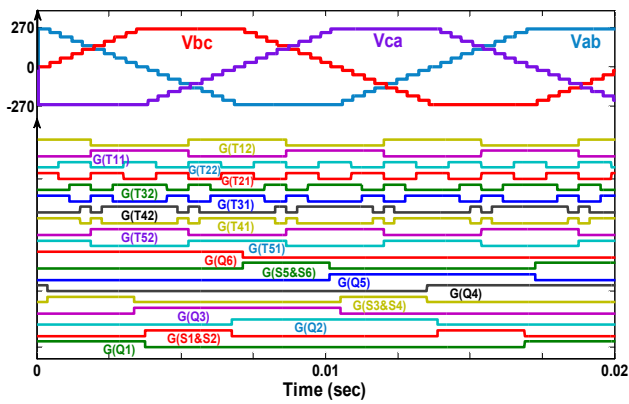
(c)

(d)

(e)

(f)

Fig. 6. Switching gate signals and inverter line to line voltage waveforms for (a) ($n = 2$, $N = 6$), (b) ($n = 3$, $N = 8$) and (c) ($n = 4$, $N = 10$). Simulated waveforms of *VxN*, *Vxo*, *Vog* and *Vxg* for (d) ($n = 2$, $N = 6$), (e) ($n = 3$, $N = 8$) and (f) ($n = 4$, $N = 10$).
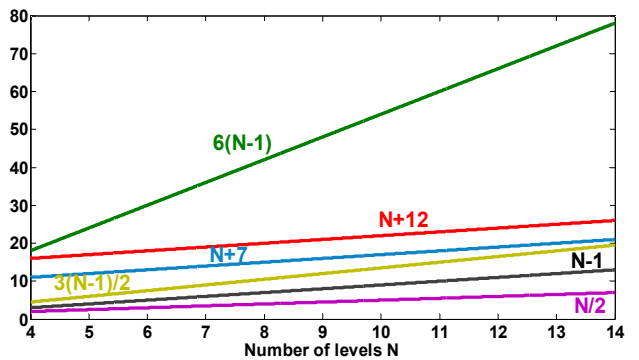

Fig. 7. Comparison of required number of power component (switches, diodes, gate drivers and DC supplies) among existing inverters and the proposed topology.

driver circuits are required for the existing inverters. However, only four voltage DC supplies, twenty switches and fifteen gate driver circuits are required for the proposed inverter structure.

In the three-phase topology recently introduced in [5], three multilevel DC-links were utilized to come up with eleven voltage levels. In order to reach this level count in three-phases, fifteen equal DC voltage supplies along with forty two switches are required. As *N* increases the required numbers of
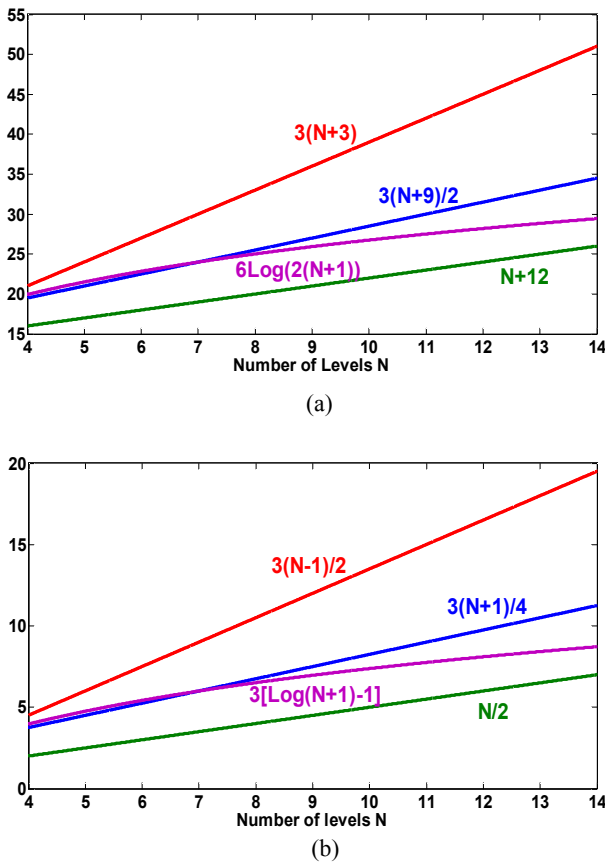
(a)

(b)

Fig. 8. Comparison of required number of (a) switches and (b) DC voltage supplies among the introduced inverters in [5] and [10] and the proposed topology.

DC voltage supplies and switches increase to $3(N-1)/2$ and $3(N+3)$, respectively. A new multilevel inverter topologies based on [5] were introduced in [10]. Different methods to determine the magnitudes of the DC voltage supplies were also suggested. More voltage levels with a smaller number of power components were obtained. For three-phase applications the mentioned power circuits need to be duplicated thrice. As a result, ($6\text{Log}_2[2(N+1)]$ or $3(N+9)/2$) switches with the same number of gate driver circuits and ($3[\text{Log}_2(N+1)-1]$ or $3(N+1)/4$) DC voltage supplies are required for such inverter topologies. When compared to the topologies introduced in [5] and [10], a substantial increment in the proposed inverter output voltage levels with a reduction in power electronics components is clearly shown in Figs. 8(a) and (b).

Since the cost and realization of an N-level multilevel inverter depend on the rated power, the voltage and current ratings of the power components are taken into consideration. In the suggested multilevel inverter topology, all of the power components have an equal current rating which is the rated current of the load IL. However, different voltage ratings based on the inverter structure, the utilized DC voltage supplies and the voltage stress are required as listed in Table VII.

TABLE VII

THE PROPOSED TOPOLOGY RATING REQUIREMENTS PER LEVEL N

Proposed inverter	Main bridge Q1~ Q6	Main bridge S1~ S6	DC-link T11~T(n+1)2 1st method
Switches voltage rating	$(N\text{-}1)Vdc$	$(N\text{-}2)Vdc$	$nVdc$
Active component current	IL	IL	IL

TABLE VIII

NPC, FC, CHB AND [5] RATING REQUIREMENTS PER LEVEL N

Converter type	NPC	FC	CHB	Proposed [5]
switches voltage rating	Vdc	Vdc	Vdc	$Vdc\sim(N\text{-}1)Vdc$
Clamping diodes voltage rating	Vdc	0	0	0
Clamping capacitor voltage rating	0	Vdc	0	0
Active component current	IL	IL	IL	IL

The power components' ratings for N-level NPC, FC, CHB inverters and the one proposed in [5] are listed in Table VIII. It can be seen that the introduced structure employs switching devices with high voltage ratings. This increases the cost of the components. Since the structure is introduced with a reduced number of switches, gate driver circuits and diodes, and no clamping capacitors or diodes are involved, the power components expenses are considerably recovered.

IV.   EXPERIMENTAL RESULTS

In order to verify the feasibility of the proposed topology, a prototype was manufactured. A Digital Signal Processor DSP was used to generate the appropriate switching gate signals. The multilevel DC-link was made of two DC voltage supplies $Vdc = 30$ V and $Vmain = 3Vdc = 90$ V. A three-phase series resistive-inductive load (20 Ohm – 3 mH/Phase) in a star connection was used. The fundamental frequency f = 50Hz staircase modulation technique was employed. The prototype of the proposed inverter, shown in Fig. 9, includes the following: two isolated DC voltage supplies with four switches, a main bridge, gate driver circuits, a three-phase resistive-inductive load, a TMS320F28335 DSP controller and a personal computer. Fig.10 shows a control block diagram of the inverter power circuit where Matlab/Simulink software is used to develop the inverter control algorithm using simulation and code generation. The output of the DSP controller is the IGBTs switching gate signals.
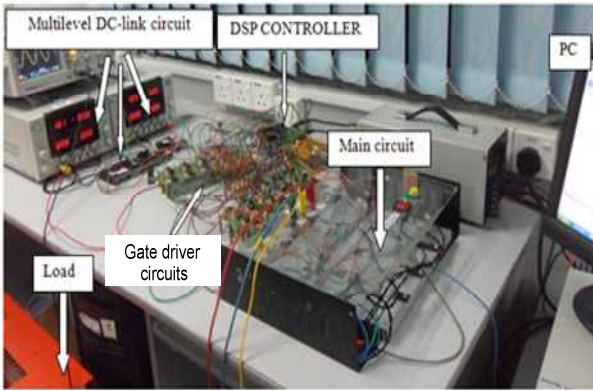
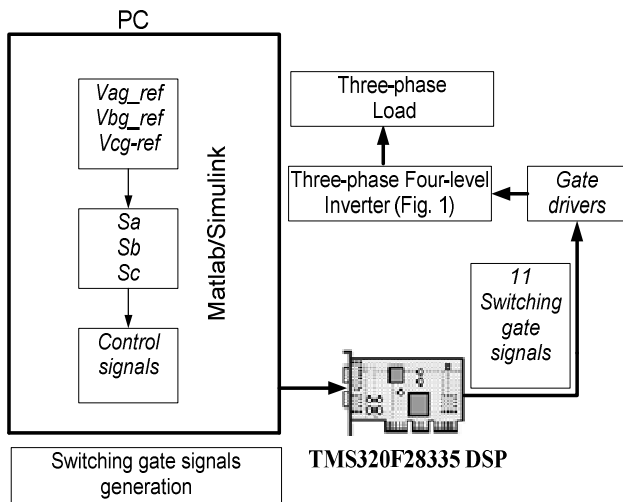Fig. 9. Prototype of the proposed three-phase four-level multilevel inverter.

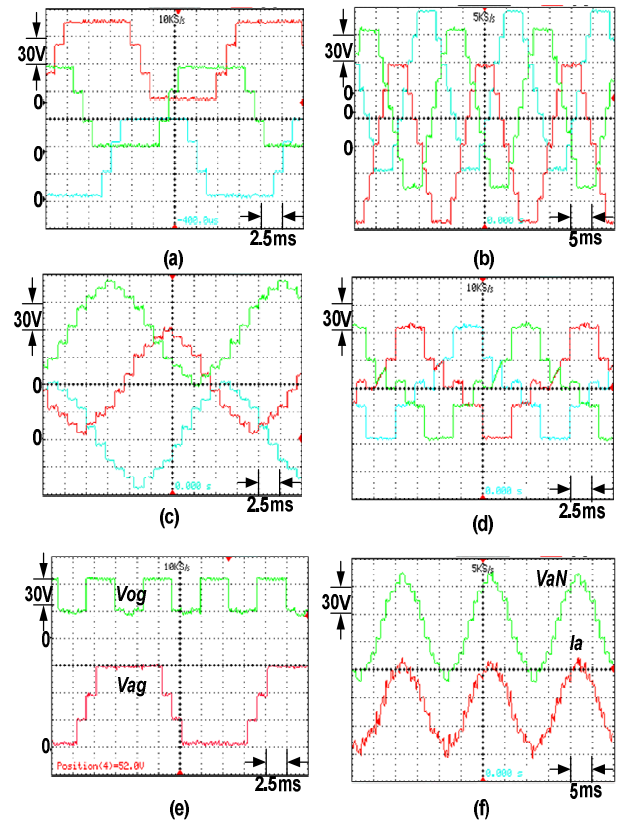Fig. 10. The control block diagram of the proposed inverter.

Fig. 11. Four-level inverter (a) line to ground voltages, (b) line to line voltages, (c) line to neutral voltages, (d) line to mid-point voltages, (e) line to ground Vag and mid-point to ground Vog voltages and (f) load current Ia and line to neutral voltage VaN.

The experimental results of the four-level inverter based on the proposed configuration are shown in Fig. 11, where the inverter line to ground voltage waveforms at $Ma = 1.15$ are shown in Fig. 11(a). It is clearly shown that the controller manages to generate appropriate switching gate signals that lead the inverter to output the desired voltage with four voltage levels. Figs. 11(b) and (c) depict the output voltage waveforms of the seven steps line to line and the output voltage waveforms of the ten steps line to neutral, respectively. The voltages at terminals a, b and c with respect to the mid-point are also obtained as shown in Fig. 11(d). Based on the shapes of Vag and Vog, Vog takes two different voltage values and repeats itself three times within a full cycle of Vag as shown in Fig. 11(e). Fig. 11(f) shows the experimental waveforms of the load current and line to neutral voltage of phase a. Furthermore, the total harmonic distortion THD% and frequency spectrum of the unfiltered line to line voltage are shown in Fig. 12. The graph contains the fundamental component and fourteen harmonic components. Due to the symmetry attained in the inverter output line to line voltage, all of the even harmonic components are nearly eliminated. Moreover, the triplen harmonic such as the 3rd, 9th and 15th are also eliminated.

Lower harmonic components lead to a lower THD%. The measured THD% is found to be around 9.4%. The measured (rms) value of the fundamental frequency component of the proposed inverter line to line voltage waveform Vab is 65.9 V. It is nearly $1.15*(0.612*3Vdc)$, where $(0.612*3Vdc) = 55.08$ V is the maximum (rms) value of the fundamental frequency component at $Ma = 1$. It can be seen that the (rms) value of the fundamental voltage shown in Fig. 12 is increased by 15% at a low THD%. The normalized value of the 5th harmonic component is $2.28/65.9 = 0.034$. The existing harmonic components such as the 5th, 7th, 11th and 13th can be eliminated by applying staircase modulation with selective harmonics. It is worth pointing out that the estimation of the optimal switching angles is not the goal of this study.

Experiments to investigate the feasibility of a six-level inverter based on the proposed structure, shown in Fig. 5, are carried out. Three DC voltage supplies $Vdc = 30$ V, $2Vdc = 60$ V and $Vmain = 5Vdc = 150$ V are connected with six switches to form a new multilevel DC-link. Under conditions similar to those of the circuit shown in Fig. 9, for the load and inverter control algorithm, Fig. 13 shows a set of experimental waveforms where the inverter line to line, line to neutral, line to mid-point, line to ground and mid-point to ground voltage
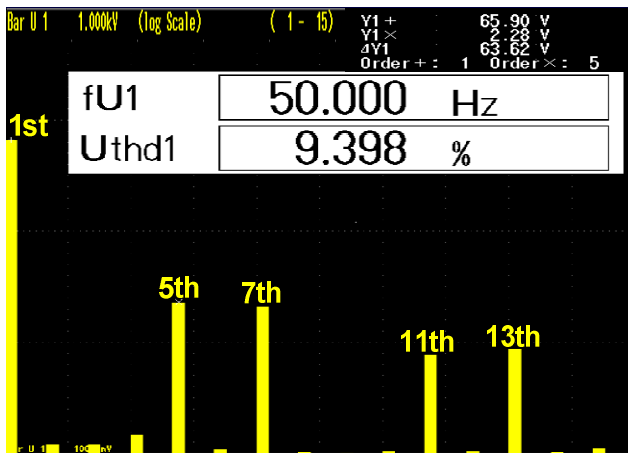
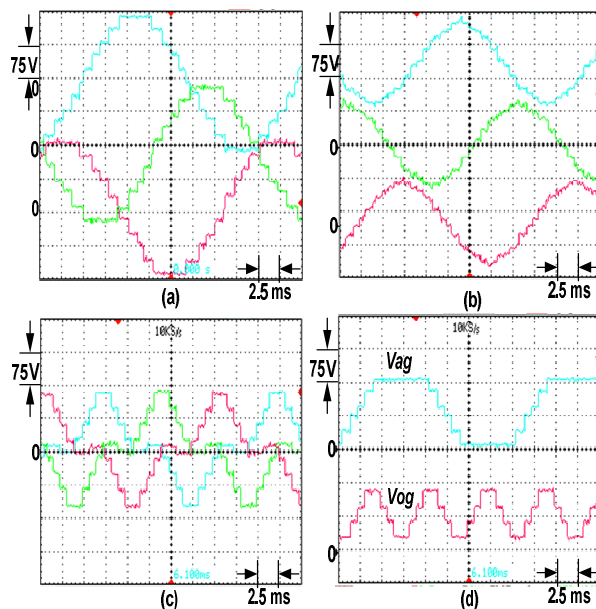Fig. 12.   Frequency spectrum of line to line voltage.

Fig. 13. Six-level inverter (a) line to line voltages, (b) line to neutral voltages, (c) line to mid-point voltages and (e) line to ground *Vag* and mid-point to ground *Vog* voltages.

waveforms are shown in Figs. 13(a), (b), (c) and (d), respectively. It is clearly shown that the inverter line to line output voltage reached its maximum value of 150 *V* with eleven steps as designed. Based on a comparison of the simulation and experimental results, it can be seen that both are in close agreement. Therefore, the proposed inverter is a promising configuration that may serve in many applications.

V.   CONCLUSIONS

In this paper a novel topology of a three-phase four-level multilevel inverter was presented. The proposed configuration came with a minimum number of DC voltage supplies and power electronic components. Therefore, the suggested topology results in reductions in terms of installation area and cost. The fundamental frequency staircase modulation technique was comfortably implemented and it showed high flexibility and simplicity in control. Moreover, the proposed configuration was extended to *N*-levels with different methods used for determining the magnitudes of the DC voltage supplies. Furthermore, for the purpose of verifying the performance of the new multilevel inverter, the proposed topology was simulated and a prototype was manufactured. The obtained simulation and experimental results met the desired output. Subsequent may include an extension to higher levels with other suggested methods.

REFERENCES

[1]   I. Colak, E. Kabalci, and R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes," *Energy Conversion and Management*, Vol. 52, No. 2, pp. 1114-1128, Feb. 2011.

[2]   J. Rodriguez, L. Jih-Sheng, and P. Fang Zheng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Appl.,* Vol. 49, No. 4, pp. 724-738, Nov. 2002.

[3]   L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, Vol. 2, No. 2, pp. 28-39, Jun. 2008.

[4]   I. Abdalla, J. Corda, and L. Zhang, "Multilevel DC-Link inverter and control algorithm to overcome the PV partial shading," *IEEE Trans Power Electron.,* Vol. 28, No. 1, pp. 14-18, Jan. 2013.

[5]   S. Gui-Jia, "Multilevel DC-link inverter," *IEEE Trans. Ind. Appl.,* Vol. 41, No. 3, pp. 848-754, May/Jun. 2005.

[6]   J. Rodriguez, S. Bemet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped Inverters," *IEEE Trans. Ind. Electron*, Vol. 57, No. 7, pp. 2219-2230, Jul. 2010.

[7]   L. Delmas, G. Gateas, T. A. Meynard, and H. Foch, "Stacked multicell converter (SMC): Control and natural balancing," in *PESC IEEE 33rd Annual,* Vol. 2, pp. 689-694, *2002.*

[8]   P. F. Zheng, "A generalized multilevel inverter topology with self voltage balancing" *IEEE Trans. Ind Appl.,* Vol. 37, No. 2, pp. 611-618, Mar./Apr. 2001.

[9]   B. Thomas and B. Steffen, "The active NPC converter for medium-voltage applications," *in Industry Applications Conference, Fourtieth IAS Annual Meeting,* Vol. 1, pp. 84-91, 2005.

[10]   E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," *Energy Convers. Manage.*, Vol. 50, No. 11, pp. 2761-2767, Nov. 2009.

[11]   H. Belkamel, S. Mekhilef, A. Masaoud, and M. Abdel Naiem, "Novel three-phase asymmetrical cascadedmultile

vel voltage source inverter," *IET Power Electronics,* Vol. 6, pp. 1696-1706, Sep. 2013.

[12] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new topology of cascaded multilevel converters with reduced number of components for high-voltage applications," *IEEE Trans Power Electron.,* Vol. 26, No. 11, pp. 3109-3118, Nov. 2011.

[13] M. K. Menshawi and S. Mekhilef, "Multistage inverters control using surface hysteresis comparators," *Journal of Power Electronics*, Vol. 13, No. 1, pp. 59-69 Jan. 2013.

[14] M. K. Menshawi, M. N. A. Kadir and S. Mekhilef, "Voltage vector approximation control of multistage-multilevel inverter using simplified logic implementation," *IEEE Trans.Ind informat.*, Vol. 9, No. 4, pp. 2052-2062, Nov. 2013.

[15] M. N. A. Kadir, S. Mekhilef, and H. W. Ping "Voltage vector control of a hybrid three-stage 18-level inverter by vector decomposition," *IET Power Electronics*, Vol. 3, No. 4, pp. 601-611, Jul. 2010.

[16] M. N. A. Kadir, S. Mekhilef, and H. W. Ping "Dual vector control strategy for a three-stage hybrid cascaded multilevel Inverter," *Journal of Power Electronics*, Vol. 10, No. 2, pp. 155-164, Mar. 2010.

[17] Y. Hinago and H. Koizumi, "A single phase multilevel inverter using switched series/parallel DC voltage sources," in *Energy Conversion Congress and Exposition, ECCE 2009. IEEE,* pp. 1962-1967, 2009.

[18] S. Mekhilef, and A. Masaoud, "Xilinx FPGA based multilevel PWM single phase inverter," in *IEEE International Conference on Industrial Technology, ICIT 2006*, pp. 259-264, 2006.

[19] H. W. Ping, N. A. Rahim, and J. Jamaludin, "New three-phase multilevel inverter with shared power switches," *Journal of Power Electronics*, Vol. 13, No. 5, pp. 787-797, Sep. 2013.

[20] E. Babaei, "A Cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.,* Vol. 23, No. 6, pp. 2657-2664, Nov. 2008.

[21] C. Klumpner, and F. Blaabjerg, "Using reverse-blocking IGBTs in power converters for adjustable-speed drives," *IEEE Trans. Ind. Appl.,* Vol. 42, No. 3, pp. 807-816, May/Jun. 2006.

[22] M.E.Ahmed and S.Mekhilef, "Design and implementation of a multilevel three-phase inverter with less switches and low output voltage distortion," *Journal of Power Electronics*, Vol. 9, No. 4, pp. 594-604, Jul. 2009.

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