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A New ZVS-PWM Full-Bridge Boost Converter

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Abstract

Pulse-width modulated (PWM) full-bridge boost converters are used in applications where the output voltage is considerably higher than the input voltage. Zero-voltage-switching (ZVS) is typically implemented in these converters. A new ZVS–PWM full-bridge converter is proposed in this paper. The proposed converter does not have any of the disadvantages associated with other converters of this type, including a complicated auxiliary circuit, increased current stresses in the main power switches, and load-dependent ZVS operation. The operation of the proposed converter, its steady-state characteristics, and its design are explained and examined. The feasibility of the converter is confirmed with results obtained from an experimental prototype.

Key words: Boost converter, DC–DC power conversion, Full-bridge, ZVS

I. INTRODUCTION

Current-fed PWM full-bridge boost converters, like the one shown in Fig. 1, are very attractive in applications where the required output DC voltage is considerably larger than the input voltage. Such applications include medical power supplies and power supplies for electrostatic applications requiring extremely high output voltages , as well as fuel cell and photovoltaic applications where the input voltage is very low. Standard voltage-fed PWM full-bridge converters that have a bulk capacitor at the input of the full-bridge are not typically used in these applications because a large turns ratio of the main power transformer is needed and this large ratio exacerbates the non-idealities of the transformer. In particular, leakage inductance and winding capacitance can significantly change the behavior of the converter by generating high voltage and current spikes.

A PWM full-bridge boost converter can be implemented with either zero-voltage switching (ZVS) [2]-[13] or zero-current switching (ZCS) [14]-[20] depending on the application. ZVS is implemented in applications where the input voltage is high, the input current is low or moderate, and the switch turn-on switching losses are dominant. ZCS is implemented in applications where the input current is high and the conduction losses are dominant. The focus of this paper is on ZVS-PWM full-bridge boost converters and is based on a study that was performed by the authors [1].

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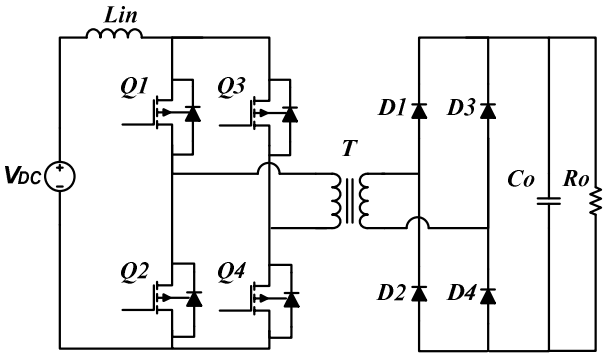


Fig.1. Current-fed PWM full-bridge boost converter.

Although the full-bridge boost converter shown in Fig. 1 is a boost converter and its operation is similar to that of a single-switch PWM boost converter (either the DC bus is shorted and the current in the input inductor L_{in} increases or the diagonally opposed switches are on and the current in L_{in} decreases while energy is being transferred to the output), a number of ZVS techniques that can be used in single-switch boost converters cannot be used in isolated boost full-bridge converters. The reason for this limitation in the applicability of ZVS techniques is the interaction between the output capacitances of the converter switches and the leakage inductance of the main power transformer. Unlike a single-switch PWM boost converter, the converter in Fig. 1 does not have a bulk capacitor across the DC bus whenever a switch is turned off. The only bulk capacitor in the circuit is at the secondary side of the converter, far from the converter switches. Unless the circuit in Fig. 1 is modified, the switches will experience high-voltage overshoots and ringing whenever

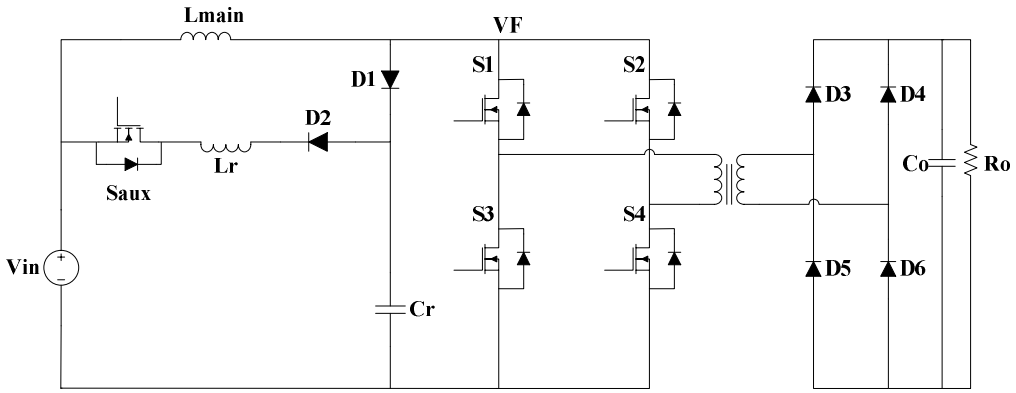


Fig. 2. Proposed ZVS full-bridge boost converter.

they are turned off. Such overshoots and ringing cannot be avoided in many ZVS techniques that can be used in single-switch PWM boost converters.

Despite this limitation, a number of ZVS-PWM current-fed boost full-bridge converters have been proposed. At present, these converters elicit considerable attention because of their use in various industrial applications, such as those mentioned above. Previously proposed converters of this type, however, have at least one of the following disadvantages:

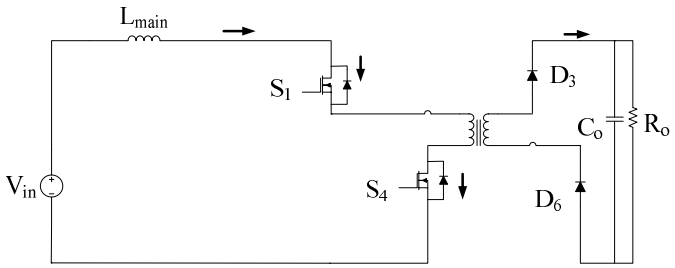
- The converter is a resonant converter [2]-[5] and therefore has the disadvantages associated with many resonant converters. Such disadvantages include the need for variable switching frequency control, which complicates the design of the transformer as it must be able to operate across a wide range of switching frequencies, and high circulating primary current, which increases conduction and turn-off switching losses. Although the converter becomes more efficient, if ZVS is not implemented, the gains in efficiency are not as much as what they could possibly be because of these losses.
- The converter is implemented with some sort of dissipative snubber at the DC bus to suppress voltage overshoots and ringing across the switches [6], [22]. Although the efficiency of these techniques is improved, the losses in the dissipative snubber limit the gains in efficiency.
- The converter is implemented with some sort of active auxiliary circuit that consists of an active device and a few passive components. The auxiliary circuit is connected parallel to the full bridge. It is used to discharge the switch output capacitances before the switches are turned on and is deactivated shortly afterward. The active switch in the auxiliary circuit, however, does not turn off softly and thus entails turn-off losses [7]. Again, these losses partially offset whatever gains in efficiency may be achieved by the reduction in the converter's turnon switching losses.
- The auxiliary circuit is an active clamp-type circuit [8]-[12], and although the converter operates with ZVS, its ZVS operation is load dependent and is lost at light loads. Moreover, the current stresses of the switches are higher than those of other PWM boost full-bridge converters because the switches must conduct current from the auxiliary circuit in addition to the input inductor current.

The converter's auxiliary circuit is very complicated and its cost is not negligible because it contains many components [13].

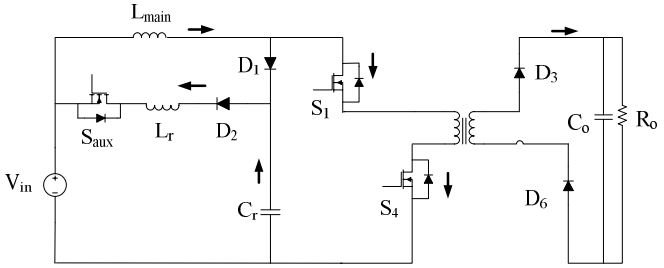
A new ZVS-PWM full-bridge boost converter (Fig. 2) with none of the disadvantages discussed above is proposed in this paper. The converter is specifically designed for applications that require a high step-up voltage ratio. In the paper, the operation of the proposed converter is explained in detail, and a mathematical analysis of its steady-state operation is performed. The results of the analysis are used to establish a procedure for the design of the converter. The feasibility of the converter is confirmed with results obtained from an experimental prototype.

II. CONVERTER OPERATION

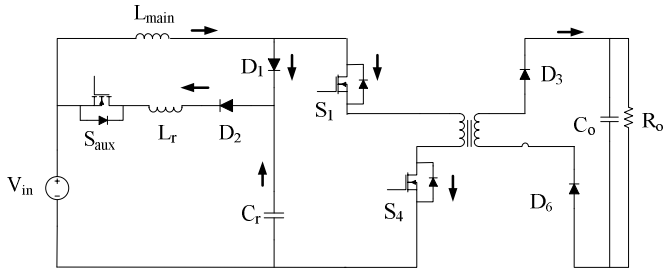
The proposed converter is a standard PWM full-bridge converter but with an auxiliary circuit that consists of auxiliary switch S_{aux}, snubber capacitor C_r, resonant inductor L_r, and two diodes D_1 and D_2. The sequence of gating signals that the converter operates with in a typical switching cycle is as follows: S_1 and S_4 on → all bridge switches on → S_2 and S_3 on → all switches on. In other words, an energy transfer mode, in which only a pair of diagonally opposed switches is on, is always followed by a "boosting" mode, in which all the switches are on and no energy is transferred. The basic principle behind the converter is that the auxiliary circuit is activated whenever two converter switches are about to be turned on to short out the DC bus. The switches turn off with ZVS because of the switch output capacitances (which may be a combination of internal and external capacitances) and capacitor C_r in the auxiliary circuit, which is larger than the switch output capacitances. The ZVS operation of the switches can be seen by considering the various modes of operation that the proposed converter undergoes during a half-switching cycle. The modes are as follows:



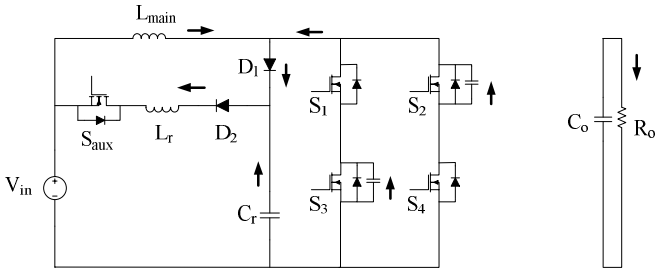
(a) Mode 0.



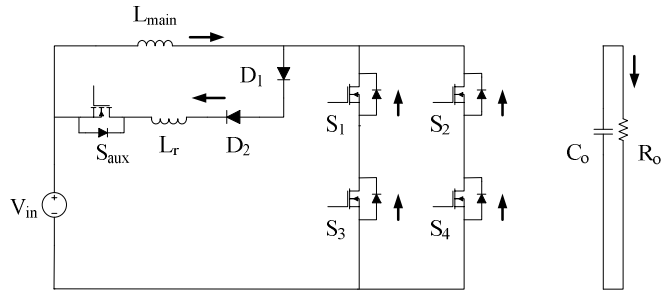
(b) Mode 1.



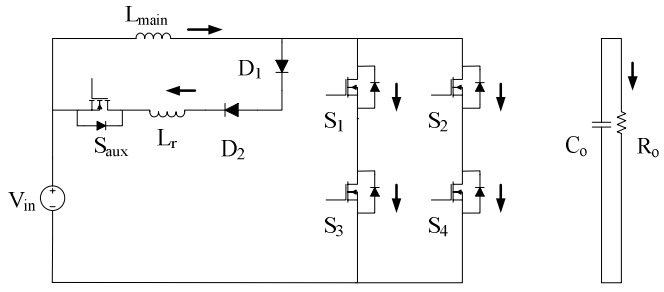
(c) Mode 2.



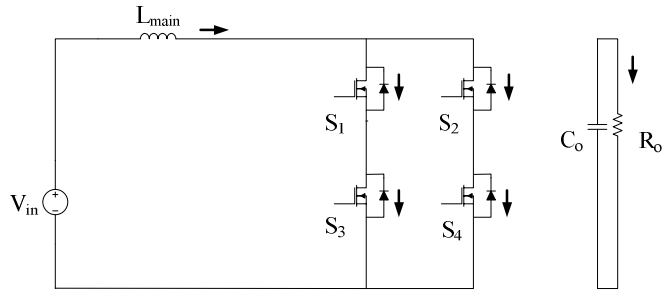
(d) Mode 3.



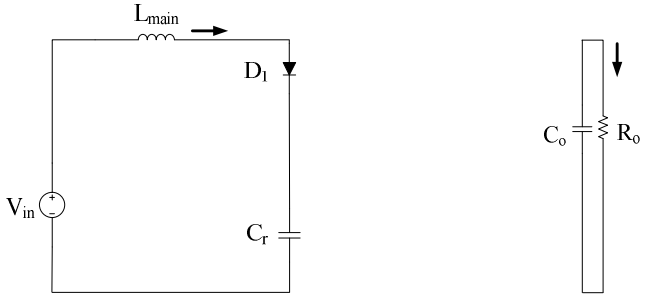
(e) Mode 4.



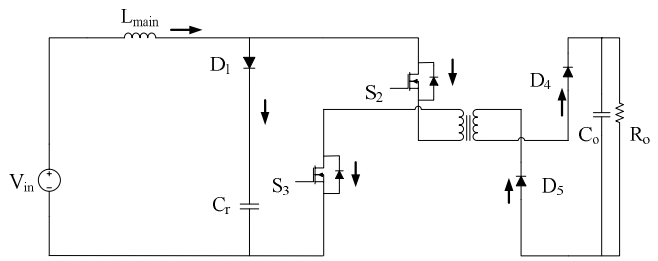
(f) Mode 5.



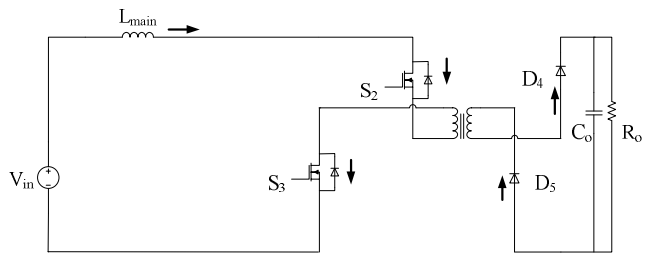
(g) Mode 6.



(h) Mode 7.



(i) Mode 8.



(j) Mode 9.

Fig. 3. Converter modes of operation.

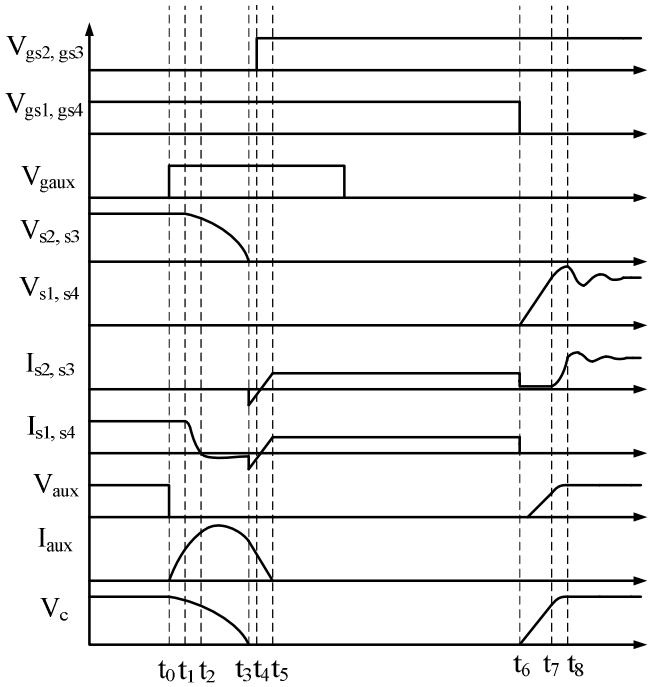


Fig. 4. Typical converter waveforms.

Mode 0 ($t< t_0$) (Fig. 3(a)): In this mode, only switches S_1 and S_4 are on. The converter is in an energy transfer mode as energy is transferred from the input to the output through diodes D_3 and D_6. The current through L_{main} decreases throughout this mode.

Mode 1 ($t_0<t<t_1$) (Fig. 3(b)): This mode begins when switch S_{aux} is turned on in anticipation of the DC bus being shorted and the converter entering a boosting mode. The current starts flowing through S_{aux} because snubber capacitor voltage V_{Cr} is greater than the input voltage. S_{aux} turns on softly given that inductor L_r is in series with this switch and limits the increase in current through it. C_r discharges into the auxiliary inductor during this mode. Diode D_1 is reverse-biased and does not conduct because voltage V_{Cr} is higher than the bridge voltage. This mode ends when C_r voltage reaches the voltage across the off-state bridge switches, which is $\frac{V_o}{N}$.

Mode 3 ($t_2<t<t_3$) (Fig. 3(d)): The output capacitances of switches S_2 and S_3 and capacitor C_r continue to discharge in this mode. The current in the auxiliary circuit branch is equal to the sum of the current from the full bridge caused by discharging the switch output capacitances and C_r and the input current that flows through L_{main}.

Mode 4 ($t_3< t < t_4$) (Fig. 3(e)): At the beginning of this mode, the DC bus voltage is zero and is clamped to zero as the body diodes of the converter switches are forward-biased and begin to conduct. Switches S_2 and S_3 can be turned on with ZVS sometime during this mode as the current flows through their body-diodes. Moreover, during this mode, the current that flows through the auxiliary circuit (and thus, the current through the full bridge) begins to decrease because the voltage across the auxiliary inductor is negative as the input voltage is at one end of the circuit and the DC bus voltage is zero. The auxiliary circuit current is equal to the current through L_{main} at the end of this mode; this condition makes the current flowing through the full bridge zero.

Mode 5 ($t_4< t < t_5$) (Fig. 3(f)): At $t = t_4$, the current flowing through the full bridge reverses its direction and flows through the switches. The current in the auxiliary circuit continues to decrease as the input current is gradually transferred to the full bridge. The auxiliary circuit current is zero by the end of this mode, and S_{aux} can be turned off softly at any time afterward until a diagonal pair of switches is turned off and the DC bus is no longer shorted.

Mode 6 ($t_5< t < t_6$) (Fig. 3(g)): The converter is in a boosting mode. It operates like a standard PWM boost converter as the DC bus is shorted. The current through L_{main} increases, and the auxiliary circuit is inactive.

Mode 7 ($t_6< t < t_7$) (Fig. 3(h)): At $t = t_6$, switches S_1 and S_4 are turned off. These switches can be turned off with ZVS because of the presence of their output capacitances (not shown in the figure) and C_r. The main switch output capacitances and C_r begin charging. At the end of this mode, their voltage reaches $\frac{V_o}{N}$.

Mode 8 ($t_7< t < t_8$) (Fig. 3(i)): At the beginning of this mode, as the DC bus voltage increases, the transformer primary-side voltage reaches a certain level and results in the output diodes becoming forward-biased and thus conducting current. The main inductor current transfer from snubber capacitor C_r to the transformer primary winding is gradual and requires some time because of the leakage inductance of the transformer. During this time, the current flowing through C_r results in the capacitor being charged over and above the DC bus voltage, which in turn results in voltage overshoots across the main full-bridge switches that are off. At the end of this mode, the voltage across C_r reaches its maximum value and is clamped at this value as no current path exists for it to discharge. In the meantime, the main switch output capacitances and capacitor C_r begin to resonate with the transformer leakage inductance at the start of this mode.

Mode 9 ($t > t_8$) (Fig. 3(j)): After $t = t_8$, the converter is in an energy-transfer mode as switches S_2 and S_3 conduct current. Power is transferred from the input to the output, and the current in L_{main} decreases. The transformer leakage inductance continues to resonate with the output capacitors of the main switches at the beginning of this mode, but this resonance eventually recedes because of the parasitic resistances in the converter.

III. CONVERTER ANALYSIS

To design the converter, its steady-state characteristics must be determined. In this section, a mathematical analysis of converter modes of operation is performed to derive key

equations and understand the steady-state behavior of the converter relative to the values of certain key components. These relations will be used to develop a design procedure for the proposed converter.

For the steady-state mathematical analysis, the following assumptions are made:

- Input inductor L_{main} is sufficiently large to be considered a constant current source.
- The output capacitor is sufficiently large to be considered a voltage source equal to the output voltage.
- All semiconductors have zero voltage drops while turned on.
- The transformer is ideal and has an infinite magnetizing inductance.

The main objective of the mathematical analysis is to obtain equations for auxiliary circuit capacitor voltage V_{Cr} and auxiliary circuit inductor current i_{Lr} for each mode of operation where the auxiliary circuit is active. Using a computer program to monitor V_{Cr} and i_{Lr} throughout one switching cycle, analytical waveforms related to these parameters are then generated. These waveforms can then be used as part of a design procedure for the converter so that it is possible to turn its switches on and off softly, and to determine the voltages across them and the currents that flow through them so that appropriate devices can be selected. In what follows, the circuit analyses of the proposed converter in different modes of operation are presented and explained:

Mode 0 (Fig. 3(a)): Based on the circuit in Fig. 3(a), the following Kirchhoff's Voltage Law (KVL) equation can be written applied at the transformer primary side:

$$\frac{V_o}{N} = (V_{in} + L\frac{di_{Lm}}{dt}) \tag{1}$$

where i_{Lm} is the current flowing through the input voltage source and N is the secondary to primary turns ratio of the transformer.

Mode 1 (Fig. 3(b)): In this mode, the auxiliary switch is turned on and the current begins to circulate through the auxiliary circuit without any influence on the main converter operation. The initial current of auxiliary circuit inductor L_r is zero, and the initial value of snubber capacitor C_r can be expressed as

$$V_{Cr0} = I_{in}\sqrt{\frac{L_k}{C_{tot}}} + \frac{V_O}{N} \tag{2}$$

where $C_{tot} = C_r + 2C_S$, C_S is the output capacitor of one of main switches, L_{lk} is the transformer leakage inductance, and I_{in} is the boost inductor current. The derivation of this equation is based on Mode 8. Mode 8 is the last mode of the half-switching cycle when the auxiliary circuit is active; thus, the value of V_{Cr} at the end of Mode 8 can be considered to be the initial value of Mode 1, which is the first mode when the auxiliary circuit is active in the converter.

By applying KVL to the auxiliary circuit loop shown in Fig. 3.3, the following differential equation can be derived:

$$-V_{Cr}(t) + L_r\frac{di_{Lr}}{dt} + V_{in} = 0 \tag{3}$$

This equation can be solved to obtain

$$V_{Cr}(t) = \left(I_{in}\sqrt{\frac{L_k}{C_{tot}}} + \frac{V_O}{N} - V_{in}\right)\cos\omega\ (t - t_0) + V_{in} \tag{4}$$

$$i_{Lr}(t) = C_r\omega\ \left(I_{in}\sqrt{\frac{L_k}{C_{tot}}} + \frac{V_O}{N} - V_{in}\right)\sin\omega\ (t - t_0) \tag{5}$$

where $\omega = \frac{1}{\sqrt{L_rC_r}}$, $t_0 < t < t_1$. V_O can be substituted with

$$V_O = \frac{N}{2(1-D)}V_{in} \tag{6}$$

where D is the duty ratio of each main switch and N is the transformer secondary to primary turn ratio.

Snubber capacitor voltage V_{Cr} reaches $\frac{V_O}{N}$ at the end of Mode 1, at time $t = t_1$; thus,

$$V_{Cr}(t_1) = \frac{V_o}{N}\ . \tag{7}$$

Substituting Eqs. (6) and (7) into Eqs. (4) and (5), the equation that expresses the duration of time for Mode 1, $t_1 - t_0$, can be written as

$$t_1 - t_0 = \sqrt{L_rC_r}\cos^{-1}\frac{1}{1+\frac{I_{in}\sqrt{\frac{L_k}{C_{tot}}}}{(\frac{2D-1}{2-2D})V_{in}}}\ . \tag{8}$$

Substituting Eq. (8) into Eq. (5) provides the following equation for $i_{Lr}(t_1)$:

$$i_{Lr}(t_1) = \sqrt{\frac{C_r}{L_r}\times I_{in}\sqrt{\frac{L_k}{C_{tot}}}\times\left(I_{in}\sqrt{\frac{L_k}{C_{tot}}} + \left(\frac{2D-1}{1-D}\right)V_{in}\right)} = \alpha \tag{9}$$

$i_{Lr}(t_1)$ is henceforth referred to as α to simplify the expression of the Mode 2 equations.

Mode 2 (Fig. 3(c)): In this mode, the output capacitors of switches S_2 and S_3 have the same voltage as capacitor C_r, $V_{Cr}(t_1) = \frac{V_o}{N}$. By applying KVL and KCL to the circuit shown in Fig. 3(c), the following equations can be derived:

$$I_{in} + i_C - i_{Lr} - i_{Lk} = 0 \tag{10}$$

$$V_{Cr} - V_{Lr} - V_{in} = 0 \tag{11}$$

$$\frac{V_o}{N} + V_{Lk} - V_{Cr} = 0 \tag{12}$$

where the initial value conditions are

$$i_{Lr}(t_1) = \alpha \tag{13a}$$

$$V_{Cr}(t_1) = \frac{V_O}{N} = \frac{V_{in}}{2(1-D)}\ . \tag{13b}$$

$$i_{Lk}(t_1) = I_{in} \tag{13c}$$

The current in the transformer reaches zero at the end of this mode. Given the complexity of the above modal equations, a closed-form equation for the length of time $(t_2 - t_1)$ is required to be determined by the computer program.

Mode 3 (Fig. 3(d)): At the start of this mode, the transformer primary current is zero and the initial values of the inductor

current and capacitor voltage are I_0 and V_0, respectively. With KVL and KCL, the following equations can be derived:

$$V_{Cr} - V_{Lr} - V_{in} = 0 \quad (14)$$

$$I_{in} + i_C - i_{Lr} = 0. \quad (15)$$

Solving these equations results in the following expressions:

$$V_{Cr}(t) = (V_0 - V_{in})\cos\omega_2(t - t_2) + \left(\frac{I_{in} - I_0}{C_{tot}\,\omega_2}\right)\sin\omega_2(t - t_2) + V_{in} \quad (16)$$

$$i_{Lr}(t) = C_{tot}\,\omega_2(V_0 - V_{in})\sin\omega_2(t - t_2) + (I_0 - I_{in})\cos\omega_2(t - t_2) + I_{in} \quad (17)$$

where $\omega_2 = \frac{1}{\sqrt{L_r C_{tot}}}$ and $t_2 < t < t_3$. Similar to Mode 2, the length of this mode can be calculated by the computer program by determining the time ($t_3 - t_2$) required for V_{Cr} to decrease to zero.

Mode 4 (Fig. 3(e)): During this mode, the voltage across C_{tot}, V_{Cr}, is always zero and that across the auxiliary circuit inductor is constant and equal to $-V_{in}$ because one end of the inductor is connected to the V_{in} input source through S_{aux} and the other end is connected to C_r (thus, 0 V) through D_2. The auxiliary circuit inductor voltage can be expressed as

$$-V_{in} = L_r \frac{di_{Lr}}{dt}. \quad (18)$$

By solving Eq. (18), $i_{Lr}(t)$ can be derived as

$$i_{Lr}(t) = -\frac{V_{in}}{L_r}(t - t_3) + I_{02} \quad (19)$$

with the initial value of $i_{Lr}(t_3) = I_{02}$ and $t_3 < t < t_4$; thus, current linearly decreases in the auxiliary branch. From KCL, the total current flowing through the bridge switches equals $I_{in} - i_{Lr}$; therefore, the current in each main switch, i_S, can be expressed as:

$$i_S = \frac{I_{in} - i_{Lr}}{2}. \quad (20)$$

Given that $I_{in} < i_{Lr}$ in this mode, this current is negative because it flows through the body diodes of the switches.

Mode 5 (Fig. 3(f)): The only difference between this mode and Mode 4 is that current reverses in the bridge switches. The voltage across capacitor C_r remains clamped at zero because all full-bridge switches are on and the DC bus is shorted. Eqs. (18) and (19), which were derived for the previous mode, are also valid for this mode. Eq.(19) can be rewritten as

$$i_{Lr}(t) = -\frac{V_{in}}{L_r}(t - t_4) + I_{03} \quad (21)$$

with the initial value of $i_{Lr}(t_4) = I_{03}$ and $t_4 < t < t_5$. At the end of this mode, the current through L_r, i_{Lr}, reaches zero and the auxiliary circuit is inactive.

Mode 6 (Fig. 3(g)): During this mode of operation, the converter is in a boosting mode because all bridge switches are on. The input current flows through the main switches, and the auxiliary circuit is inactive. The input inductor is magnetized according to following equation:

$$V_{in} = L_{m\,ain}\frac{di_{Lm}}{dt}. \quad (22)$$

The auxiliary switch can be turned off anytime during this mode with zero-current switching. After the switch is turned off, the output capacitance that is parallel to the auxiliary switch cannot be charged because of blocking diode D_2. The voltage across this switch therefore remains zero until the start of the next mode. The duration of this mode is determined by the converter's duty cycle.

Mode 7 (Fig. 3(h)): This mode begins when a pair of diagonally opposed switches, S_1 and S_4, are turned off. In this mode, the full input inductor current flows through capacitor C_r and the output capacitances of switches S_1 and S_4. No power is delivered to the output through the full-bridge switches. As current flows through the auxiliary circuit, an equation is required to define V_{Cr}. No such equation is required for i_{Lr} because S_{aux} is off. Such an equation can be written as

$$C_{tot}\frac{dV_{Cr}}{dt} = I_{in} \quad (23)$$

where $C_{tot} = C_r + 2C_S$, $V_C(t_6) = 0$ and $t_6 < t < t_7$. Rearranging this equation gives

$$V_{Cr}(t) = \frac{I_{in}}{C_{tot}}(t - t_6) \quad (24)$$

where V_{Cr} is the same as the voltage across switches S_1 and S_4. At the end of this mode, V_{Cr} reaches $\frac{V_O}{N}$. This condition makes output bridge diodes D_4 and D_5 forward-biased so that they can conduct current. This condition allows power to be transferred through D_4 and D_5 to the output.

It should be noted that the voltage across diode D_2 is V_{in}-V_{Cr}. After V_{Cr} is charged to the level of the input voltage, diode D_2 becomes forward-biased and the output capacitance of the auxiliary switch voltage begins to charge. Given that the capacitance is small compared with that of C_{tot}, this capacitance is ignored in Eqs. (23) and (24). At the end of this mode, the voltage across S_{aux}, V_{aux}, is equal to

$$V_{aux} = V_{Cr} - V_{in}. \quad (25)$$

Mode 8 (Fig. 3(i)): During this mode, the main inductor current is gradually diverted from snubber capacitor C_r to the transformer. As this transition occurs, the input inductor current continues to charge C_r and V_{Cr} begins to exceed $\frac{V_O}{N}$, which results in voltage overshoots across switches S_1 and S_4. The following equations can be derived with KCL and KVL:

$$i_C + i_{Lk} = I_{in} \quad (26)$$

$$V_{Cr} - V_{Lk} - \frac{V_O}{N} = 0 \quad (27)$$

where $V_{Cr}(t_7) = \frac{V_O}{N}$ and $i_{Lk}(t_7) = 0$. By solving Eqs. (26) and (27), the following expression for $V_{Cr}(t)$ can be derived.

$$V_{Cr}(t) = \frac{I_{in}}{C\omega_3}\sin\omega_3(t - t_7) + \frac{V_O}{N} \quad (28)$$

where $\omega_3 = \frac{1}{\sqrt{L_k C_{tot}}}$ and $C_{tot} = C_r + 2C_S$. . (28) shows that the voltage overshoot of C_r, S_1, and S_4 is

$$\Delta V_{pk} = I_{in} \sqrt{\frac{L_k}{C_{tot}}} \quad (29)$$

such that the initial value of the snubber capacitor voltage of the next mode is the maximum of V_{Cr} in Eq. (28):

$$V_{cr,max} = I_{in} \sqrt{\frac{L_k}{C_{tot}}} + \frac{V_O}{N} \quad (30)$$

Mode 9 (Fig. 3(j)): During this mode, the converter is in an energy-transfer mode because switches S_2 and S_3 conduct current. Power is transferred from the input to the output, and the current in L_{main} declines. The transformer's leakage inductance continues to resonate with the output capacitors of the main switches at the beginning of this mode, but this resonance eventually recedes because of parasitic resistances in the converter. From a mathematical point of view, the voltage across the full-bridge switches eventually settles to $\frac{V_O}{N}$ sometime during this mode.

IV. Design Procedure

A design procedure for the proposed full-bridge boost converter is explained with an example in this section. The following specifications are considered for the design:

Output voltage	V_o = 300 V
Output power	P_o = 500 W
Input voltage	V_{in} = 100 V
Expected efficiency at full load	ή = 93 %
Switching frequency	f_{sw} = 50 kHz

The design procedure presented requires several iterations, both theoretical and experimental, before the final design can be achieved. The general approach taken in the procedure is as follows: First, the converter is designed as a conventional hard-switched converter without the auxiliary circuit. Next, the auxiliary circuit is designed. Finally, the design of the converter is confirmed. Eqs. (4) to (19) can be used to generate graphs of the key steady-state characteristic curves of this converter. The curves can be generated by a computer program, such as MATLAB.

A. Transformer Turns Ratio

The turns ratio of the transformer can be considered the most critical converter parameter, considering that all other parameters are ultimately dependent on it. The turns ratio, N, affects the converter's duty cycle range, which in turn affects the selection of input inductor and output capacitor values. An appropriate value of N can only be determined after several iterations. Once N is determined, the rest of the converter parameters are designed based on this value. Verification or "checking" should be performed afterward to confirm the validity of the design.

If the input inductor current is continuous, then the relation between output voltage V_O and input voltage V_{in} can be expressed by the equation below, which is based on the operation of a conventional single-switch boost converter:

$$V_O = \frac{N}{1-D_c} V_{in} \quad (31)$$

Given that a path for current to flow through in the converter must always be provided, each switch must be on for at least a switch duty-cycle of D = T/2. Converter duty cycle D_c is based on the amount of overlap between the gating signals of S_1 and S_4 and those of S_2 and S_3; thus, the relation between D and D_c can be expressed as

$$DT = D_c \frac{T}{2} + \frac{T}{2} \quad (32)$$

where D_cT represents the amount of time during which an overlap occurs in the two pairs of gating signals (i.e. all the switches are on) throughout a switching cycle. Considering that there are two instances during a switching cycle when all the converter switches are on, the term $D_c \frac{T}{2}$ is used in Eq. (32). If Eq. (32) is substituted into Eq. (31), then the following equation can be derived:

$$V_O = \frac{N}{2(1-D)} V_{in} \quad (33)$$

Eq. (4-2) can be rearranged to give

$$D_c = 2D - 1. \quad (34)$$

For this design example, a value of N = 1, which was determined from the previous iteration is used. The converter is designed based on this value. With this value of N and assuming that the input inductor current is continuous, a value of D = 0.83 is determined based on input voltage V_{in} = 100 V and V_O = 300 V. If D = 0.83, then D_c = 0.66 from Eq. (34). This value of D_c is used in the subsequent sections to determine the input inductor and output capacitor values.

B. Input Inductor

With the values of N and D determined, the design of the rest of the hard-switching converter can proceed, beginning with the input inductor in this section and the output capacitor in the next section. The main consideration for the design of the input inductor in an isolated full-bridge DC–DC boost PWM converter is to limit the peak-to-peak ripple of the current flowing through the inductor. There is, however, a compromise that should be considered in selecting the inductor value. If L_{main} is large, then the peak-to-peak ripple of the current will be small, but the physical size of the inductor will increase significantly, as will the size and weight of the converter. If L_{main} is too small, then the physical size of the inductor will likewise be small, whereas the peak-to-peak ripple of the inductor current will be large. A 10% peak-to-peak ripple to average current ratio is a compromise that is typically made [21]; such compromise is adopted in this example design.

The converter operates with a continuous input current. The average input current (input current without the ripple) can be determined from the converter specifications:

$$I_{in} = \frac{P_O}{V_{in} \times \eta} = \frac{500}{100 \times 093} \approx 5.4 \quad \text{Amps} \tag{35}$$

The auxiliary circuit injects some current back into the input source during Modes 1 to 5 of operation; thus, the value of I_{in} when the converter operates with the auxiliary circuit is different from the value of I_{in} when the converter operates without the auxiliary circuit. Given that the average value of this current is small compared to the input current, it can be considered negligible and is thus not considered in calculating the average inductor current in Eq. (35) for simplicity.

After the average inductor current value is determined, ΔI should be

$$\Delta I = 0.1 \times I_{in} = 0.54 \quad \text{Amps.} \tag{36}$$

A relation between L_{main} and ΔI exists. The voltage across the input inductor when the converter is in a boosting mode and when all switches are on can be expressed as

$$V_{in} = L_{main} \frac{di}{dt} \tag{37}$$

where V_{in} is the voltage across L_{main} when switches $S_{1,4}$ and $S_{2,3}$ are conducing. $dt = D_c \frac{T}{2}$ is the duration of the boosting mode in a half-switching cycle, and $di = \Delta I$ is the change in the input current during that time.

The value of can thus be determined by rearranging Eq. (37) to obtain

$$L_{main} = V_{in} \frac{D_c T}{2\Delta I} = 100 \times \frac{0.66 \times 20\,\mu s}{2 \times 0.54} = 1.22\ m\,H. \tag{38}$$

C. Output Capacitor

The minimum value of the output capacitor can be determined from Eq. (39) as provided in [20]:

$$C_o > \frac{D_c}{R f_o (\frac{\Delta V_o}{V_o})} \tag{39}$$

where R is the output resistance at maximum load ($V_o^2/P_{o,max}$), f_o is the output voltage ripple frequency that is twice the switching frequency, and $\frac{\Delta V_o}{V_o}$ is the percentage of the peak-to-peak output voltage ripple. By assuming a 0.1 % peak-to-peak output voltage ripple, which is considered as acceptable for many converter applications, and by substituting $D_c = 0.66$, $f_o = 100$ kHz, and R = 180 Ω, C_o is determined to be

$$C_o > \frac{D_c}{R f_o (\frac{\Delta V_o}{V_o})} = \frac{0.66}{180 \times 100\,k \times 0.001} = 36.7\ \mu F. \tag{40}$$

D. Snubber Capacitor

The first step in the design of the auxiliary circuit is the selection of a value for the snubber capacitor C_r considering that the design of the other auxiliary circuit parameters is dependent on this value.

The value of C_r should be as small as possible to minimize the amount of energy ultimately transferred to the input after it is discharged. It should also be small to minimize the amount of time that the auxiliary circuit is in the circuit and to minimize the effect that it may have on the general operation of the converter. A large C_r means that much time is required by the auxiliary circuit to discharge it. C_r, however, should be large enough to decrease the rate of the voltage rise across the main switches during Mode 7, to obtain a ZVS turn-off for the main switches, and to prevent voltage spikes from appearing across the switches when they are turned off, as much as possible.

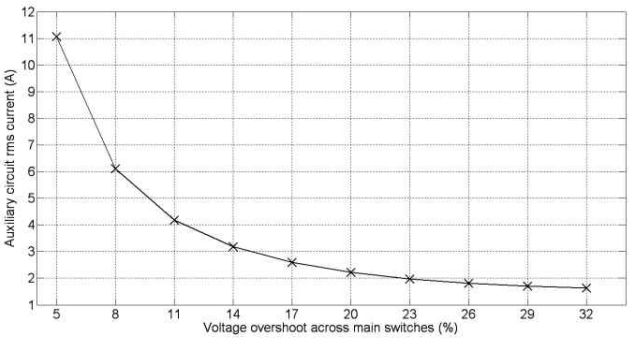


Fig. 5. Voltage overshoots of the main switches versus the auxiliary circuit rms current.

One measure of the amount of energy processed by the auxiliary circuit is the rms value of the current that flows through it during a switching cycle. With this in mind, a graph of auxiliary circuit rms current vs. % voltage overshoot, such as the one shown in Fig. 5, can be generated with a MATLAB program. The graph in Fig. 5 was generated with Eq. (29), which is reproduced here

$$\Delta V_{pk} = I_{in} \sqrt{\frac{L_k}{C_{tot}}} \tag{41}$$

It should be noted that voltage overshoot is dependent on the transformer leakage inductance, as shown in the description of Mode 8 of the converter. The higher the leakage inductance of the transformer is, the more voltage overshoot can appear across the main full-bridge switches. Leakage inductance, however, cannot be eliminated because it is an inherent part of any transformer. The leakage inductance of the transformer used for this design example is L_{lk} = 750 nH.

The graph in Fig. 5 shows that overshoot levels higher than 20% do not have a significant effect on the reduction of the auxiliary circuit rms current. An overshoot of 20% is therefore, is selected for this design example. From Eq. (41)

$$I_{in} \sqrt{\frac{L_k}{C_{tot}}} = 0.2 \times \frac{V_O}{N}. \tag{42}$$

and thus C_{tot} = 6.2 nF, according to $C_{tot} = C_r + 2C_S$ where C_s is the output capacitance of a main switch. If it is assumed, based on previous iterations, that IXFH52N50P2 MOSFET devices, which have an output drain-source capacitance of approximately 600 pF, are used as the main power switches, then the required C_r is 5 nF.

E. Auxiliary Inductor

Given that the auxiliary switch operates with soft switching, the main concern in selecting the auxiliary inductor is to

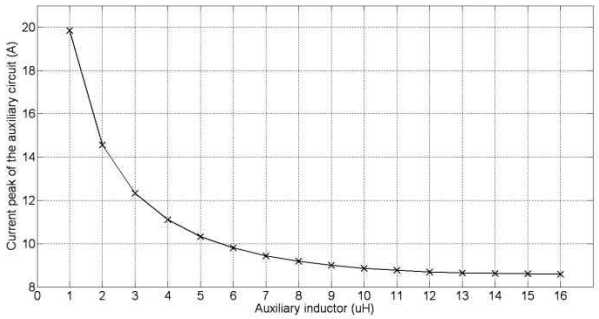


Fig. 6. Current peak of the auxiliary circuit.

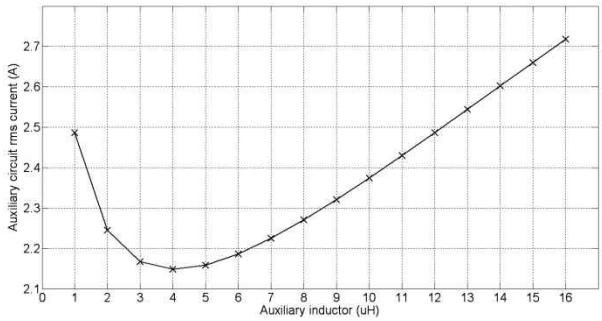


Fig. 7. Rms of the auxiliary circuit current.

minimize the amount of rms current that flows in the auxiliary circuit and the peak current stress on the devices in the auxiliary circuit. An appropriate auxiliary inductor value can be selected using graphs, such as those shown in Figs. 6 and 7. The graph shown in Fig. 6 is a graph of the auxiliary switch peak current vs. the auxiliary circuit inductor value. The graph shown in Fig. 7 is a graph of the auxiliary switch rms current vs. the auxiliary circuit inductor value. These graphs were generated from the modal equations derived in Section III

Figs. 6 and 7 show that there is little change occurs in the peak auxiliary switch current when the auxiliary circuit inductor L_r is greater than 7 μH, but that the rms current increases when L_r is greater than 7 μH. This is because the L_r current becomes flat as L_r increases, but it exists for a longer amount of time as increasing L_r increases the resonant cycle between L_r and C_r. As a result, a value of L_r = 7 μH is selected.

F. Conditions for the soft switching operation of the converter switches

Due to the inductor in series with the auxiliary switch, this switch turns on softly and the current in the switch increases gradually. The auxiliary switch can be turned off with ZCS when no current flows through the switch. No specific time window exists during which the auxiliary switch needs to be turned off with ZCS because of the nature of the auxiliary circuit in the converter and because the current flows through this circuit for only a small fraction of the switching cycle.

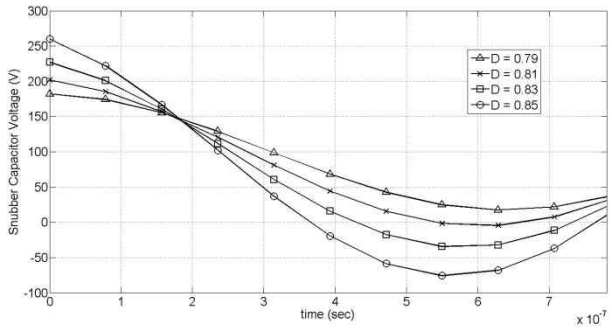


Fig. 8. Variation in snubber capacitor voltage for different values of the main switch duty cycle (D).

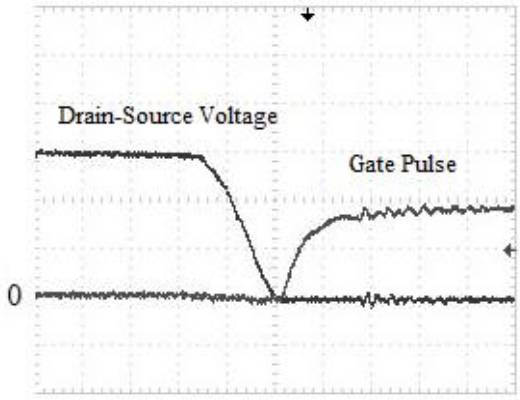
As long as the auxiliary switch is turned off before a pair of main full-bridge switches is about to be turned off, the auxiliary circuit will not interfere with the operation of the main full-bridge switches. The main power switches can be turned off with ZVS as described above because each main power switches has an output drain-source capacitance and because C_r is present in the converter. As for the ZVS turn-on of the main switches, snubber capacitor voltage V_{Cr} should reach zero at the end of Mode 3 of converter operation before a switch is turned on with ZVS; therefore, the following expression can be derived from Eq. (17) from Mode 3:

$$V_{Cr}(t) = \quad (43)$$
$$(V_0 - V_{in})\cos\omega_2(t-t_2) + \left(\frac{I_{in}-I_0}{C_{tot}\,\omega_2}\right)\sin\omega_2(t-t_2) + V_{in} = 0.$$

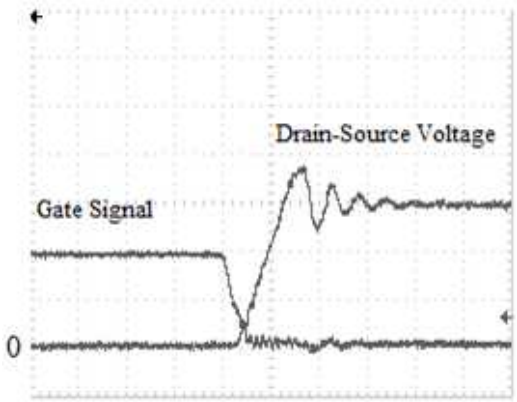
Given that the parameters such as ω_2,C_{tot}, and V_o are interrelated by V_{in} , L_r, C_r, C_s, L_k , I_{in} ,, and D, Eq. (43) can be rewritten as a function of D and can be used to explore the converter's ZVS range with different values of D. A graph of snubber capacitor voltage V_{Cr} vs. time for different values of main switch duty cycle D is shown in Fig. 8, with the time axis starting from time t_2.

The ZVS time window (the amount of time during which a main power switch can be turned on with ZVS) is the interval during which the snubber capacitor voltage is negative, as shown in Fig. 8. A main power switch will not turn on with ZVS unless its main switch duty cycle is at least D = 0.81 as it can be seen in Fig. 8. Given that D is equal to 0.83 as shown in the previous steps, the main full-bridge switches can be turned on with ZVS.

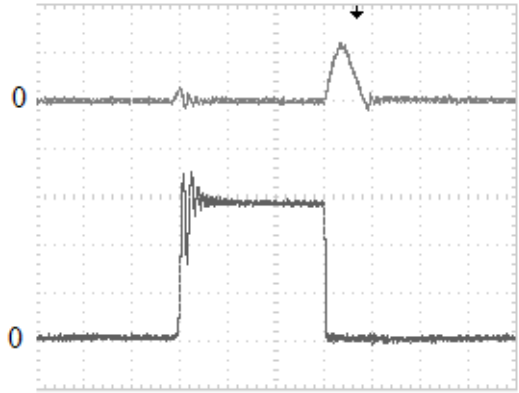
The key condition for ZVS operation is that the DC bus voltage (voltage at the input of the bridge) must be at least twice the input voltage. If the converter is designed to operate with D < 0.5 under steady-state full-load conditions, then the converter will not operate with ZVS. If the converter is designed to operate with D > 0.5 under full-load conditions, then it can operate with ZVS even if D is less than 0.5 under light load conditions because the voltage reflected to the primary side is still greater than twice the input voltage.



(a) ZVS turn-on of a main switch.
(switch voltage: 100 V/div., gate pulse voltage: 5 V/div., t: 250 ns/div.)



(b) ZVS turn-off of a main switch.
(switch voltage: 100 V/div., gate pulse voltage: 5 V/div., t: 500 ns/div.)



(c) Auxiliary switch current (top) and auxiliary switch drain-source voltage (bottom).
(V: 100 V/div., I: 5 A/div., t: 1 μs/div.)

(d) Transformer current (top) and voltage (bottom).
(I: 5 A/div., V: 250 V/div., t: 5 μs/div.)

Fig. 9. Experimental results.

G. *Voltage and current stress of auxiliary switch S_{aux}*

The KVL and KCL equations of the auxiliary circuit in Mode 1 show that the maximum current flowing through the auxiliary switch can be maintained at twice the value of the input inductor current. Moreover, the maximum voltage across this switch occurs at the end of Mode 5, which is around V_o/N.

V. EXPERIMENTAL RESULTS

An experimental prototype of the proposed converter was built to confirm its feasibility. The prototype was designed based on the following specifications:

Input voltage	V_{in} = 100 V
Output voltage	V_o = 300 V
Output power	P_o = 500 W
Switching frequency	f_{sw} = 50 kHz

The prototype was implemented with the component values determined from the design example discussed in Section IV. The main bridge switches, $S_{1\text{-}4}$, were IXFH52N50P2, auxiliary switch S_{aux} was FCA36N60NF. Diode D_1 was BYV29-300, diode D_2 was BYV29-300, and output diodes $D_{3\text{-}6}$ were BYV29-500. Auxiliary inductor L_r was 7 μH, input inductor L_{main} was 750 μH, resonant capacitor C_r was 5 nF, and the transformer turns ratio was 1:1.

The ZVS operation of one of the main full-bridge switches during turn-on and turn-off is shown in Figs. 9(a) and 9(b). Typical auxiliary switch S_{aux} voltage and current waveforms are shown in Fig. 9(c) to demonstrate that this switch can be turned on and off with ZCS. The voltage and current waveforms of the power transformer are shown in Fig. 9(d). All the waveforms were obtained with the converter operating at maximum load.

The efficiency of the converter prototype was measured with the auxiliary circuit (ZVS soft-switching implementation) and without it (hard-switching implementation) to determine the effectiveness of this circuit in improving converter

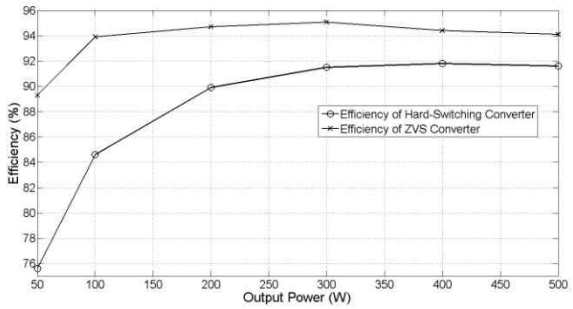


Fig. 10. Efficiency measurement for the proposed ZVS converter and the conventional hard-switching converter.

efficiency. If the auxiliary circuit is removed, then the hard-switching converter may exhibit high voltage spikes across its main switches when they are turned off because the switch output capacitances are not, by themselves, sufficiently large to limit voltage rise and overshoots. As a result, an RCD snubber circuit was placed across the DC bus of the converter. The value of the capacitor (C) of this snubber was similar to that of C_r in the auxiliary circuit of the proposed converter.

Fig. 10 shows the efficiency of the converter prototype with ZVS and with hard-switching. The proposed ZVS converter exhibits considerably higher efficiency than the hard-switching boost converter over the load range. Efficiency is improved because no turn-on or turn-off switching losses occur in the main switches and because the energy used for soft-switching operation is delivered to the input. Normally, turn-on and turn-off switching losses account for most of the losses in a hard-switching converter at high load.

The proposed converter has the following features:

- All four main switches can be turned on and off with ZVS.
- The auxiliary switch can be turned on and off softly.
- The auxiliary circuit is very simple as it consists of a switch, an inductor, and a few diodes.
- The timing of the turning off of the auxiliary switch is very flexible as it can be performed at any time while the DC bus is shorted. This condition is in contrast to other ZVS converters where the auxiliary switch, if it can actually be turned off softly, must be turned off within a narrow window of time.
- The auxiliary circuit does not dump additional current into the full-bridge switches so that their rms current and peak current ratings are similar to those of the switches of the PWM converter shown in Fig. 1.

The converter's ZVS operation is load independent because its switches can be turned on with ZVS from full-load to no-load. The proposed converter is very well suited to industrial applications mentioned in the Introduction of this paper.

VI. CONCLUSIONS

A new ZVS-PWM full-bridge converter that is specifically targeted towards for applications that require a high step-up voltage ratio is proposed in this paper. The proposed converter does not have any of the disadvantages associated with other converters of this type, including a complicated auxiliary circuit, increased current stresses in the main power switches, and load dependent ZVS operation. In this paper, the operation of the new converter, its steady-state characteristics, and its design were explained and examined. The feasibility of the converter was confirmed with the results obtained from an experimental prototype.

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