*IEIE Transactions on Smart Processing and Computing, vol. 3, no. 6, December 2014*
http://dx.doi.org/10.5573/IEIESPC.2014.3.6.416



# A Low-Voltage Low-Power Opamp-Less 8-bit 1-MS/s Pipelined ADC in 90-nm CMOS Technology

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*Received February 20, 2014; Revised April 20, 2014; Accepted August 28, 2014; Published December 31, 2014*

** Regular Paper*

***Abstract*:** This paper presents an 8-bit pipelined analog-to-digital converter. The supply voltage applied for comparators and other sub-blocks of the ADC were 0.7V and 0.5V, respectively. This low power ADC utilizes the capacitive charge pump technique combined with a source-follower and calibration to resolve the need for the opamp. The differential charge pump technique does not require any common mode feedback circuit. The entire structure of the ADC is based on fully dynamic circuits that enable the design of a very low power ADC. The ADC was designed to operate at 1MS/s in 90nm CMOS process, where simulated results using ADS2011 show the peak SNDR and SFDR of the ADC to be 47.8 dB (7.64 ENOB) and 59 dB respectively. The ADC consumes less than 1mW for all active dynamic and digital circuitries.

***Keywords*:** Pipeline ADC, Charge-pump, Opamp-less, Low-power, Dynamic comparator, Low voltage

## 1. Introduction

The new advances in wireless and mobile applications and the cost sensitivity of the IC design and fabrication have been the driving forces in the development of low-power circuits [1]. ADCs have seen a burst of development in recent years with the introduction of new design techniques. For systems requiring a moderate to high resolution with a sampling rate at the Nyquist rate, the pipeline ADC is a suggestive alternative [2]. With the continuous down scaling of the CMOS process toward the sub-micron region to achieve low-cost, low-area, low-power, and high-speed digital systems, ADC design in sub-micron technologies has become a necessity. As the feature size in advanced CMOS technology shrinks to the nanometer scales, it improves the speed and power consumption of digital circuits. On the other hand, it also leads to a decrease in the supply voltage as the technology scales. This decreases the voltage headroom and causes significant challenges in the design of analog circuits [3].

The challenges in sub-micron devices has caused a flurry of research into the removal of the OTA and substituting it with another less challenge alternative. Studies in reducing the power consumption of OTA-based pipelined ADCs are another reason for the development of techniques, such as opamp sharing [4], powering off the opamp when it is idle for half a clock cycle [5, 6], double sampling [7], and developing more power efficient opamp topologies [8].

Using an open-loop residue amplification technique [9] instead of capacitive feedback opamp-based circuits enable the designer to achieve a low power ADC because open-loop gain stages do not require a large DC-gain, thereby simplifying the MDAC circuit. Employing comparators and integrators instead of opamp is another recently introduced innovation [10] that can perform the same response of the opamp but with far less power dissipation.

This paper presents a low-power pipelined ADC with very low power consumption due to the new technique introduced in [11]. The innovation in [11], is based on a simple conventional charge pump that can produce the required stage gain; thus eliminating the need for a power-hungry opamp-based approach. In addition to having a power saving benefit, charge pump based circuits can resolve the need for common mode feedback in fully differential circuits and achieve high degree of linearity.

This paper also addresses two important aspects of pipelined ADC design. The first is regarding a pipelined ADC with ultra-low supply voltage. As CMOS technology advances, lower supply voltages are expected in the near

future. This study explored its design feasibility and implications. The second aspect is related to minimizing the total power consumption of the pipelined ADC [3]. A 0.5V 8bit pipelined ADC operating at 1MS/s is proposed.

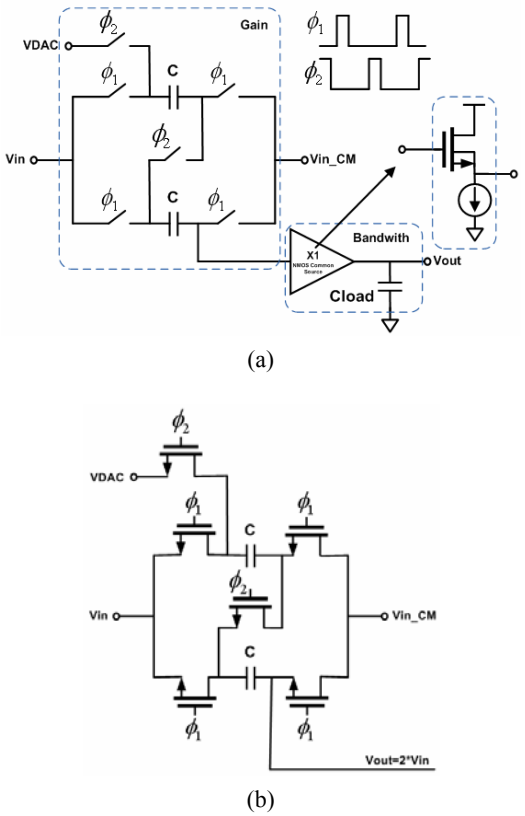
The organization of this paper is as follows. Section 2 describes the differential capacitive charge pump technique used to design the gain stages and the sample, and hold circuit. Section 3 details the performance of the low-power high-speed dynamic comparator. Section 4 presents the circuit simulation of the whole ADC using ADS2011 in a 90nm CMOS process. Section 5 summarizes and concludes the work.

## 2. Capacitive charge pump circuit

The main motivation of the technique presented was to reduce significantly the power consumption in the pipelined ADC. In this technique [11], instead of producing the required gain from the conventional capacitive feedback and OTA, a passive charge pump sharing technique is utilized. As 1.5 bit sub-ADCs are designed for the stages, the required gain for each stage is equal to 2. The basic of this technique simply originates from a combination of two capacitors along with some switches. As shown in Fig. 1, in phase $\Phi_1$, the capacitors are charged to $V_{in}$ and in phase $\Phi_2$ the charged voltages on the two capacitors are added up and the $2V_{in}$ is delivered to the output.

By performing the voltage doubling that was introduced, a fully differential capacitive charge pump multiplying DAC (MDAC) with some modification can be designed without any need for an op-amp or other active circuits. A differential capacitive charge pump based MDAC developed in a 1.5-bit pipeline stage to avoid amplifying the common-mode offset voltages and the proposed MDAC topology can achieve the same speed as the traditional MDAC with half the power consumption, due to the larger β (feedback factor) value in the proposed MDAC. An additional advantage, as the buffer comes after the passive gain block, the power of the buffer's noise when referred to the input of the pipeline stage is divided by the amount of passive gain squared – unlike the traditional MDAC, where the noise of the opamp is not divided by the stage gain when referred to the input. Therefore, the noise from the active circuitry in the proposed topology contributes less to the overall noise floor than that in the traditional MDAC; hence enabling a further decrease in ADC power.

The sampling network was arranged such that the differential input was sampled in a fully bridged configuration across the sampling capacitors during $\Phi_1$. Because the input common-mode voltage is sampled on both sides of the series combination of the sampling capacitors, common-mode variations in the differential input are rejected during $\Phi_2$. Switches $S_1$ and $S_2$ are included in Fig. 2 to isolate nodes $X_1$, $X_2$, $X_3$, and $X_4$ during $\Phi_1$; thus ensuring that switches $S_3$, $S_4$, $S_5$, and $S_6$ act as bottom-plate sampling switches to achieve high linearity by minimizing charge-injection effects. The advantages of




(a)

(b)

**Fig. 1. Basic voltage doubler (a) Gain of approximately 2 using a capacitive charge pump approach, (b) the transistors level.**

proposed MDAC are low power consumption, good linearity, low noise, and no need for an explicit common-mode feedback circuit. Figs. 2 and 3 present the circuit of the designed MDAC and the simulation result of the MDAC, respectively. The MDAC circuit has a gain equal to 2 regarding the input signals.

In most highly accurate ADCs, a bootstrapped analog switch is used for sampling. This provides a constant $R_{ON}$ by maintaining the VGS of the sampling switches independent of the input signals [12]. Bootstrapped switches (Fig. 4) are utilized in the input lines to improve the linearity of the circuit because the variation of the $R_{ON}$ of the simple NMOS switches has an effect on the SFDR of the whole ADC. To reduce this effect, bootstrapped switches are used, at least for input switches. In this type of switch, the voltage of VGS remains unchanged as the input signal varies, thus the $R_{ON}$ remains approximately fixed, giving rise in the linearity of the circuit. To ensure the performance of the switch, spectral analysis with a sampling frequency equal to 100 MS/s and 512-point FTT is performed. The result of this test is also shown, which shows that the third harmonic is 80dB below the fundamental tone.

The sample and hold circuit can be designed by B modifying the same approach utilized for the MDAC. Fig. 5 shows a schematic of the simple charge pump based S&H and its simulation result. Similar to the MDAC circuit, the bootstrapped switch was utilized for the input switches of the S&H to improve the linearity of the circuit.

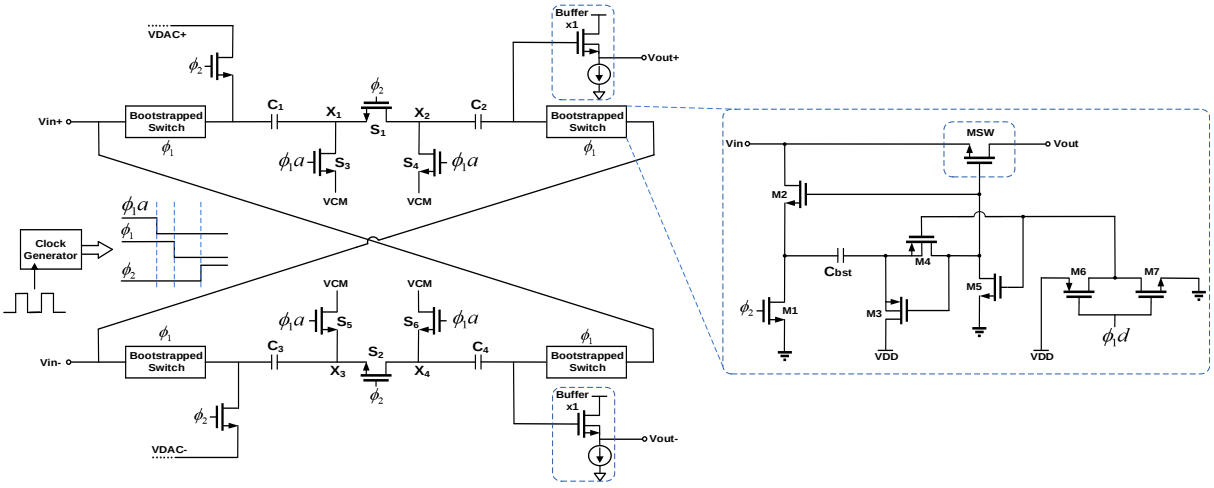



**Fig. 2. The schematic of the fully differential capacitive charge pump based MDAC.**

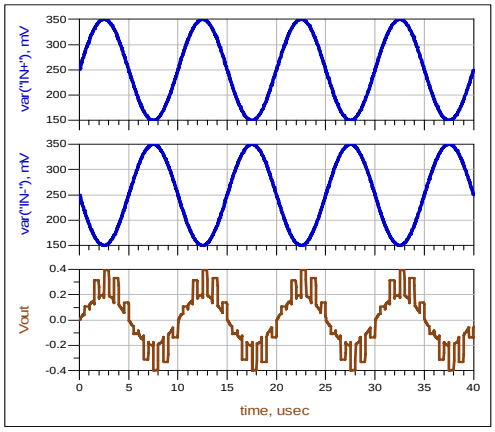



**Fig. 3. Simulation of the MDAC with gain=2.**

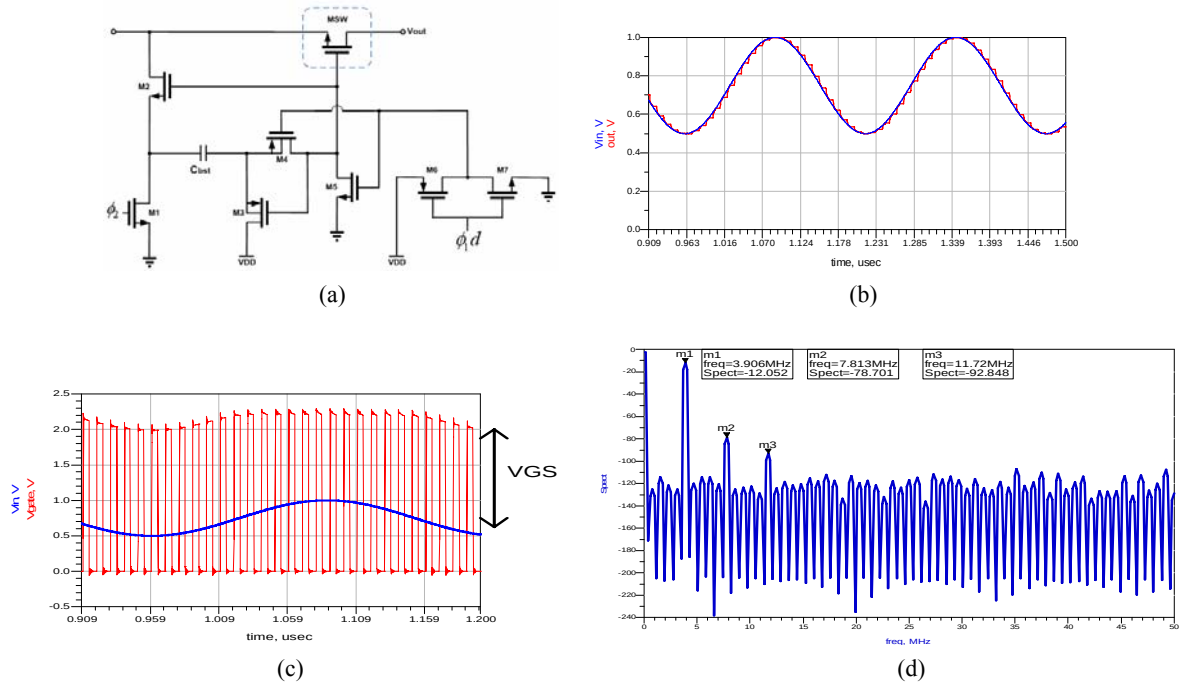
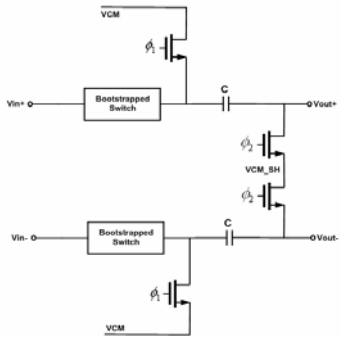
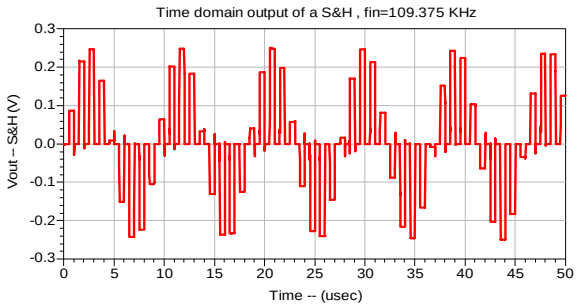



**Fig. 4. Simulation result of the bootstrapped switch and the FFT test (a) Bootstrapped switch, (b) the sampled output of the switch, (c) signals of the input and the gate of the switch, showing the constant $R_{ON}$ by maintaining the VGS over the input signal, (d) 512-point FFT simulation of the switch with 100MHz sampling frequency.**




(a)




(b)

**Fig. 5. S&H (a) schematic of the S&H circuit, (b) its simulation result.**

## 3. Dynamic comparator design

In some previously introduced comparators [13] the clock boosting technique was used to supply a higher voltage to the input transistors. In this comparator [14], to avoid any reliability concerns due to voltage boosting, transistor M5 was applied instead of a clock booster. The back to back positive feedback inverters realize the latch part of the comparator. In the reset phase, this latch was shorted to the ground and M5 was switched off to stop the current flowing into the inverters. As the clock edge increases, the latch phase starts, the positive feedback is realized, the small voltage difference the was saved during the last phase is amplified, and the logic is produced. When the input transistors are ideally matched, the differential input voltage (VIN) is zero. When VIN is negative due to of the difference between the resistances of the transistors, the positive feedback behaves in a way that the VOP reaches zero while the VON is equal to one. A reverse phenomenon is observed when VIN is positive. In a 1.5 bit pipeline, stage two nonzero threshold voltages ($+V_{REF/4}$ , $-V_{REF/4}$) are required. To realize this, two transistors parallel to the input transistors are applied. Ideally, if the sizes of these transistors are set to the one fourth of the width of the input transistors then the desired nonzero threshold voltages are obtained. The supply voltage used for the comparator and other parts of the ADC are 0.7V and 0.5V, respectively. Therefore, to relate the different blocks to each other, a level shifter circuit was applied, as implemented in Fig. 6.

The reference voltage, $V_{RP}$ and $V_{RN}$, are equal to the equations below:

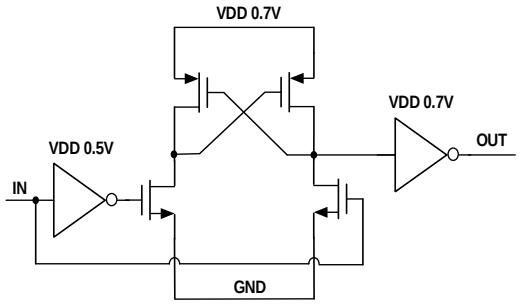
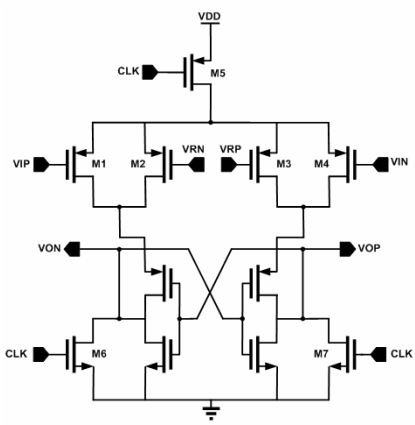
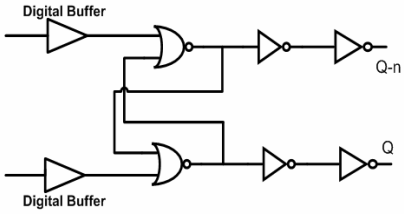



**Fig. 6. Level shifter circuit.**




(a)

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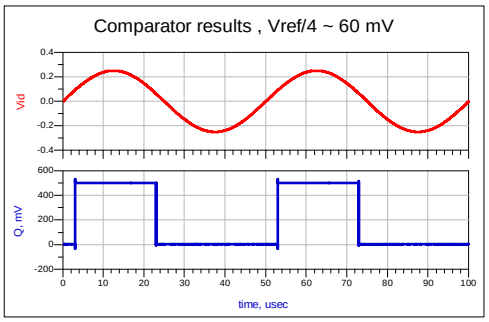



(c)

**Fig. 7. Schematic of the (a) low-power dynamic comparator, (b) its output digital logic, (c) its simulation result.**

$$V_{RP} = \left(V_{CM} + V_{FS}/4\right) \quad (1)$$

$$V_{RN} = \left(V_{CM} - V_{FS}/4\right) \quad (2)$$

where $V_{CM}$ is 0.25 V and full scale input signal is $V_{FS}$ = 0.5V. Therefore, $V_{RP}$ = 0.375 V and $V_{RN}$ = 0.125 V and

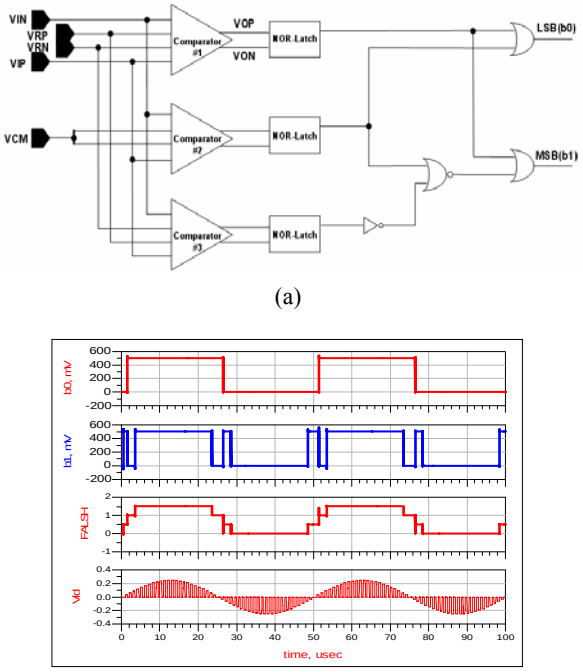



**Fig. 8. 2-bit Flash ADC (a) schematic of the 2-bit Flash ADC, (b) its simulation result.**

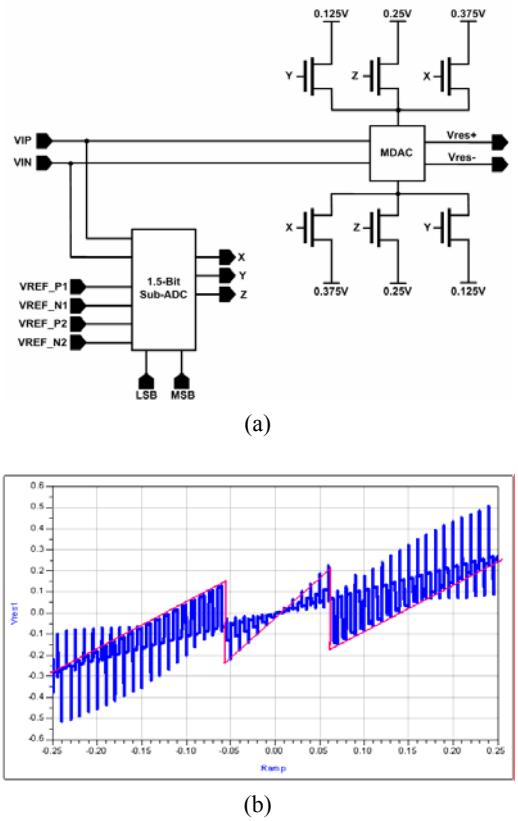



**Fig. 9. 1.5-bit stage (a) schematic of the stages of the ADC, (b) its residue vs. input signal with a nonzero threshold voltage = 50 Mv.**

nonzero threshold voltage will be 50 mV. Fig. 7 presents a schematic of the low-power dynamic comparator, its output digital logic and its simulation results.

This comparator can also be used to design the last stage of this pipelined ADC. The last stage is a 2-bit Flash ADC, the schematic of the 2-bit Flash ADC and its simulation result is shown in Fig. 8. The structure of the whole circuit of the first stage along with its transfer cure characteristic result is shown in Fig. 9. For the simplicity of the design, all the 1.5-bit stages are designed to be the same. The DAC part of these stages are realized using NMOS switches, which are controlled with signals X,Y and Z generated from the two comparators in the 1.5-bit sub-ADCs.

## 4. ADC topology and Performance Evaluation

This 8-bit ADC is composed of six 1.5-bit stages (including Sample-and-Hold, Passive MDAC and 1.5-bit flash stage ADC), one 2-bit flash ADC at its end side and a S&H circuit. Each six 1.5-bit stages generate the digital codes in different phases (Φ1 and Φ2) using a non-overlapping clock generator circuit. The output bits from each stage are delayed according to the number of stages and the bits are added using a full adder. At the end, the digital data are weighted and added up to generate the digitized sinusoidal output signal. The delay line is composed of DFFs (D Flip-Flop) and the full adders are based on XOR-based half adders. The data from the first stage are delayed equal to $7*T_S/2$ and the data from the last stage are delayed only $1*T_S/2$; thus all the bits are synchronous and adding them will have no problem. Fig. 10 shows the top level topology of the ADC designed using the power reduction techniques discussed in this paper. Low power was achieved using a simple architecture consisting of a charge pump combined with a source-follower and digital calibration, which replaced the functionality of power-hungry opamp based pipeline stages found in prior works. A differential sampling technique was used, which eliminated the need for an explicit CMFB circuit; thus enabling further power savings.

Fig. 11 also presents the simulation result for the 10 kHz full-scale input signal. The output signal ranged from 0 to 255 showing the 8-bit performance of the ADC. Moreover, the ramp test was performed on the ADC. In this test, the differential ramp signal from -0.25 V to +0.25 V with a slope of (1.LSB/nTs ), where n=5, was applied to the input and the result is shown in Fig. 12. This shows the good performance of the ADC with less error before the calibration techniques. Performing a calibration on this result will provide a transfer curve with minimal error and also better linearity with the INL and DNL values given in the comparison table.

The values of INL and DNL may be to some extent larger than typical values. However, applying linearization or calibration techniques will bring these values to the desired range. In Fig. 13 the simulation results of the INL and DNL before calibration are illustrated. In Fig. 14, the results after calibration using the MATLAB code were implemented. Calibration improves the INL and DNL of

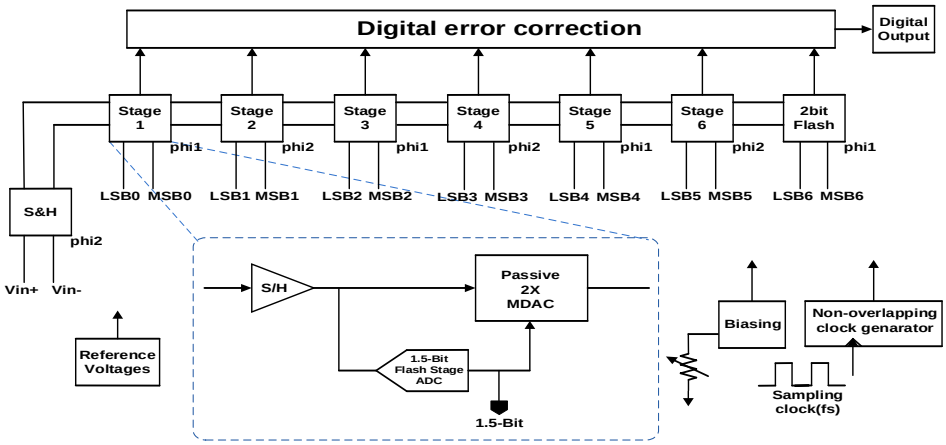



**Fig. 10. Complete structure of the ADC.**

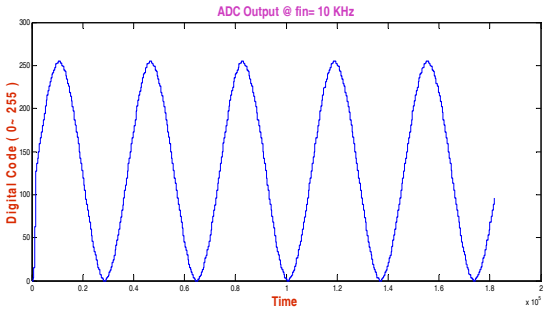



**Fig. 11. Simulation result of the ADC for Fin=10 kHz.**

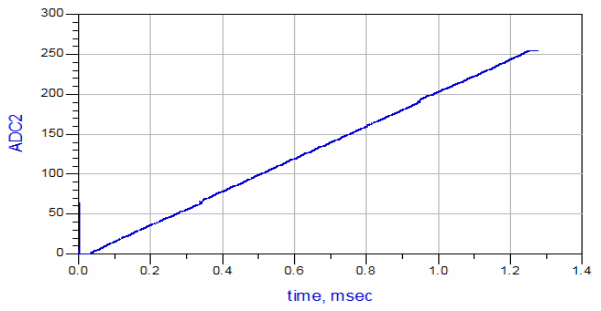



**Fig. 12. Simulation result of the ADC under the ramp test.**

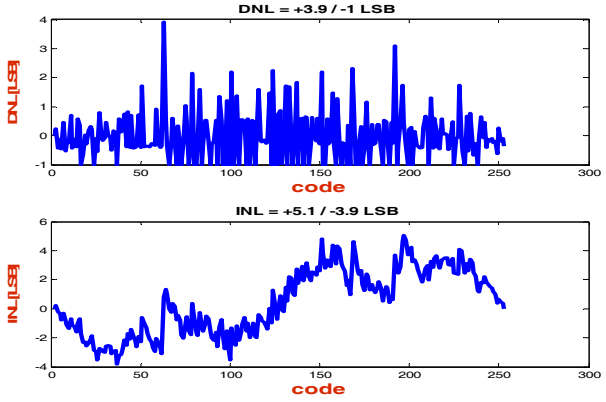



**Fig. 13. DNL and INL of the ADC without calibration (before calibration).**

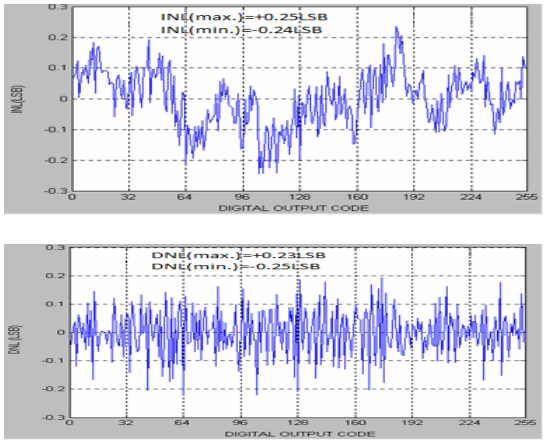


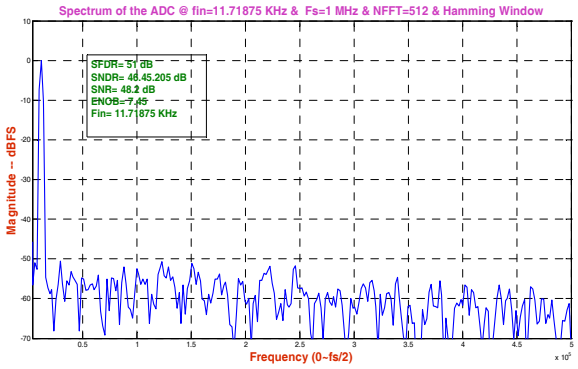

**Fig. 14. INL and DNL of the ADC after calibration.**

the ADC significantly. The digital outputs of each pipeline stage imported into MATLAB, and by some code, better ADC INL and DNL results can be obtained.

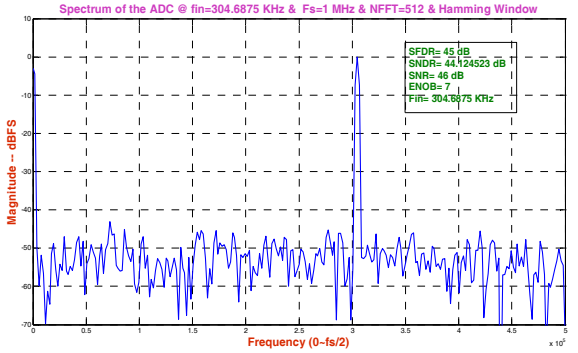
The 512-points FFT test on the ADC with two different input frequencies shows the proper performance of the ADC. Fig. 15 shows the spectrum of the ADC before calibration. The band width of this ADC is 500 kHz, the sampling rate is 1 MHz and the two input signal frequencies are 304.68 kHz and 11.71 kHz.

Fig. 16 presents the spectrum of the ADC output signal with a 107.2575 KHz input tone frequency after calibration for fs = 1MS/s. The FFTs clearly show better ADC performance by the calibration. Using the calibration technique, significant improvement in ADC performance can be observed. After calibration, the INL of the ADC improves significantly from +5.1/-3.9 LSB to +0.25/-0.24 LSB and DNL from +3.9/-1 LSB to +0.23/-0.25 LSB, and the 1024-points FFT plots considering the device noise in this work with an improvement in ADC popular specifications, such as SFDR=59dB, SNDR=47.8dB, SNR=49.1dB and ENOB=7.64-bit, as shown in Fig. 16.

Fig. 17 shows the simulated values of ADC SFDR, SNDR, SNR and ENOB versus the input frequency before/after calibration. After calibration, the ADC dynamic performance was better than that before calibration.




(a)




(b)

**Fig. 15. Simulated output spectrum at two different frequencies before calibration with full-scale sine wave input signal (a) Fin =11.71875 KHz, (b) Fin =304.6875 KHz.**

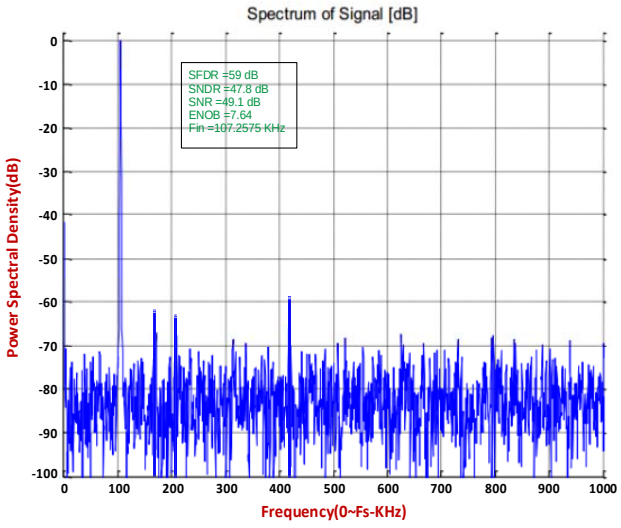



**Fig. 16. 1024-points FFT of ADC output signal after calibration with 107.2575 KHz input tone, $f_s$ =1MS/s.**

Table 1 summarizes the key experimental results of this ADC and compares it with some new works. To compare the proposed ADC with other state-of-the-art pipelined ADCs, the well-known figure-of-merit (FOM) equation was used.

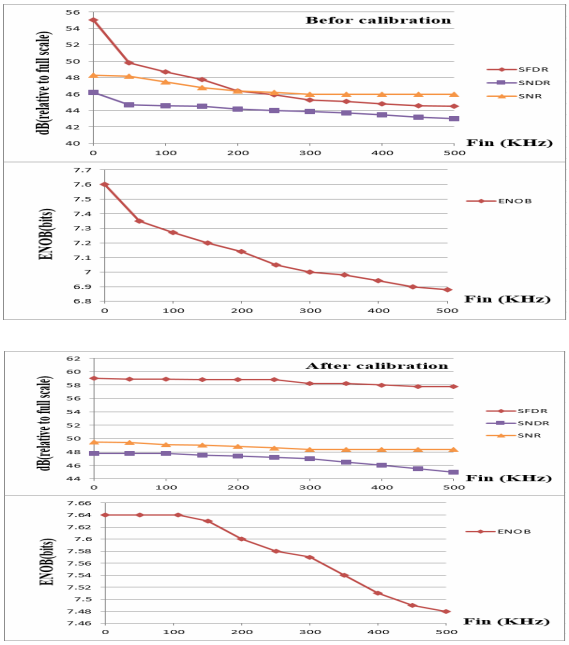



**Fig. 17. Simulated SNDR, SNR, SFDR and ENOB before/after calibration for full-scale input versus the input frequencies.**

**Table 1. ADC performance summary and comparison.**

| Reference | [15] | [3] | [11] | This Work |
|---|---|---|---|---|
| Technology | 90 nm | 90 nm | 180 nm | **90 nm** |
| Sample Rate (MHz) | 100 | 10 | 50 | **1** |
| Full Scale Input Signal Range (V) | N/A | 0.4 | 1 | **0.5** |
| VDD (V) | 0.9 | 0.5 | 1.8 | **0.5** |
| $SNDR_{peak}$(dB) | 59 | 48.1 | 58.2 | **46*/47.8**** |
| $SNR_{peak}$(dB) | N/A | 49.3 | N/A | **48*/49.5**** |
| $SFDR_{peak}$(dB) | 67 | 57.2 | 66 | **51*/59**** |
| DNL min/max(LSB) | N/A | -0.48/+0.55 | -0.35/+0.35 | **-1/+3.5*** / **-0.25/+0.23**** |
| INL min/max(LSB) | N/A | -1.19/+1.12 | -0.8/+0.7 | **-3.9/+5.1*** / **-0.24/+0.25**** |
| Power | 15.5mW | 2.4mW | 10mW | **840µW** |
| ENOB(bits) | N/A | N/A | 9.4 | **7.64** |
| FOM(pJ/Conv-step) | 0.21 | 1.15 | 0.3 | **4.2** |
| *Before Calibration, **After Calibration | | | | |

$$FOM = \frac{Power}{2^{ENOB} \times \min\{f_s, 2 \times ERBW\}}$$

where the fs is the sampling rate, and the ENOB is the effective number of bits at the effective resolution bandwidth (ERBW). The FOM of the proposed ADC is 4.2 pJ/conversion-step at 1MS/s and a 0.5V supply.

## 5. Conclusion

In this paper a low voltage low power 1MS/s 8-Bit pipelined ADC in a 90nm CMOS technology was designed and simulated in ADS2011. The device mismatch was considered in this simulation to obtain nonlinear performance. The ADC was based on the capacitive charge pumps and calibration techniques, which gives the possibility of removing power-hungry opamps from the entire structure. Utilizing this technique, a low-power low-area ADC was achieved. The simulated results, showed the peak SNDR of 47.8 dB (7.64 ENOB), and 59 dB SFDR. This ADC achieves 4.2pJ/conv-step figure-of-merit and consumes less than 1 mW for all active dynamic and digital circuitries.

## Acknowledgement

This study was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2013R1A1A2010114).

This work was supported by IDEC (IPC, EDA Tool, MPW).

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