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A High Efficiency Active Rectifier for 6.78MHz Wireless Power Transfer Receiver with Bootstrapping Technique and All Digital Delay-Locked Loop

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** Short Paper*

***Abstract*:** This paper presents a new rectifier with a bootstrapping technique to reduce the effective drop voltage. An all-digital delay locked loop (ADDLL) circuit was also applied to prevent the reverse leakage current. The proposed rectifier uses NMOS diode connected instead of PMOS to reduce the design size and improve the frequency respond. All the sub-circuits of ADDLL were designed with low power consumption to reduce the total power of the rectifier. The rectifier was implemented in CMOS 0.35 μm technology. The peak power conversion efficiency was 76 % at an input frequency of 6.78MHz and a power level of 5W.

***Keywords*:** Rectifier, High efficiency, Bootstrapping, ADDLL

1. Introduction

Recently, wireless power transfer (WPT) technology has become a very popular research topic, particularly in applications related to portable device chargers and biomedical devices. Since the WPT idea was proposed, many researchers have tested the probability of applying this concept to commercial applications. The WPT has been prevented from widespread used for a number of reasons, but the major issues is the power transfer efficiency.

Therefore, the target of all research in the field of WPT is to improve the efficiency of the WPT system so that less transmitting power is required and/or a longer distance between the external transmitting device and the implant device can be facilitated while using the same transmitting power from the external device. Fig. 1 gives an example of the WPT system. To achieve this target, besides improving the performance of coil transfer, the rectifier also plays a very important role in the total efficiency of the WPT system.

Within the scope of this research, this paper proposes a high power efficient rectifier using a connected diode operating at 6.78MHz. The power conversion efficient (PCE) was improved by combining bootstrapping technique [1] to increase the voltage conversion ratio and all digital DLL circuits to reduce the leakage current. As a result, the total power conversion efficiency is increased.

All the designs used to control the rectifier were designed with low power consumption to reduce the total power of the rectifier and increase the conversion efficiency. The NMOS diode connected is used instead of a PMOS to reduce the size and power consumption. NMOS diode connected also improves the frequency response and increases the reliability of the proposed rectifier design.

The remainder of this paper is structured as follows: Section 2 discusses the design issues of the rectifier; Section 3 presents the bootstrapping technique and all-digital delay locked loop; full proposed rectifier is also presented in this session. Section 4 presents the simulation results of the new structure. Finally, in Section V reports

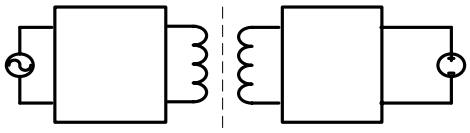


Fig. 1. Wireless power transfer block diagram.

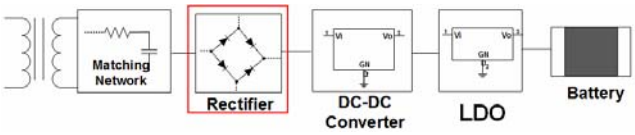


Fig. 2. Wireless power transfer receiver block diagram.

the conclusions.

2. Design issue of rectifier

2.1 Overall Wireless Power Transfer Receiver Architecture

Fig. 2 shows the diagram of the overall wireless power transfer system at the receiver side. The start of the receiver is a secondary antenna that receives power from the primary antenna of the transport part of WPT system. The voltage at this antenna is the AC signal. In the RF system, the network matching component always appears so as to match the impedance of parts in the system. In the scope of this paper, the matching network is not considered. The power received at the secondary antenna will be passed through the matching network and input to the rectifier. The rectifier converts this AC voltage to a DC voltage. The low-dropout (LDO) circuit controls the DC voltage and reduces the ripple variation, and supplies the expected voltage to battery.

To increase the power transfer efficiency, the power loss needs to be reduced and the conversional efficiency in each block of the system needs to be improved. The related work in reference [4] specifies that the antenna transfer efficiency and rectifier conversion efficiency are the most important components in the contribution to the total power transfer efficiency of the WPT system. As shown in Fig. 2, this work will specifically discuss the rectifier, and based on that discussion, an active rectifier is proposed.

2.1 Rectifier design issues

Conventional AC to DC conversion is achieved by diodes and capacitors. This may be as simple as a half-wave rectifier or full-wave rectifier. These rectifiers are normally used in high voltage applications, where the forward voltage drops of 0.7V~1V are relatively low. In low-voltage integrated circuits applications, this voltage drop reduces the power efficiency significantly. The power efficiency of rectifier is calculated as follows:

$$\eta_{rectifier} = \frac{V_{out}}{|V_{in}|} \times \frac{I_{out}}{I_{in}} \approx \frac{V_{out}}{V_{out} + V_{do}} \times \frac{I_{out}}{I_{out} + I_{loss}} \qquad (1)$$

where V_{do} and I_{loss} are the drop voltage and loss current, respectively. As shown in formula (1), the drop voltage in the diode or the loss current of the switching state are the reason for the significant degradation of the power efficiency. Schottky diodes can be used to enhance the power efficiency because of the low forward drop voltage. However, the fabrication cost is high compared to the CMOS process. Another way to reduce the drop voltage is to use an advanced CMOS process, which incurs extra cost for additional masks and fabrication steps. In addition, the turn-on threshold voltage of a standard CMOSS process can be cancelled by adding some additional biasing circuits. In these cases, the gate-drain voltages are fixed and the gate-drive voltages are controlled by their drain-source voltage that change only slightly from the forward to reverse conduction. Therefore, the switches cannot be turned on and off completely, which leads to inefficient rectification.

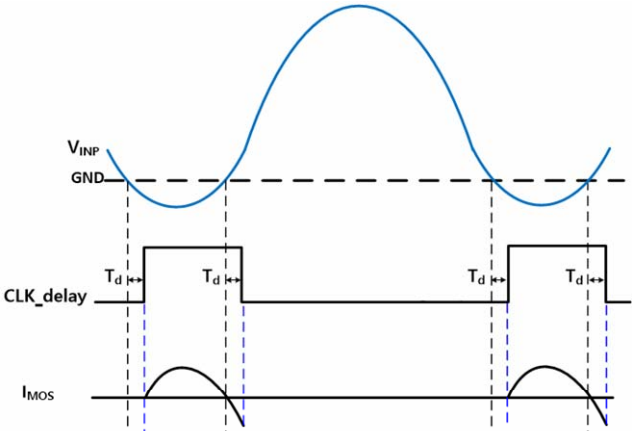


Fig. 3. Reverse current in the rectifier.

The current flow in the MOS transistor is bidirectional, which means that it can flow from the DC output to the AC input side. The reverse current will degrade the power efficiency significantly as in formula (1). The reverse current is due mainly to the delay of the comparator and buffer driving the gate of transistors, as shown in Fig. 3. Therefore, to prevent this leakage current, the delay time should be either cancelled or compensated. To achieve higher power conversion efficiency, the switches need to be turned on and off immediately before the reverse current is set in. In other words, a zero delay from the AC input to gate voltage of MOS transistors is needed. When input signal and output of gate driving are synchronized, the reverse current is also cancelled and the power conversion efficiency is increased.

3 Active Rectifier Architecture

3.1 Implementation

3.1.1 Bootstrapping technique

Various techniques have been used to reduce the influence of the threshold voltage. They often benefit from the use of either bootstrap capacitors or dynamic techniques for gate-drain or bulk-source (body effect) biasing [3]. Among these techniques, the bootstrapping technique is the most effective in a CMOS integrated circuit.

Fig. 4 presents the bootstrapping technique using bootstrap capacitor, C_B.

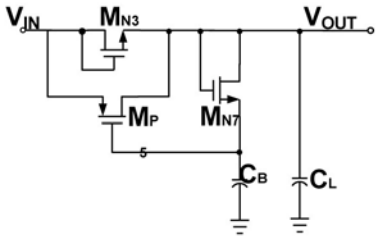


Fig. 4. Bootstrapping Technique.

When the input voltage V_{IN} is larger than the output voltage V_{OUT} and the difference amount is at least V_{th}, the current will move from the input to the output and charge the output capacitor C_L. As C_L is charged up, C_B also charges up through the diode-connected M_{N7} and V_{CB} is Vth7, 8 below the VDC. Therefore, the output voltage is as follows:

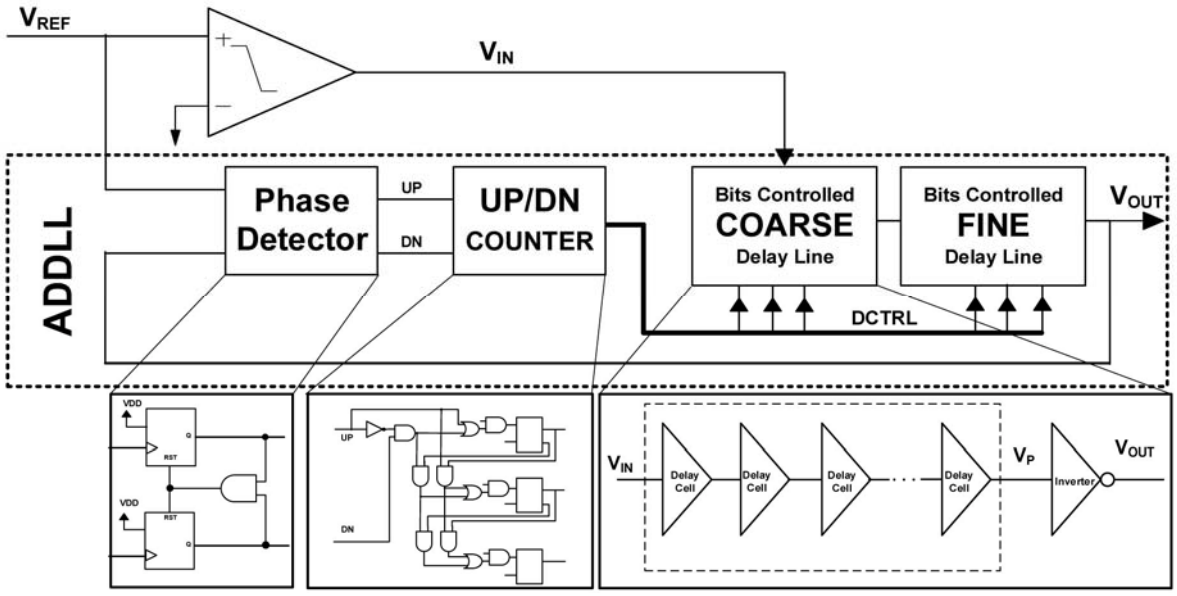
$$V_{OUT} = V_{IN} - (|V_{th3}| - |V_{th7}|) \quad (2)$$

From (2), the effective threshold voltage is very small compared to that in a conventional rectifier. The voltage drop across the PMOS in the power transfer path is then reduced significantly.

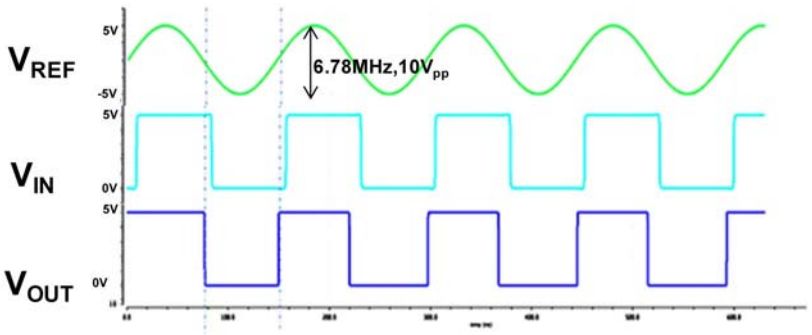
3.1.2 All Digital Delay-Locked Loop

As discussed above, a delay-locked loop is needed to compensate for the delay time of the comparator and then cancel the reverse current from the output side to the rectifier. At low operating frequencies in WPT applications, in this case 6.78MHz, an all-digital delay-locked loop is preferred because of its advantages compared to an analog DLL. ADDLL has low power consumption, smaller area and less complexity. Therefore, it is the most appropriate choice for the rectifier requirements.

Fig. 5 presents the structure and timing diagram of ADDLL using in proposed rectifier. To make this circuit more accurate, two delay lines, the coarse delay and fine delay, are used. The input voltage is compared with the V_{OUT} via the PD circuit. The output of the PD is the phase differences and is expressed as the pulses UP and DN, which will be transferred to the control bits. These control bits determine the delay time of the delay cell and delay line.



(a)



(b)

Fig. 5. (a) Block diagram, (b) Timing diagram of proposed ADDLL.

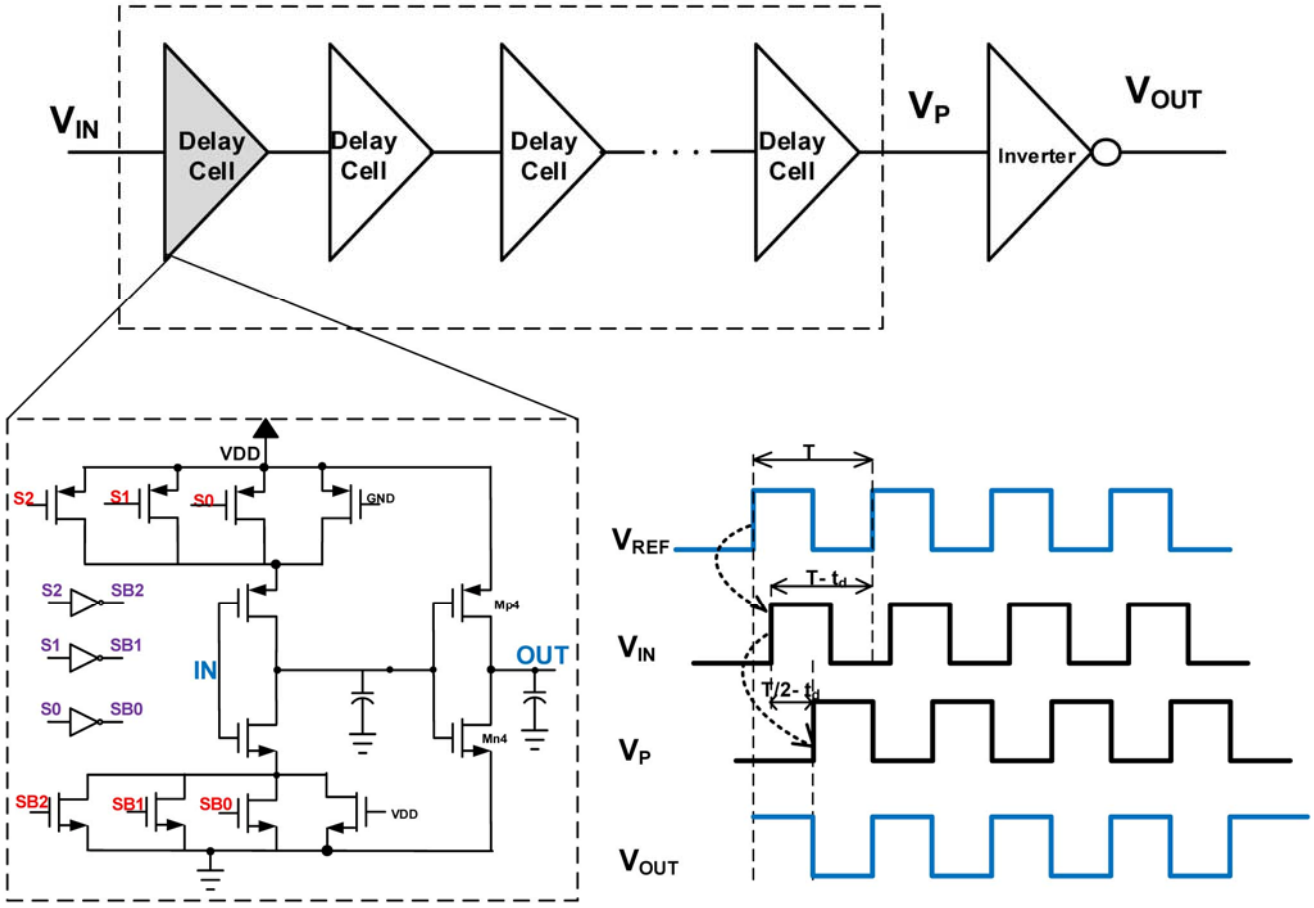


Fig. 6. Variable Delay Line Implementation.

The variable delay line (VDL) is implemented using current –starved driver structure, as shown in Fig. 6.

In addition to the two cascaded inverters, the current–starved delay has two additional PMOS and NMOS to extend the delay value. The delay value of the circuit is inversely proportional to the current. This is presented in Eq. (3). Therefore, three control bits S [0:2] are used as switches to turn on and turn off three PMOS at the high side of the delay cell.

$$t_{delay} = \frac{C_L * V_{DD}}{2 * I} \tag{3}$$

The VDL consists of several delay cells that are connected in series, as shown in Fig. 6. In this study, an inverter was used to reduce the number of delay cells, power consumption and chip area. Conventionally, the VDL needs to compensate for a delay time of T- td, where T is the period of the reference voltage, V_{REF}, and td is the delay time to align V_{REF} and V_{OUT}. With an operation frequency of 6.78MHz, the period time is 147ns; the delay time of the comparator is approximately 18ns, and the compensation delay time is 129ns. When the maximum delay time of each delay cell is 8.5ns, at least 15 cells are needed. This number of cells will increase power consumption significantly as well as the area of the rectifier. As illustrated in Fig. 6, an inverter is used to shift the signal 180° in phase after passing the T/2- t_d delay line. As a result, V_{OUT} and V_{REF} are aligned.

3.2 Final Proposed Active Rectifier architecture

Fig. 7 presents a full schematic of the proposed rectifier. In this active rectifier, four main diode connected MOSFET $M_{N1, 2, 3, 4}$ are NMOS instead of PMOS as reported in previous works. The benefit from this replacement is very easy to see. With NMOS, the frequency response is better than PMOS. In addition, the size of NMOS is also smaller, which saves the area of the chip.

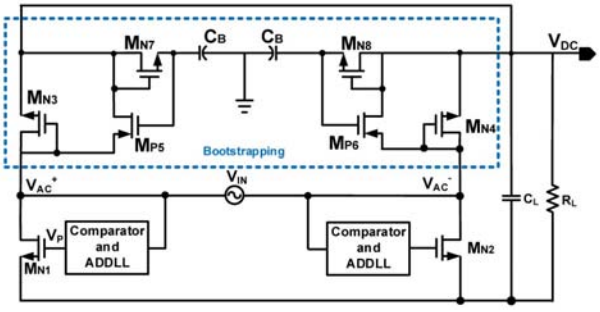


Fig. 7. Proposed Rectifier.

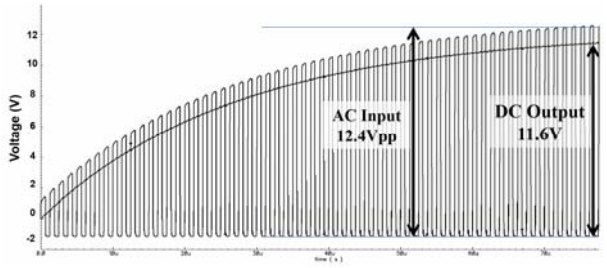


Fig. 8. Input/output voltage.

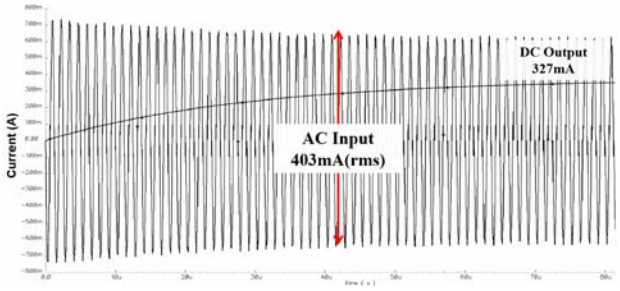


Fig. 9. Input/output current.

Fig. 7 presents a new rectifier that combines the bootstrapping techniques and ADDLL circuit to enhance the PCE. The bootstrapping technique is applied to a pair of diode-connected NMOS at the high side of the rectifier to reduce the effective drop voltage. The other pair of NMOS gates are driven by the combination of a comparator and ADDLL. This combination becomes a zero compensation circuit, which cancels the delay time caused by the comparator.

4. Experiment Results

This new rectifier was implemented at the circuit level using 0.35 μm CMOS technology with a Spectre simulator under the Cadence environment. The source input port was 5 W power, 50 Ω impedance and its frequency was set to 6.78 MHz. In this study, the bootstrapping technique resulted in an approximate 5% increase in PCE, whereas the ADDLL circuit cancelled the delay effectively and increased the efficiency by approximately 7%.

The rectifier supplies power to the electronic devices, which are considered the active loads. The impedance of the active loads is unstable. A variation of the load will cause a variation of the output current. Therefore, the power conversion efficiency will be affected. To check the variation of the power conversion efficiency dependent on the load current, the variation load is applied to create a variation current at the load and the efficiency is measured, as shown in Fig. 10.

As shown in Fig. 10, the power conversion efficiency decreased significantly when the output current exceeded 340mA. The maximum efficiency was obtained at output currents from 220mA to 300mA. This current range matches the target current consumption of most of the modern micro-electronic devices.

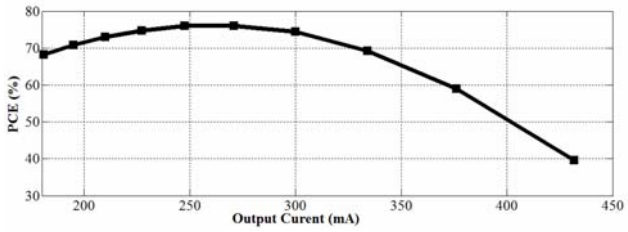


Fig. 10. Power efficiency with the load current.

Table 1. Performance summary and comparison.

Parameters	[2]	[3]	This work
Process	0.35 BCDMOS	0.18 TSMC	0.35 TOWER JAZZ
Input Frequency	3.23MHz 6.78MHz	10MHz	6.78MHz
Input voltage	4.0~8.0V_{rms}	0.8Vp 3.3Vp	12.4Vpp
Input current	-	-	403$mA_{,rms}$
Input power	-	-	5W
Output voltage	-	0.49V 2.8V	11.6V
Output current	-	-	327mA
Output power	-	-	3.8W
PCE	81% 74%	67% 86%	76%

5. Conclusion

This paper presented the proposed new rectifier architecture using the bootstrapped technique and ADDLL circuit. This active rectifier was implemented in 0.35 μm CMOS technology. Comparing to the conventional rectifier, the PCE of the rectifier in this study was increased by 11%. According to the simulation result, the PCE of the proposed rectifier architecture reached 76% at an input frequency of 6.78MHz.

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