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High accuracy, Low Power Spread Spectrum Clock Generator to Reduce EMI for Automotive Applications

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** Short Paper*

***Abstract*:** This paper presents a Spread Spectrum Clock Generator (SSCG) based on Relaxation oscillator using Up/Down Counter. The current is controlled by a counter and the spread spectrum of the Relaxation Oscillator. A Relaxation Oscillator with temperature compensation using the BGR and ADC is presented. The current to determine the frequency of the Relaxation Oscillator can be controlled. The output frequency of the temperature can be compensated by adjusting the current according to the temperature using the code that is the output from the ADC and BGR. EMI Reduction of SSCG is 11 dB, and Spread down frequency is 150 kHz. The current consumption is 600 μA from 5V and the operating frequency is from 2.3 MHz to 5.75 MHz. The rate of change of the output frequency with temperature was approximately ±1 %. The SSCG is fabricated in a 0.35um CMOS process with active area 250um x 440um.

***Keywords*:** Low power, Spread spectrum clock generator, Relaxation oscillator, Temperature compensation

1. Introduction

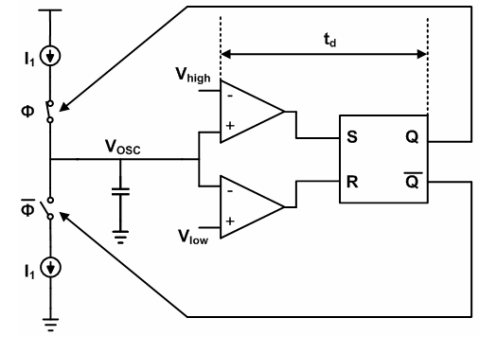
Recently, the continuous shrinking of the device feature sizes introduced by the aggressive technology scaling trends, and the increasing complexity of digital ICs, require higher operating frequencies with faster clock rates. ICs are becoming prolific Electro Magnetic Interference (EMI) generators because of the high-frequency square-waves rich in harmonics and distributed throughout the die. Until recently, however, the circuit, package, and board designers did not give much consideration to EM emissions and interference. Traditionally, the problem of reducing on-chip EMI has been tested, and implemented by trial-and-error, without a structured approach [1]. On-chip reference oscillators are required for low-cost one-chip applications including biomedical sensors, microcomputers, high-speed interfaces such as DDR I/F and HDMI, and SoCs. RC oscillators, including relaxation oscillators, were developed to realize on-chip oscillators with a standard CMOS process [2]. The oscillator used in the analog circuit can be divided into two main circuits, which are the LC oscillator and RC oscillator. The LC oscillator and RC oscillator are used in high frequency band and low frequency band, respectively. Because the Phased Locked Loop (PLL) is not used in low frequency band, the characteristics of the oscillator itself should be highly reliable.

The percentage of electronic devices in cars is increasing. The EMI to other electronic devices can cause a malfunction. Because a large amount of EMI might affect each electronics device, it is essential to reduce the EMI emissions in each device [3].

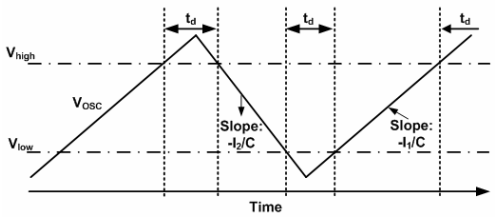
The remainder of this paper is organized as follows. In Section 2, the Block diagram of the Proposed Relaxation Oscillator is described. Section 3 describes the building blocks. Section 4 presents the experimental results from the 0.35 μm CMOS implementation and section 5 presents the concluding.

2. Proposed Relaxation Oscillator

Fig. 2 shows the block diagram of the Relaxation Oscillator with Temperature Compensation Circuit (TCC) and the Spread Spectrum Clock Generator (SSCG). The TCC is composed of a Proportional to Absolute Temperature (PTAT) Generator, a 4-bit ADC, a Decoder, and Reference Generator using Bandgap Reference (BGR).



(a)



(b)

Fig. 1. (a) Block diagram, (b) Waveform of the Conventional Relaxation oscillator.

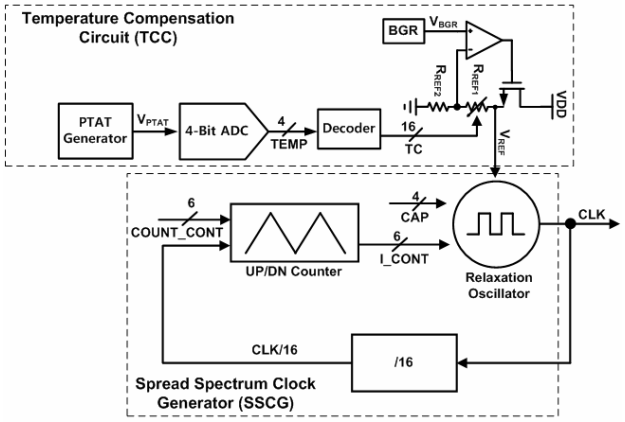


Fig. 2. Block diagram of the Proposed Relaxation Oscillator with temperature compensation and spread spectrum Clock generator.

The SSCG is composed of a Relaxation Oscillator, a UP/DN Counter, and a 16-Divider. The SSCG generates the counter signal by the self-clock feedback and controls the frequency of the Relaxation Oscillator. The input of UP/DN Counter uses clocks that are 16-divided to operate the counter. The automotive IC must have high reliability in any circumstances. The EMI which can affect each block and causes the wrong operation needs to be reduced.

3. Building Blocks

3.1 Relaxation Oscillator

Fig. 3 shows a schematic of the Relaxation Oscillator. The structure of the proposed oscillator generates a

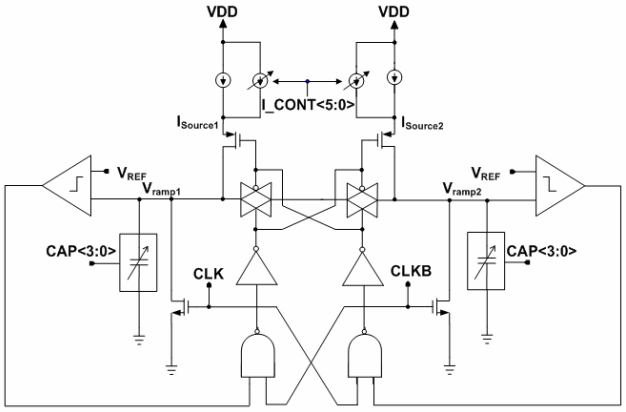


Fig. 3. Schematic of the Relaxation Oscillator.

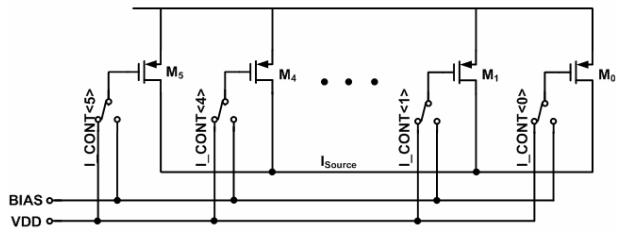


Fig. 4. Controllable current source.

frequency by charging and discharging the current of the capacitor continuously. Using the SR latch, charge and discharge, set-reset occur repeatedly to have a structure that is applied to the comparator inputted in to the SR latch. The output of the capacitor is again the charged and discharged voltage. Using the logic to generate a different frequency from the other oscillator, the structure is a structure suitable to consume less current, and generate a low frequency.

$T_{ramp1} = T_{ramp2} \fallingdotseq 2T_{OSC}$. The frequency of oscillation is given by [4] :

$$C\frac{dV_{ramp}}{dt_{ramp1}} = I_{source} \tag{1}$$

$$\therefore f_{osc}(Hz) \approx \frac{1}{t_{osc}} = \frac{I}{2CV_{ramp}} \tag{2}$$

The frequency of the Relaxation Oscillator is determined by the current, capacitance, and value of V_{REF} in Eq. (2).

3.2 Spread Spectrum Clock Generator

Fig. 5 shows the block diagram of the Spread Spectrum Clock Generator (SSCG). The proposed Spread Spectrum Clock Oscillator generates the counter signal by the self-clock feedback and controls the frequency of the Relaxation Oscillator. This is composed of a UP/DN Counter, 16-Divider, and Relaxation Oscillator. The SSCG can control the frequency by controlling the capacitor and the current bank. The PMOS Current bank composed by 6-bit controls the current following the signals from the

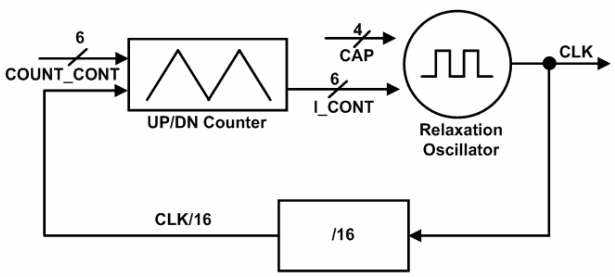


Fig. 5. Block diagram of SSCG.

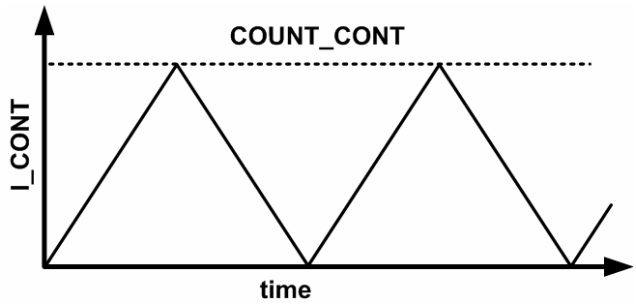


Fig. 6. Simulation result of the UP/DN Counter.

counter block to spread the spectrum of the Relaxation Oscillator. The 16-Divider is implemented by a series connection of four D flip-flops.

Fig. 6 presents the simulation results of UP/DN Counter. The output codes of UP/DN Counter (I_CONT<5:0>) change from '0' to the input code (COUNT_CONT<5:0>). Therefore, COUNT_CONT<5:0> control the spread range of the SSCG.

Fig. 7 shows the Fast Fourier Transform (FFT) simulation result of the spread spectrum clock generator. Fig. 7(a) shows how to generate a fixed frequency as the oscillator in general when applying a fixed digital code to the counter which is shown in Fig. 5. Fig. 7(b) shows the frequency changes. The spectrum is spread, when applying a digital code that varies at the counter.

3.3 Temperature Compensation

Fig. 8 shows the block diagram of the Temperature Compensation Circuit (TCC). The TTC is composed of PTAT Generator, 4-bit Flash ADC, Decoder, and Reference generator.

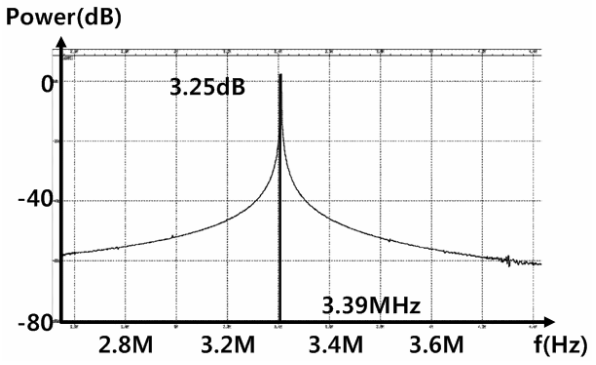
Fig. 9 shows the temperature compensation circuit. Lateral PNP transistors (Q1, Q2, and Q3) are used to implement the BGR [5]. Its output voltage can be derived as Eq. (3).

$$V_{PTAT} = V_{EB3} + V_T \times \ln(n) \times \frac{R_4}{R_3} \tag{3}$$

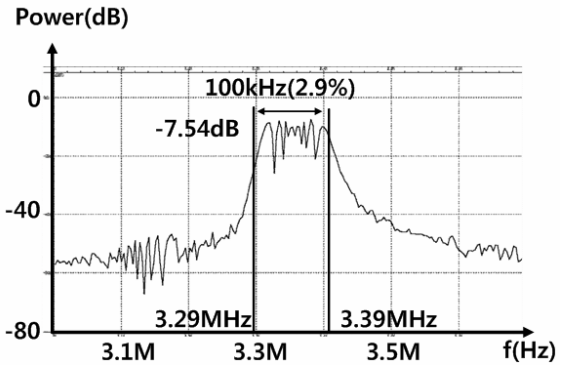
where n is the area ratio of Q2 and Q1.

The temperature coefficient can be derived as Eq. (4).

$$\frac{\partial V_{PTAT}}{\partial T} = \frac{\partial V_{EB3}}{\partial T} + \frac{k}{q} \times \ln(n) \times \frac{R_4}{R_3} \tag{4}$$



(a)



(b)

Fig. 7. (a) Turn off, (b) Turn on of SSCG.

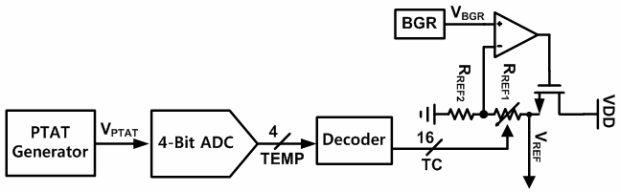


Fig. 8. Block diagram of the Temperature Compensation.

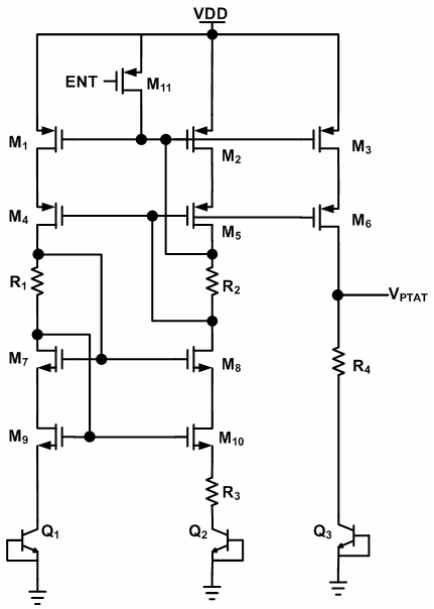


Fig. 9. Schematic of the PTAT Generator.

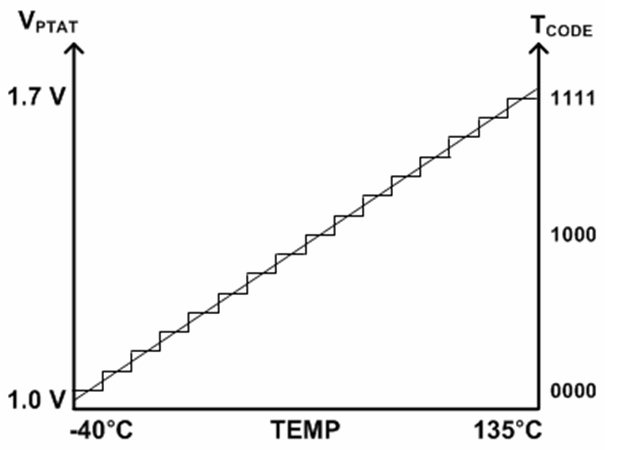


Fig. 10. Output of PTAT and output code of ADC according to the temperature variation.

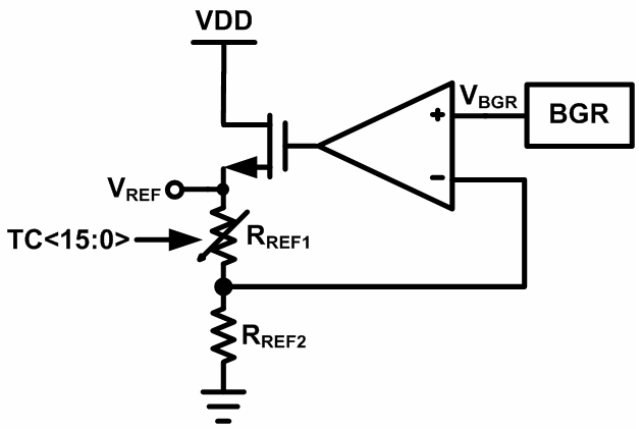


Fig. 11. Schematic of the Reference Generator.

where k is the Boltzmann constant.

The PTAT Generator can be implemented by adjusting n and (R4/R3) from Eq. (4).

Fig. 11 shows the Reference Generator which generates the reference voltage (V_{REF}) of the Relaxation Oscillator. V_{REF} is determined by the ratio of R_{REF1} and R_{REF2}, as shown in the expression below [5] :

$$V_{REF} = (1 + \frac{R_{REF1}}{R_{REF2}}) \times V_{BGR} \quad (5)$$

where V_{BGR} is the output voltage of BGR.

4. Experimental Results

Fig. 12 shows the chip layout of the proposed relaxation oscillator with the temperature compensation and SSCG. This chip was fabricated with 2-poly 4-metal CMOS 0.35um process. The size of the relaxation oscillator with SSCG is 240 μm x 210 μm and the size of temperature compensation circuit is 550 μm x 280 μm.

Fig. 13 shows the output frequency range of the Relaxation Oscillator by varying the CAP<3:0>. The

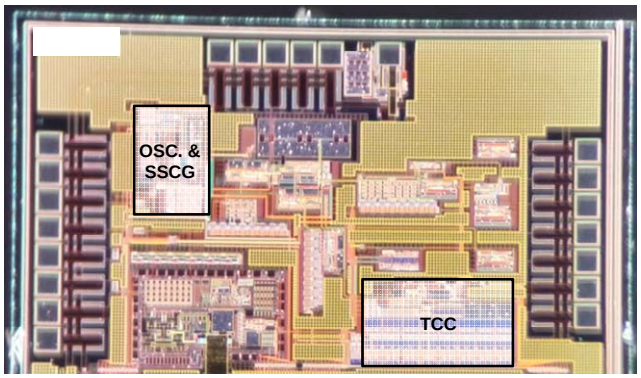


Fig. 12. Chip micrograph.

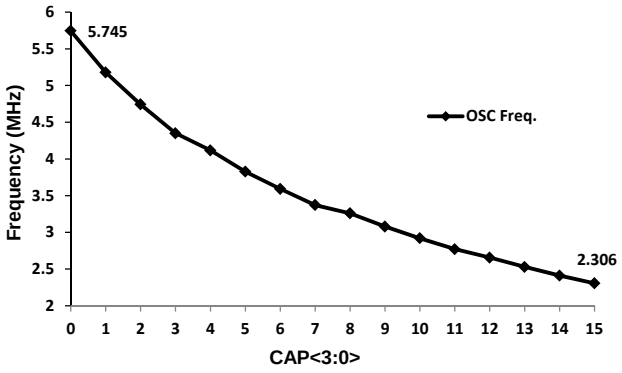


Fig. 13. Output Frequency range of the Relaxation Oscillator according to CAP<3:0>.

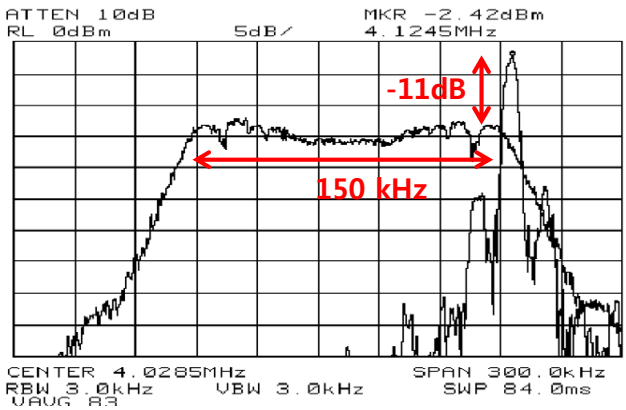


Fig. 14. Measurement Results of the SSCG operation.

figure shows the changing shapes of the frequency range according to the capacitance variation. Therefore, the frequency range of Relaxation Oscillator is from 2.3 MHz to 5.75 MHz.

Fig. 14 shows the measurement results of the SSCG. The measurement results showed that the clock signal power decreased about 11 dB and the frequency spread was reduced to approximately 150 kHz.

Fig. 15 presents the measurement results of temperature compensation. To verify the temperature compensation, CAP<3:0> was fixed to “0100” and both results were compared by turning on and off the temperature compensation circuit. As shown in the figure,

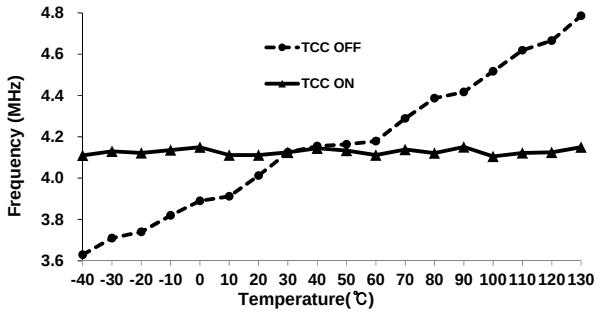


Fig. 15. Measurement result of the temperature compensation.

Table 1. Performance Summary.

	This work
Process	0.35um CMOS
Supply Voltage	5 V
Frequency	2.3 ~ 5.75 MHz
EMI Reduction	11 dB
Spread Spectrum	3.75 %
Accuracy	< 1 %
Temperature	-40℃ ~ 135℃
Current Consumption	0.6 mA
Chip Area	0.20 mm^2 (SSCG Core : 0.05 mm^2)

before the temperature compensation was adopted, approximately ± 28% output frequency error occurred when the temperature was varied from -40℃ to 135℃. By adopting the proposed temperature compensation using BGR and ADC under the same temperature condition, the output frequency error was reduced to have appoximately ±1%.

Table 1 lists the performance of the proposed SSCG. The current consumption is 600 μA from 5V and the operating frequency is ranged from 2.3 MHz to 5.75 MHz. the EMI Reduction of the SSCG is 11 dB, and the spread down frequency was 150 kHz. The rate of change of the output frequency with temperature was approximately ±1%.

5. Conclusion

A Relaxation oscillator with temperature compensation and a Spread Spectrum Clock Generator (SSCG) using Up/Down Counter is presented. The current was controlled by the counter and spread spectrum of the Relaxation Oscillator. The Relaxation Oscillator with temperature compensation using BGR and ADC is presented. The current to determine the frequency of the Relaxation Oscillator can be controlled. The output frequency of the temperature could be compensated by adjusting the current according to the temperature using the code that is output from the ADC and BGR. The EMI Reduction of SSCG was 11 dB, and the spread down frequency was 150 kHz. The current consumption was 600 μA from 5V and the operating frequency ranged from 2.3 MHz to 5.75 MHz. The rate of change of the output frequency with temperature was approximately ±1 %.

Acknowledgement

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