A 120 GHz Voltage Controlled Oscillator Integrated with 1/128 Frequency Divider Chain in 65 nm CMOS Technology

Namhyung Kim, Jongwon Yun, and Jae-Sung Rieh

Abstract—**A 120 GHz voltage controlled oscillator (VCO) with a divider chain including an injection locked frequency divider (ILFD) and six static frequency dividers is demonstrated using 65-nm CMOS technology. The VCO is designed based on the LC cross-coupled push-push structure and operates around 120 GHz. The 60 GHz ILFD at the first stage of the frequency divider chain is based on a similar topology as the core of the VCO to ensure the frequency alignment between the two circuit blocks. The static divider chain is composed of D-flip flops, providing a 64 division ratio. The entire circuit consumes a DC power of 68.5 mW with the chip size of 1385 × 835 μm^2.**

Index Terms—**Voltage controlled oscillator, injection locked frequency divider, phase noise**

I. INTRODUCTION

The need for high data transfer in communication systems is soaring with the explosive data traffic in our modern daily lives. This calls for a high demand for increased bandwidth for communication systems. Higher carrier frequency naturally leads to a wider bandwidth and thus systems operating at frequencies beyond 100 GHz are attracting increasing attention nowadays. In the D-band, in particular, the industrial scientific medical (ISM) band near 122 GHz and the atmospheric window around 140 GHz have drawn much interests from researchers for their visible application fields. Recently, the rapid development of CMOS technology has enabled the circuits operating over 100 GHz based on Si technologies. Hence, various CMOS circuits working at such frequency band have been reported [1-6].

One of the key challenges for implementing those communication systems operating at such high frequency band is the realization of stable local oscillation (LO) signal. When precise frequency control is critical, as in the case of advanced modulation schemes based on phase control, phase locked loops (PLLs) are highly preferred over free running voltage controlled oscillators (VCOs). For PLLs operating at raised frequency, the challenges lie not only on the VCO, but the frequency dividers that guarantee the operation at such high frequency band. Especially, for the frequency divider at the first stage of the divider chain, the popular static frequency dividers cannot be used any more due to the prohibitively high DC power consumption at the high frequency band, and the injection locked frequency dividers (ILFDs) are being seriously considered as a promising candidate owing to their low power operation [5]. However, one outstanding issue with ILFD is the relatively narrow locking range, which makes it difficult to align with the VCO oscillation frequency. Hence, there have been efforts to implement PLLs avoiding the use of high frequency divider [4], or to obtain high purity signals at raised frequencies by multiplying the frequency from PLLs operating at lower frequencies [3].

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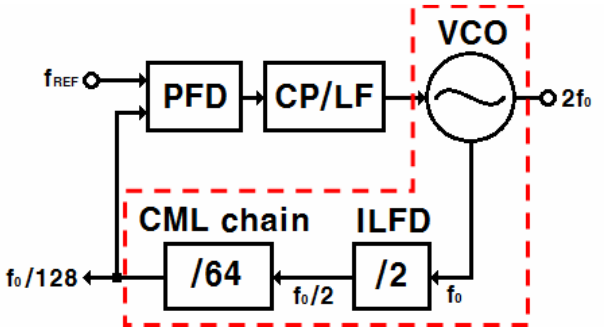

Fig. 1. Block diagram of a phase locked loop including the circuit proposed in this paper, which is surrounded with dotted line.

II. CIRCUIT DESIGN

The circuit is composed of a 120 GHz push-push VCO, 60 GHz /2 ILFD, and a 6-stage static frequency divider as shown in Fig. 1. For the VCO, the second harmonic signal ($2f_0$) generated from the push-push operation can be taken as the output of PLL if completed, while the fundamental signal (f_0) is injected into the input node of the following ILFD.

In this work, we address this issue by proposing a D-band VCO integrated with a divider chain that employs an ILFD as the first stage of the chain based on 65-nm CMOS technology. The topology of the ILFD was taken similar to that of the VCO core thus making the locking less vulnerable to external uncertainties. The ILFD was also made tunable with varactors for better frequency alignment.

1. VCO

The VCO adopts the push-push LC cross-coupled topology as shown in Fig. 2. In the oscillator core, the LC tank is composed of C_{var1} and C_{var2}, accumulation mode MOSFET varactors, and T1 and T2, microstrip lines of 50 ohm. The Q-factor of T1 and T2 was higher than 12 around 60 GHz. The blocking capacitors (C1 and C2) and external bias (V_{bias1}) are added in order to linearize the tuning behavior of the VCO against the tuning voltage [7]. The fundamental output signal f_0 is available at the differential output nodes. One node leads to the single-ended input of the following ILFD, while the other node is connected to the probing pad intended for f_0 monitoring, both through source follower buffers

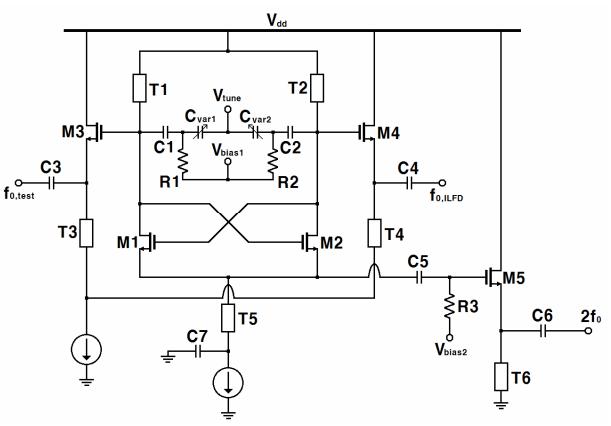

Fig. 2. Schematic of the D-band push-push VCO.

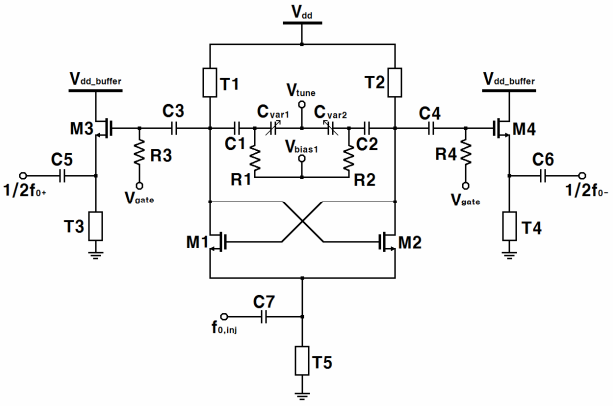

Fig. 3. Schematic of the V-band ILFD.

(M3 and M4). The second harmonic signal $2f_0$ around 120 GHz is extracted at the common node of M1 and M2 through a source follower buffer (M5). The lengths of T5 and T6 were tuned around $\lambda/4$ of the second harmonic for frequency selection. As the high frequency VCO is very sensitive to the variation of the voltage bias, current biasing was used with current sources implemented by current mirrors.

2. ILFD

The schematic of the ILFD designed for /2 frequency division is shown in Fig. 3. As mentioned earlier, the topology of the ILFD was selected similar to that of the VCO core. In this way, external variations that may affect the operation frequencies of the VCO and ILFD, such as uncertainties in the device model and EM simulation, may shift the frequencies in the same direction, maximally retaining the frequency alignment

between the two circuits. The varactors included in the circuit core also serve as a tool to additionally adjust the frequency alignment by controlling the free running frequency of the ILFD. For the injection of the input signal, the tail injection method is used together with a transmission line current path (T5), which can resonate out the parasitic capacitances from M1 and M2.

The locking range of the frequency divider is inversely proportional to the quality factor of the tank and the ratio between the injection current and the oscillator current as shown below [8]:

$$\omega_L \approx \frac{\omega_0}{2Q} \cdot \frac{2}{\pi} \cdot \frac{I_{inj}}{I_{osc}}. \quad (1)$$

The varactors described above help to degrade the Q-factor of the tank, leading to a locking range improvement according to (1). As another effort to increase the locking range, the ratio between the injection and the oscillation currents was increased by pushing the drain voltage down to the minimum value required for ILFD oscillation.

3. CML divider chain

The CML dividers employed in the design to provide a 1/64 frequency division with a 6-stage chain is based on a D-latch circuit [9]. Each stage adopts the same topology, which is composed of two coupled CML latches as depicted in Fig. 4(a). The CML latch is built with two transistor pairs as shown in Fig. 4(b), in which the size of the resistors and transistors are optimized for each stage to meet the target frequency of the stage. Typically, the inputs of CML dividers are driven by differential rail-to-rail clock, leading to clear switching of the circuit. In the proposed circuit, however, the output power from the ILFD, which drives the following CML divider, may not be sufficiently strong. Hence, blocking capacitors and external voltage bias are inserted to the first 3 stages of the CML divider chain for a clear switching of the circuit by adjusting the gate bias level for maximum device switching. An output buffer is placed at the end of the divider chain for measurement purpose.

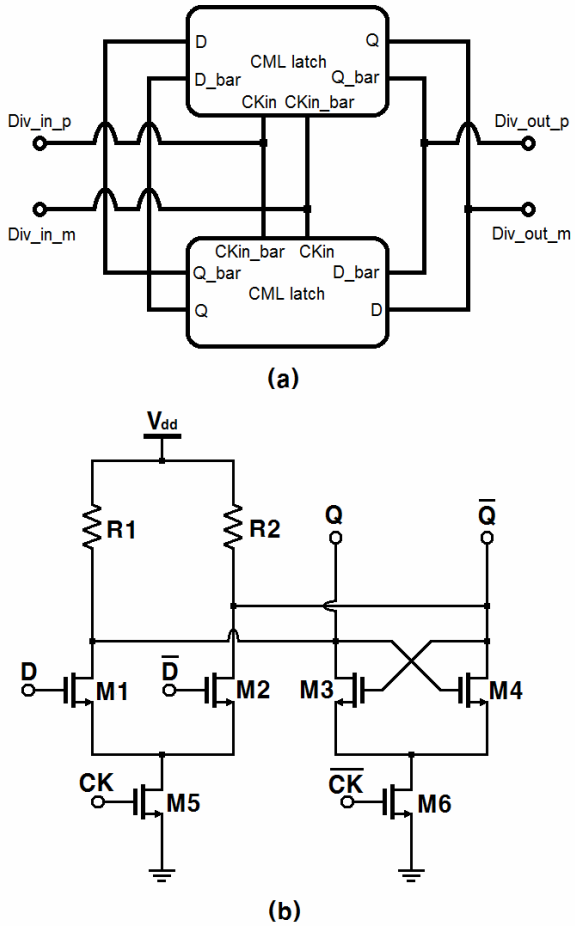

Fig. 4. CML static divider (a) Block diagram of the CML static divider, (b) Schematic of the CML-latch inside CML static divider.

III. MEASUREMENT

The circuit was implemented using Samsung 65-nm CMOS technology. Fig. 5 shows the die photo of the fabricated chip. The area including probing pads is 1385 $\times$ 835 μm^2. The entire circuit, as well as the individual VCO and ILFD separated for testing, were measured through on-wafer probing using D-band and V-band measurement setups.

The measurement setups for the VCO test circuit are shown in Fig. 6. For the second harmonic signal frequency measurement, a D-band setup was used, in which a Quinstar D-band harmonic mixer is connected with an Agilent E4407B spectrum analyzer. As shown in Fig. 7, the output frequency varies from 116.5 GHz to 118.4 GHz as the tuning voltage is swept from 0 to 1.5 V. The output power of the signal was directly measured with an Ericson PM4 power meter to avoid uncertainty

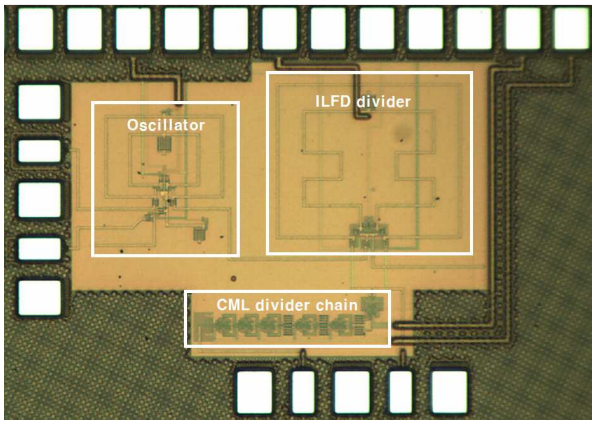

Fig. 5. Photo of the fabricated chip including D-band push-push VCO, V-band ILFD and CML divider chain.

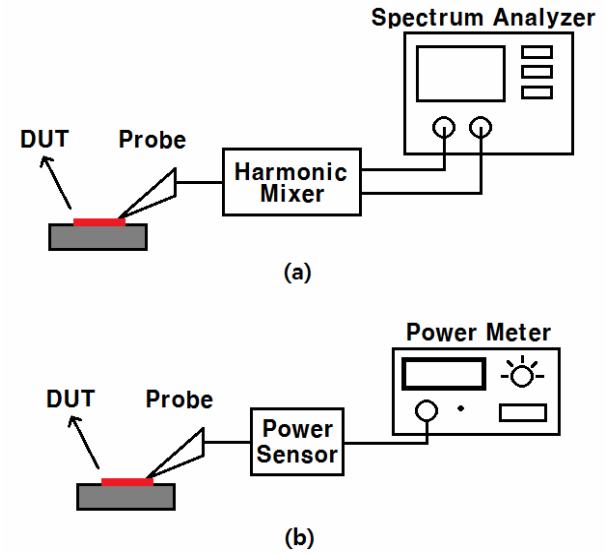

Fig. 6. Measurement setup for VCO (a) Spectrum measurement, (b) Output power measurement.

on the power loss with the mixer. The measured output power is around -21 dBm over the entire tuning range with the probe loss accounted for. The fundamental signal was measured with a V-band setup, which is similar to the D-band setup with small modifications. The frequency was measured with an Agilent V-band 11974V preselected harmonic mixer connected with the spectrum analyzer. The operation frequency is about a half of the second harmonic signals as shown in Fig. 8. Comparison with Fig. 7 reveals a slight deviation from a half of the second harmonic signal frequency, which is ascribed to the different loading effect of the probing for each test. The output power is around -1 dBm with the probe loss de-embedded, which is expected to be

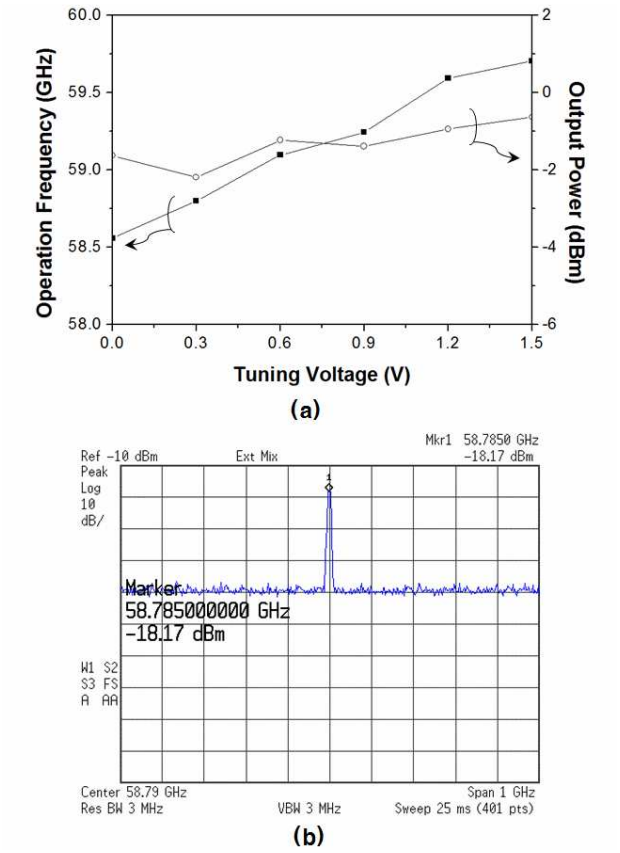

Fig. 7. Measured properties of the fundamental output signal of the VCO (a) Operation frequency and output power versus tuning voltage, (b) Output spectrum.

sufficient to drive the following ILFD circuit. The VCO draws 24 mA from a 1.5 V supply voltage, including the output buffers.

The ILFD test circuit was characterized for locking range with the setup described in Fig. 9. It is composed of a HP 83650B signal generator connected with OML V-band source module and the spectrum analyzer. Fig. 10 shows the extracted locking range of the ILFD for varactor tuning voltages. The locking range was around 3.5 GHz for a fixed varactor state with an injection power level of around -1 dBm. With the extra varactor tuning, an operation range over 5 GHz was obtained with the input frequency of around 30 GHz. The ILFD core and the buffer draw 6 mA and 4 mA from a 0.8 V and 1 V supply, respectively, leading to a total DC power consumption of 8.8 mW.

Finally, the entire circuit was characterized. The spectrum of the divided signal (f_0/128) at the output of the circuit is shown in Fig. 11(a). The phase noise of the output signal was also measured, which is presented in

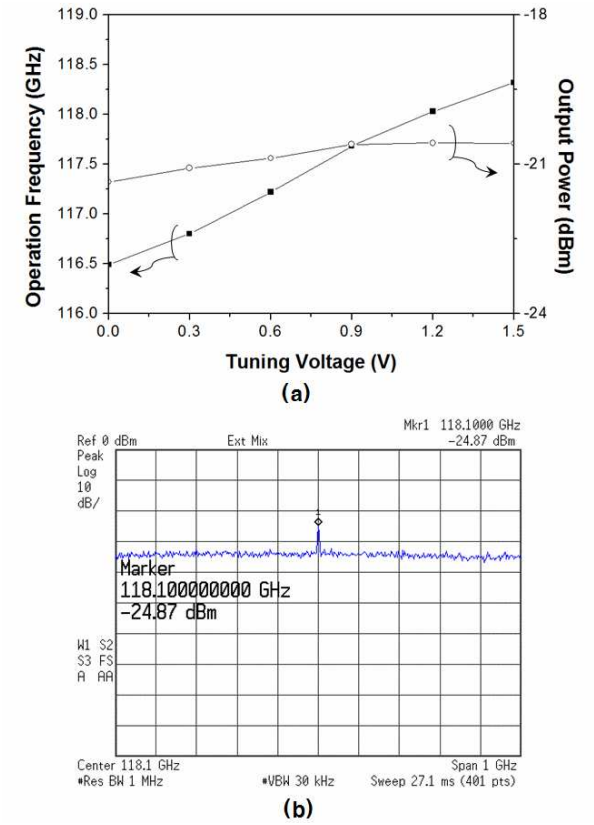

Fig. 8. Measured properties of the second harmonic output signal of the VCO (a) Operation frequency and output power versus tuning voltage, (b) Output spectrum.

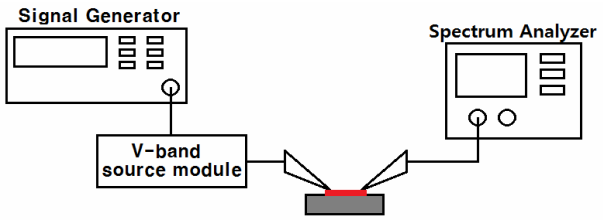

Fig. 9. Measurement setup for ILFD.

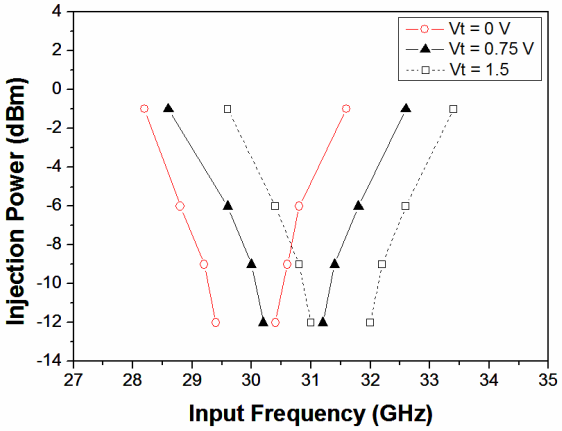

Fig. 10. Measured sensitivity curves of the ILFD with various varactor tuning voltages.

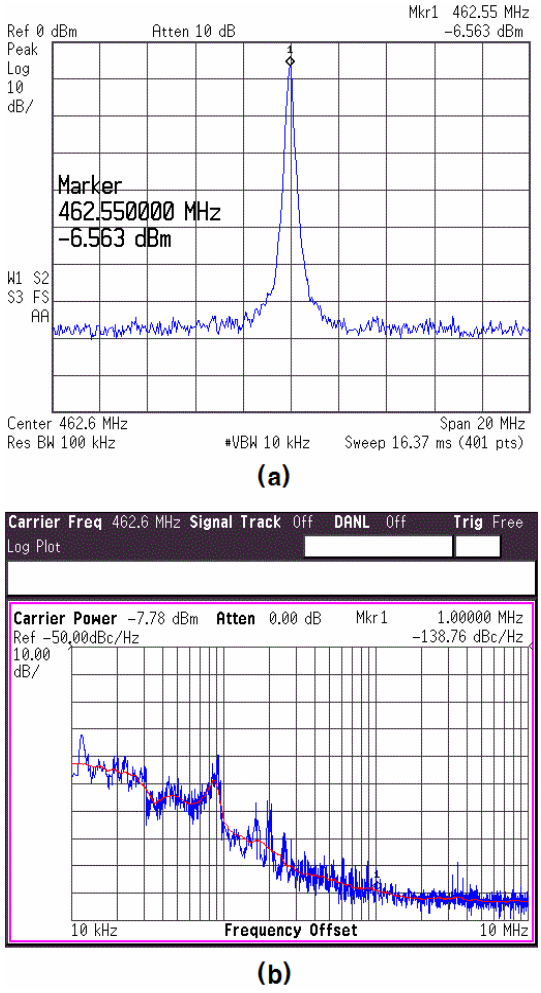

Fig. 11. Measured divider characteristics (a) Output spectrum at the output of the divider chain, (b) Phase noise at the divider chain.

Fig. 11(b). The measured phase noise is -138.8 dBc/Hz at 1 MHz offset at the 462.6 MHz carrier frequency. The total power consumption of the full chip is 68.5 mW including the 36 mW and 8.8 mW from the VCO and ILFD, respectively. The first stage of the CML divider consumes a larger DC power than the remaining 5 stages as it needs to handle the rather weak signal from the ILFD, drawing 6 mA from a 2.2 V supply. The other 5 stages together draw 7 mA from a 1.5 V supply voltage. The phase noise plot shown in Fig. 11(b) not only presents the phase noise property of the divided signal, but also serves to indicate the phase noise of the VCO output signal. The direct measurement of the phase noise of the VCO is difficult due to the high conversion loss of the D-band external mixer used for frequency down-conversion, which can be as large as ~60 dB. From the

Table 1. Comparison of Si-based Oscillators Integrated with Dividers Operating beyond 100 GHz

	[10]	[11]	[12]	This work
Technology	0.13 um SiGe HBT	0.12 um SiGe HBT	0.25 um SiGe HBT	65 nm CMOS
Tuning Range	166.2 GHz (fixed)	139 - 150 GHz	168 - 181 GHz	116.5 - 118.4 GHz
Phase Noise (@ 1 MHz offset)	N/A	-83 dBc/Hz	-82 dBc/Hz	-90.6 dBc/Hz
Power Consumption	900 mW*	99 mW	59 mW	68.5 mW
Total Division Ratio	2	16	32	128
Oscillator FoM	N/A	-166.6 dBc/Hz	-168.8 dBc/Hz	-173.3 dBc/Hz

*Entire transceiver additionally including 3 amplifiers and a mixer

measured phase noise of the divided signal, the phase noise of the D-band output signal of the VCO is estimated to be -90.6 dBc/Hz at 1 MHz offset. The corresponding FoM of the VCO is -176.5 dBc/Hz. Finally, the measured performance of the implemented VCO integrated with frequency divider chain over 100 GHz is summarized in Table 1 and compared with previous works.

IV. CONCLUSIONS

A 65-nm CMOS D-band push-push VCO integrated with a frequency divider chain of 1/128 division ratio composed of an ILFD stage 6 CML divider stages was demonstrated in this work. For accurate frequency alignment between the VCO and the ILFD, a similar topology was adopted for the two circuits with additional tuning capability for the ILFD. The VCO exhibited a tuning range of 116.5 GHz to 118.4 GHz with the second harmonic and the divider chain brought the frequency down to around 460 MHz from the fundamental frequency of the VCO. The total power consumption of the full chip was 68.5 mW. The circuit can be readily applied to a D-band PLL, which will serve as a critical component for communication systems operating at D-band.

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