http://dx.doi.org/10.5573/JSTS.2014.14.1.096 JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.14, NO.1, FEBRUARY, 2014

# Computing-Inexpensive Matrix Model for Estimating the Threshold Voltage Variation by Workfunction Variation in High-κ/Metal-gate MOSFETs

**Gyo Sub Lee and Changhwan Shin**

***Abstract*—In high-κ/metal-gate (HK/MG) metal-oxide-semiconductor field-effect transistors (MOSFETs) at 45-nm and below, the metal-gate material consists of a number of grains with different grain orientations. Thus, Monte Carlo (MC) simulation of the threshold voltage ($V_{TH}$) variation caused by the workfunction variation (WFV) using a limited number of samples (*i.e.,* approximately a few hundreds of samples) would be misleading. It is ideal to run the MC simulation using a statistically significant number of samples (> ~ $10^6$); however, it is expensive in terms of the computing requirement for reasonably estimating the WFV-induced $V_{TH}$ variation in the HK/MG MOSFETs. In this work, a simple matrix model is suggested to implement a computing-inexpensive approach to estimate the WFV-induced $V_{TH}$ variation. The suggested model has been verified by experimental data, and the amount of WFV-induced $V_{TH}$ variation, as well as the $V_{TH}$ lowering is revealed.**

***Index Terms*—Variability, workfunction variation, high-κ/metal gate, MOSFET, CMOS**

## I. INTRODUCTION

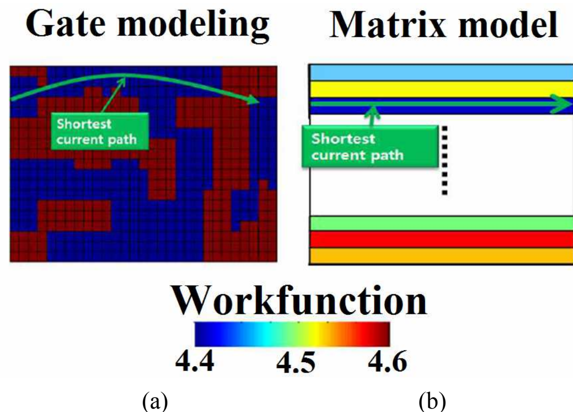
Since the high-κ/metal-gate (HK/MG) technology was adopted in the 45-nm CMOS technology, the workfunction variation (WFV) in the metal-gate has been emerged as one of the main random variation sources, such as the line-edge-roughness (LER) and random-dopant-fluctuation (RDF). In HK/MG metal-oxide-semiconductor field-effect transistors (MOSFETs), the WFV depends on not only the total number of grains and each grain's orientation but also the positional combination of the grains in the metal-gate material. In [1] and [2], the statistical distribution of the workfunction values (including the mean and standard deviation) in the HK/MG MOSFETs has been studied. However, for identical distribution of the workfunction values (*i.e.,* for the same average and standard deviation of the workfunction values), the placement effect of the grains on the WFV-induced threshold voltage ($V_{TH}$) variation in the HK/MG MOSFETs were not investigated. In this study, the leakiest current path mainly formed along the regions of relatively lower workfunction values or "lucky-channel" between the source and the drain in the HK/MG MOSFETs will be reconfigured using the Monte Carlo (MC) simulation. The WFV-induced $V_{TH}$ lowering and variation in the HK/MG MOSFETs fabricated by the 28-nm low-power CMOS technology [3] will be investigated.

## II. MODELING THE WFV

A matrix for a given gate area (equivalent to channel length × channel with) is created, whose individual element corresponds to 1 nm × 1 nm square-shaped sub-area in the gate area. We note that 1 nm is small enough

Manuscript received May. 10, 2013; accepted Oct. 25, 2013
University of Seoul - Electrical and Computer Engineering 404 Information Technology Building, 163 Siripdaero, Dongdaemu-Gu Seoul 130-743 Korea, Republic of
E-mail : cshin@uos.ac.kr

(*vs.* the average grain size of the metal-gate materials used in the industry, such as TiN, which is ~ 22 nm [3]). Since the grain size of TiN follows the Gaussian distribution, the probability of having the 6-sigma-lower grain size than the average grain size (*i.e.,* average grain size of 22 nm and sigma/standard-deviation of 0.7 nm) is "1 over 505 million". Hence, the grain size of 1 nm by 1 nm is very fine, if the average grain is a few tens of nano-meters. However, if the grain size is a few nano-meters, then the smaller unit grain size than 1 nm should be used in this work. Referring to the characteristic table of materials, including the grain orientation and its corresponding workfunction value [1], all the components in the matrix appeared to be filled with the statistically assigned grain orientation values and their corresponding workfunction values. Fig. 1(a) shows that the matrix for the gate area (equivalent to 24 nm × 30 nm) of TiN is generated based on the characteristic table of TiN [2]. Previous studies have shown that the workfunction distribution of the gate materials in HK/MG MOSFETs follows the Gaussian probability distribution [1]. The Gaussian distribution of the workfunction values is achieved in the simple matrix model (Fig. 2).




(a) (b)

**Fig. 1.** TiN has two workfunction values of 4.4 eV and 4.6 eV for the grain orientations of <111> and <100>, respectively. The probability of selecting <111> and <100> is 40 % and 60 %, respectively (a) A completed matrix for the TiN metal gate, (b) the reconfigured matrix for estimating the worst WFV-induced $V_{TH}$ lowering and variation.

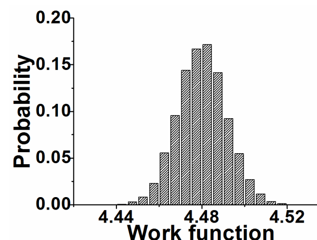



**Fig. 2.** The Gaussian distribution of the workfunction values in the TiN metal-gate with the simple matrix model used for stochastically generating the grains.

## III. Monte Carlo (MC) Simulation

To investigate the placement effect of the grains on the WFV-induced $V_{TH}$ variation, each row within the matrix shown in Fig. 1(a) was reconfigured and repositioned without affecting the mean/standard deviation of the workfunction values for the whole metal-gate area (Fig. 1(b)). Each row has a locally averaged workfunction value of the elements for the corresponding row. The reconfigured matrix was intentionally created to show the worst-case WFV-induced $V_{TH}$ (*i.e.,* one of the generated rows would become the shortest *lucky channel* consisting of the lowest potentials for the current carriers along the physical gate length). Using MC simulation to estimate the worst-case WFV-induced $V_{TH}$ variation (*i.e.,* $\sigma(V_{TH})$ by WFV), the 200 samples shown in Fig. 1(a) were generated. Then, each of the samples was reconfigured to have its own shortest lucky channel. We reasonably expected that the mean and standard deviation values in the WFV-induced $V_{TH}$ variation would decrease and increase, respectively, because of the reconfigured lucky channels.

For the metal-gate in 28-nm low-power MOSFETs [3], the mixed-mode TCAD [4] simulation of the reconfigured matrix as well as the non-reconfigured matrix with parallel-connected rows, was performed to physically understand the WFV-induced $V_{TH}$ variation and lowering observed in the experimental data. The mixed-mode TCAD simulation is used to test a function or characteristic of the circuit that is connected with two (or more) devices, when the set of the device parameters are not precisely characterized in the library of the COMPACT model. In this work, each row is corresponding to a device in the mixed-mode simulation. By connecting several devices (but with different WF) in parallel, the mixed-mode simulation has been performed. Hence, in the sense of connecting the devices in TCAD simulation, it can be referred that this work used the mixed-mode TCAD simulation.

The simulated nominal device was calibrated from the

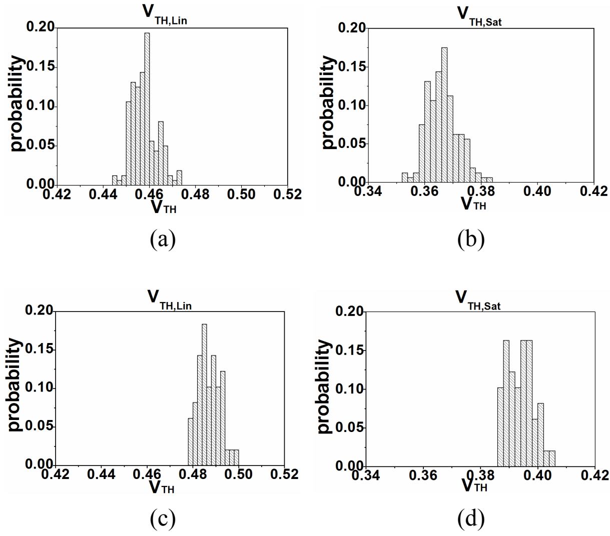



**Fig. 3.** Distribution of $V_{TH}$ (**a** and **b**) for the devices with lucky channels and (**c** and **d**) for the devices without lucky channels (a) $V_{TH,\ Lin}$ when $V_{DS} = 0.05$ V, (b) $V_{TH,-\ Sat}$ when $V_{DS} = 1.0$ V, (c) $V_{TH,\ Lin}$ when $V_{DS} = 0.05$ V, (d) $V_{TH,\ Sat}$ when $V_{DS} = 1.0$ V.

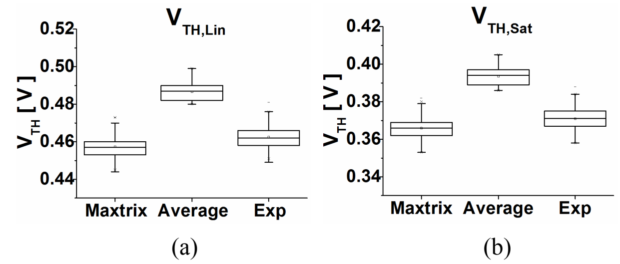



**Fig. 4.** Box-and-whisker plots of the $V_{TH}$ distribution of the matrix model, average-model, and experimental data (a) $V_{TH,Lin}$, (b) $V_{TH,Sat}$.

experimental current-*versus*-voltage curve in [3]. From the mixed-mode TCAD simulation, the WFV-induced $V_{TH}$ distribution for both the non-reconfigured and reconfigured devices was extracted from the 200 different samples in each case. Fig. 3 shows that the $V_{TH}$ distribution itself still follows the Gaussian distribution irrespective whether the matrix for the metal-gate is reconfigured or not. However, a difference exists between the two cases in terms of the average and standard deviation in $V_{TH}$.

Fig. 4 shows that the mean of the WFV-induced $V_{TH}$ distribution was reduced by approximately 300 mV, and its variation fluctuated more, primarily because of the existing lucky channels. Compared with the experimental data shown in Fig. 4, the limited number of MC simulation runs with the non-reconfigured gate matrix would be too optimistic in evaluating the WFV-induced $V_{TH}$ variation. Either a significantly large number of samples or the samples reconfigured by the simple matrix models suggested in this work should be considered in estimating the WFV-induced $V_{TH}$ variation because some of the fabricated devices with the lucky channel would significantly lower the mean of the $V_{TH}$ distribution as well as increase the standard deviation. Therefore, in estimating the WFV-induced $V_{TH}$ variation, MC simulation with statistically-significant number ($> \sim 10^6$) of samples should be performed. However, to efficiently estimate the variation, MC simulation with a few hundreds of the reconfigured matrices (*i.e.,* importance-sampling-like MC simulation) would be sufficient.

The details on the experiment are as follows: On the (100) epi-silicon substrate, the MOSFETs with <110> channel orientation were fabricated. After the shallow trench isolation (~2800 Å in depth) process for device-to-device isolation, P-well and $V_{TH}$-adjustment ion implantation (*i.e.,* B with ~100 keV in the order of $10^{13}$ $cm^{-2}$ and $BF_2$ with ~30 keV in $10^{13}$ $cm^{-2}$) as well as N-well and $V_{TH}$-adjustment ion implantation (*i.e.,* P with ~220 keV in $10^{13}$ $cm^{-2}$, As with ~125 keV in $10^{13}$ $cm^{-2}$, and another As with ~60 keV in $10^{13}$ $cm^{-2}$) were performed, followed by spike annealing at 1040 ºC. The HK/MG gate stack (*i.e.,* $SiO_2$ interface layer for ensuring high mobility + HfSiON high-k dielectric layer + carbon-incorporated TiN mono-layer + Poly-Si in consecutive order, away from the substrate) was formed using the double-patterning/double-etching. The lightly-doped-drain (LDD) and the halo region for n-type devices was doped using ion implantation with Ge(21- keV in the order of $10^{14}$ $cm^{-2}$)/F(12 keV in $10^{15}$ $cm^{-2}$)/As(2.3 keV in $10^{15}$ $cm^{-2}$) and B(30 º-tilted, 6.5 keV in $10^{13}$ $cm^{-2}$), respectively. The LDD and the halo region for p-type devices was doped by ion implantation with Ge(12.5 keV in $10^{14}$ $cm^{-2}$)/F(2.7 keV in $10^{15}$ $cm^{-2}$)/BF(3.5 keV in $10^{14}$ $cm^{-2}$) and As(30 º-tilted, 30 keV in $10^{13}$ $cm^{-2}$), respectively. The spike annealing at 925 ºC was used after forming the LDD and halo region. With the side-wall spacer of 365 Å, the source/drain for n-type devices was doped with Ge(16 keV in $10^{14}$ $cm^{-2}$)/P(11- keV in $10^{13}$ $cm^{-2}$)/As(16 keV in $10^{15}$ $cm^{-2}$)/another P(2 keV in $10^{15}$ $cm^{-2}$). The source/drain for p-type devices was doped with Ge(16 keV in $10^{14}$ $cm^{-2}$)/B(3 keV in $10^{15}$ $cm^{-2}$). Those

source/drain regions were spike-annealed at 1025 ºC. Lastly, the bar-type contacts (not like square-shaped contact) were formed onto the source/drain regions.

## IV. CONCLUSION

A simple but efficient matrix model for estimating the WFV in the 28-nm HK/MG MOSFETs has been suggested and compared with experimental data. Even though the computing-expensive and time-consuming MC simulation using a statistically significant number (> ~ $10^6$) of samples is basically appropriate to estimate the WFV, the matrix model for reconfiguring the lucky channel is inexpensive in terms of computing capability and is a quick approach for the WFV-induced $V_{TH}$ variation. The suggested model has been verified using the experimentally obtained $V_{TH}$ distribution in the 28-nm low-power MOSFETs.

## ACKNOWLEDGMENT

This work was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by Ministry of Education, Science and Technology (grant number: 201214011). This work was also supported by IDEC (IC Design Education Center at KAIST).

## REFERENCES

[1] H. F. Dadgour, K. Endo, V. K. De, and K. Banerjee, "Grain-orientation induced work function variation in nanoscale metal-gate transistors—Part I: modeling, analysis, and experimental validation", *IEEE Transactions on Electron Devices,* vol. **57**, no. 10, pp. 2504–2514, October 2010.

[2] H. Nam and C. Shin, "Study of high- κ/metal-gate work-function variation using Rayleigh distribution", *IEEE ELECTRON DEVICE LETTERS*, vol. 34, no. 4, pp. 532-534, April 2013.

[3] C. Shin and I. J. Park, "Impact of using double-patterning versus single-patterning on threshold voltage variation in quasi-planar tri-gate bulk MOSFETs", *IEEE ELECTRON DEVICE LETTERS*, vol. 34, no. 5, pp. 578-580, May 2013.

[4] Sentaurus user guide, ver. E-2010.12.

**Gyo Sub Lee** received the B.S. degree in Electrical and Computer Engineering from the University of Seoul, Korea, in 2013. He is currently pursuing the M.S. degree in the Department of Electrical and Computer Engineering from the University of Seoul, Korea. His interests are the variation analysis in CMOS technology and the yield analysis for SRAM.

**Changhwan Shin** received the B.S. degree (top honors) in Electrical Engineering from Korea University, Seoul, Korea, in 2006 and the Ph.D. degree in Electrical Engineering and Computer Sciences from the University of California, Berkeley, in 2011. In 2011, he joined the Silicon Technology Group, Xilinx Inc., San Jose, CA, as a Senior Process/Device Engineer. In 2012, he joined the Faculty of the University of Seoul, Seoul, Korea. His current research interests include advanced CMOS device designs and their applications to variation-robust SoC memory and logic devices, as well as post-silicon technology such as paper electronics. Prof. Shin was the recipient of a fellowship from the Korea Foundation for Advanced Studies (KFAS) in 2004, the General Electric Foundation Scholar Leaders Award in 2005, the Best Paper Award and the Best Student Paper Award at the IEEE International SOI Conference in 2009, and the Best Paper Award at the European Solid State Device Research Conference (ESSDERC) in 2010. He has been serving on technical committees for the IEEE International SOI conference (now, IEEE S3S conference) and the European Solid State Device Research Conference (ESSDERC) since 2011.