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Analysis of SOHOS Flash Memory with 3-level Charge Pumping Method

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***Abstract*—This paper discusses the 3-level charge pumping (CP) method in planar-type Silicon-Oxide-High-k-Oxide-Silicon (SOHOS) and Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) devices to find out the reason of the degradation of data retention properties. In the CP technique, pulses are applied to the gate of the MOSFET which alternately fill the traps with electrons and holes, thereby causing a recombination current I_{cp} to flow in the substrate. The 3-level charge pumping method may be used to determine not only interface trap densities but also capture cross sections as a function of trap energy. By applying this method, SOHOS device found to have a higher interface trap density than SONOS device. Therefore, degradation of data retention characteristics is attributed to the many interface trap sites.**

***Index Terms*—3-level charge pumping, SOHOS flash memory, interface trap, retention**

I. INTRODUCTION

The silicon–oxide–nitride–oxide–silicon (SONOS) flash memory has recently drawn attention for applications in electrically erasable and programmable read-only memories due to the advantages of lower programming voltage, smaller cell size, and better endurance characteristics for memory operation. In addition, the SONOS device is also one of the most promising candidates to realize the continuous vertical scaling on Flash memory through the mechanism of charge trapping in its structure [1, 2]. Since the SONOS device stores charge in the spatially isolated deep-level traps, a single defect in the tunnel oxide will not cause the discharge of the memory cell [3, 4]. For lower voltage operation and further scaling down of memory devices in SONOS structures, decreasing of oxide-nitride-oxide thickness is inevitable. But, the thinning of the oxides and the silicon nitride brings about the charge leakage and decrease of maximum threshold voltage shifts. It has been reported that the linear relationship of the maximum threshold voltage shifts exhibits due to the constants of trapped-electron densities at the top and bottom interface [5]. Recently, SONOS structures with high-k trapping layers being capable of the scaling down were proposed to reduce the operation voltage of program/erase and to maintain the better data retention properties [6]. But, SOHOS devices have the poorer data retention capability than SONOS devices. The optimal compositions in the HfO_2 charge trapping layer and the relevant physical mechanisms still remain unclear and thus are worth further exploring [7]. That is, to find out the reason of degradation of data retention characteristics in SOHOS device, we carried out 3-level charge pumping method analysis which is a powerful tool to get the exact interface trap density.

II. EXPERIMENTAL

The fabrication details are shown in Fig. 1(a). P-type

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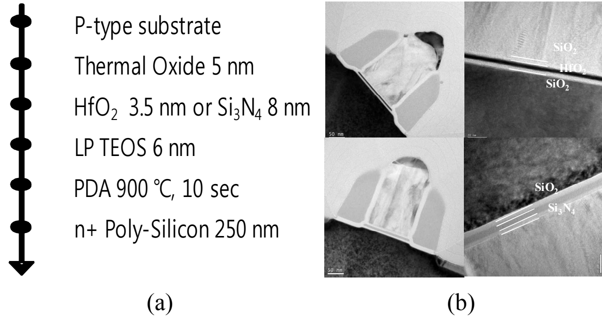

Fig. 1. (a) Process flow, (b) Cross-sectional TEM images of flash memory structure.

(100) bulk substrates are used as starting materials for a triple dielectric stack structure. The tunneling oxide of 5-nm is thermally grown, and the HfO_2 of 3.5-nm is deposited by an atomic layer deposition (ALD) using tetrakis (ethylmethylamino)hafnium (TEMAHf) precursor and ozone at 350°C, the control oxide of 6-nm is deposited by low-pressure chemical vapor deposition (LPCVD), and post deposition anneal (PDA) is performed at 900°C, 10sec. The gate length is 0.5μm. Then, n-doped source and drain junctions are formed, followed by transistor source/drain annealing at 1000°C in nitrogen ambient for 10sec, and the conventional back-end of line process such as drain contact and signal metal line are progressed. Fig. 1(b) shows the transmission electron microscopy (TEM) images of the cross section of the fabricated devices and a good interface layer between SiO_2 and HfO_2. The major electrical characteristics including 3-level charge pumping method of the devices were measured using a semiconductor parameter analyzer (HP4156C), pulse generator (Agilent81104A).

III. Results and Discussions

Fig. 2 shows the representative transfer characteristics of fabricated SONOS and SOHOS devices with structure of planar-type flash memory. The constant current method is used for threshold voltage (V_{TH}) extraction, where V_{TH} is defined as the bias of gate voltage that forces drain current to $(W/L) \times 100nA$ at $V_D = 0.05V$. Expect that HfO_2 device has lower V_{TH} due to smaller equivalent oxide thickness (EOT), both devices have similar electrical performance.

The device with HfO_2 trapping layer is expected to

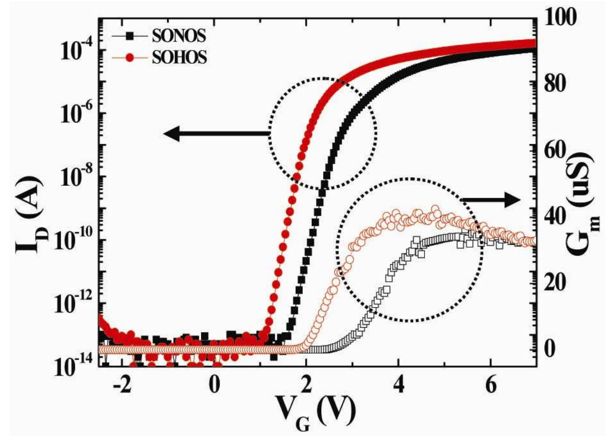

Fig. 2. V_{GS}-I_{DS} characteristic of planar type flash memory device.

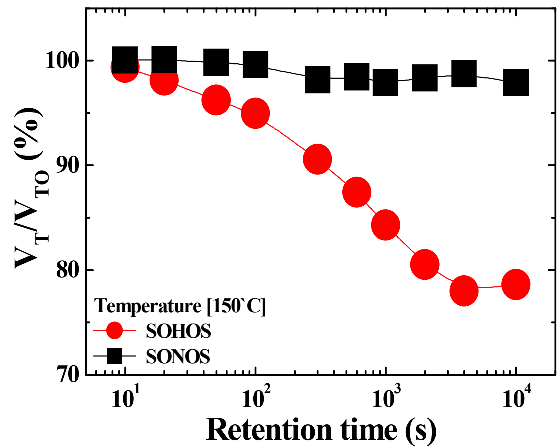

Fig. 3. Date Retention characteristic of planar type flash memory device.

show better data retention characteristics than that with Si_3N_4 trapping layer, because HfO_2 material has larger conduction band offset than Si_3N_4 material. However, threshold voltage (V_{TH}) of SOHOS device decreased about 23 percent as shown in Fig. 3.

SIMS analysis was further performed in order to verify the chemical composition of the stack. HfO_2 diffusion into SiO_2 takes place. It has been reported that the HfO_2 interface has a high interface trap density [8]. HfO_2 diffused into SiO_2/Si interface leads to an important source defects in the gate oxide stack.

Afterwards, we carried out 3-level charge pumping analysis to find out the definite reason for degradation of retention properties in SOHOS device. Fig. 5(a) shows bias levels above inversion voltage (V_{INV}) and below

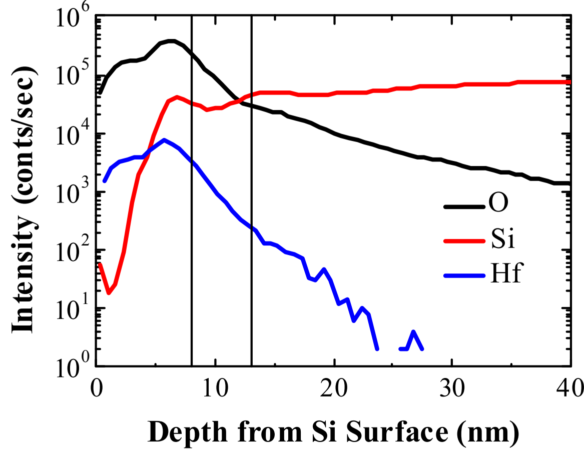

Fig. 4. SIMS depth profile of Hafnium diffusion into the tunnel oxide.

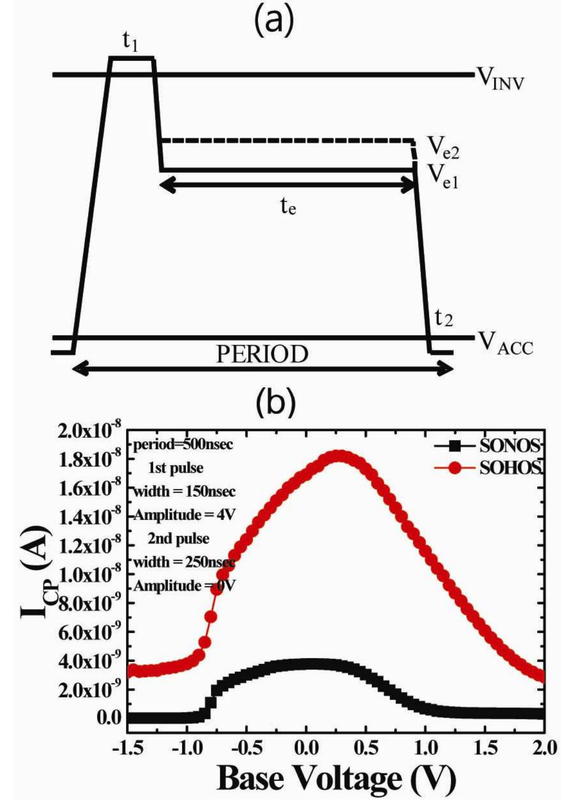

Fig. 5. (a) The three-level CP pulse, (b) Charge pumping current of SONOS and SOHOS device.

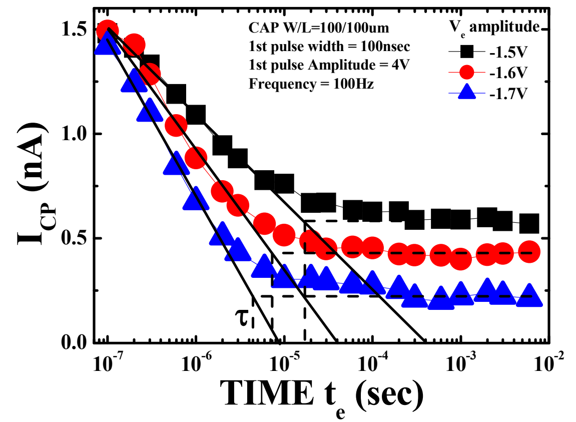

Fig. 6. I_{cp} as a function of t_e for electron emission, with pulse bias V_e as a parameter.

accumulation voltage (V_{ACC}) are used as in standard charge pumping [9]. Using 3-level CP, the 2nd pulse duration (t_e) and 2nd pulse voltage (V_e) of the 3-level are varied to determine trap parameters. And Fig. 5(b) shows SOHOS device has much higher charge pumping current than SONOS device. It is shown that strong electron trapping is observed with SOHOS device.

The test devices are MOS capacitors with 100-μm gate length, 100-μm width. The 3-level pulse used here is identical to that of Tseung but with both V_e variable. The pulse is applied to the gate and I_{cp} is measured at the substrate [9]. A 100-Hz pulse with 20-ns rise and fall times was used to explore a wide range of trap time constants. Experimental I_{cp} data obtained as a function of t_e for different values of V_e are shown in Fig. 5(a). At small t_e, I_{cp} decrease approximately as ln (t_e). This behavior is expected since [9, 10]

$$D_{it}(E_t) = -\frac{1}{qkTfA}\frac{dI_{cp}}{dln(t_e)}\left[1+\frac{kT}{\sigma}\frac{d\sigma}{dE_t}\right] \quad (1)$$

where, k is Boltzman's constant and T is the absolute temperature. If is independent of E_t, this reduces to Eq. (2).

$$D_{it}(E_t) = -\frac{1}{qkTfA}\frac{dI_{cp}}{dln(t_e)} \quad (2)$$

As discussed above, when t_e is long, the traps above the Fermi level determined by V_e emit their electrons. Therefore, the traps reach equilibrium, and I_{cp} saturates at long times, as observed in Fig. 6. This clean saturation characteristic indicates that the trap levels are associated with a single emission time and thus each is characterized by a single value of D_{it} which may then be determined using Tseung's method [10] from the variation of saturated I_{cp} with V_e.

The distributions of interface trap density D_{it} (E_t) extracted from 3-level CP measurements are shown in

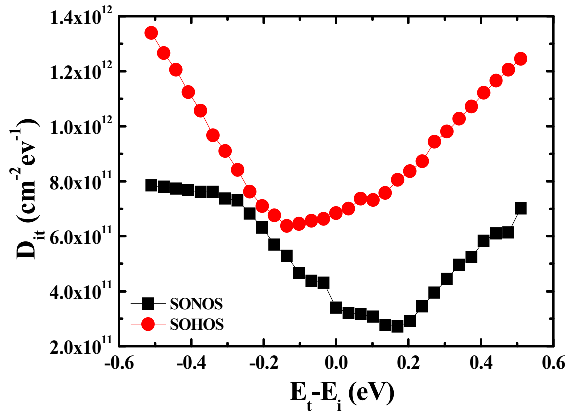

Fig. 7. Interface-trap density $D_{it}(E_t)$ as a function of band gap energy.

Fig. 7. In both devices, $D_{it}(E_t)$ are smallest in the middle of the gap and increases near the band edges. However, it is noticeable that SOHOS devices have higher interface trap density than SONOS device, with less asymmetric energy profile throughout the Si band gap.

The time constant for electron capture is given by

$$\tau_e = \frac{1}{V_{th} \times \sigma_e \times n_i} \quad (3)$$

where Vth is the electron thermal velocity, ni is the intrinsic carrier density, and σe is the capture cross section. For a 100 kHz symmetrical square gate pulse, we have τ = 10us and the capture cross section is extracted to be 2.43 x 10^{-16} for SOHOS with Vth = 1 x 10^7 cm/s and ni = 1 x 10^{14} cm^{-3}.

V. CONCLUSIONS

This paper discusses the reason of poor reliability in planar-type SOHOS devices compared with SONOS devices. We have studied the interface trap density of planar-type SOHOS devices and its energy profile through 3-level charge pumping method. SOHOS devices have a higher interface trap density than SONOS devices. Therefore, the degradation of data retention characteristics is attributed to many interface trap sites.

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