TRANSACTIONS ON ELECTRICAL AND ELECTRONIC MATERIALS
Vol. 15, No. 1, pp. 16-19, February 25, 2014

Regular Paper

pISSN: 1229-7607 eISSN: 2092-7592
DOI: http://dx.doi.org/10.4313/TEEM.2014.15.1.16

Improved Memory Characteristics by NH_3 Post Annealing for ZrO_2 Based Charge Trapping Nonvolatile Memory

Zhenjie Tang† and Dongqiu Zhao
College of Physics and Electronic Engineering, Anyang Normal University, Anyang 455000, China

Rong Li
School of Mathematics and Statistics, Anyang Normal University, Anyang 455000, China

Xinhua Zhu
National Laboratory of Solid State Microstructures, Nanjing University, Nanjing 210093, China

Received December 4, 2012; Revised December 20, 2013; Accepted December 28, 2013

Charge trapping nonvolatile memory capacitors with ZrO_2 as charge trapping layer were fabricated, and the effects of post annealing atmosphere (NH_3 and N_2) on their memory storage characteristics were investigated. It was found that the memory windows were improved, after annealing treatment. The memory capacitor after NH_3 annealing treatment exhibited the best electrical characteristics, with a 6.8 V memory window, a lower charge loss ~22.3% up to ten years, even at 150℃, and excellent endurance (1.5% memory window degradation). The results are attributed to deep level bulk charge traps, induced by using NH_3 annealing.

Keywords: Charge trapping, NH_3 annealing, Memory capacitors

1. INTRODUCTION

With the feature size of conventional floating gate type nonvolatile semiconductor memory (NVSM) approaching to its scaling limitation, tremendous effort has been made to explore low-cost, high-density, and nonvolatile solid state memory devices, for use in mobile electronics, such as digital cameras, mobile phones, and MP3 players [1]. Based on the concept that charges are stored in discrete traps within the charge trapping layer, polysilicon-oxide-nitride-oxide-silicon (SONOS) charge trapping flash memories with nitride (Si_3N_4) [2] as the charge trapping layer has attracted much attention, for commercial applications to replace the conventional FG-NVSM. However, using Si_3N_4 charge trapping layer in a SONOS structure leads to poor retention, due to the shallow traps, and the small conduction band offset at the Si_3N_4/tunneling layer interface [3]. Employing high-k dielectrics as the charge trapping layer to improve memory characteristics in SONOS structure has been reported by many researchers [4-9]. The high-k charge trapping layer allows a higher electric field cross the tunneling layer, due to electric flux density continuity [3], and results in a modified Fowler-Nordheim tunneling, due to the smaller conduction band offset (CBO) with a Si substrate [10]. However, pure high-k dielectrics as charge trapping layer, such as HfO_2 and ZrO_2, have poor retention characteristics, due to the presence of conduction paths in the high-k material [11]. In this paper, we report the improved memory characteristics, by NH_3 annealing ZrO_2 based charge trapping memory.

† Author to whom all correspondence should be addressed:
E-mail: zjtang@hotmail.com

2. EXPERIMENTS

The P-type Si (100) substrates were cleaned by the standard Radio Corporation of America (RCA) process to remove native oxide. Then, a 4 nm SiO_2 was thermally grown in dry O_2 at 900℃, as the tunneling layer (TL). After that, the ZrO_2 charge trapping layer (CTL) with a thickness of ~6 nm was deposited by pulse laser deposition (PLD), at a substrate temperature of 350℃ (a KrF excimer laser operating at 1-5 Hz was used for ablation; the laser fluence was around 1.8 J/cm^{-2}; the deposition was performed under oxygen pressure of 1×10^{-4} Pa, and the growth rate per laser shot was approximately 0.1 nm). Subsequently, a ~8 nm Al_2O_3 film as blocking layer (BL) was deposited by atomic layer deposition (ALD), using tri-methylaluminium ($Al(CH_3)_3$) precursors, at a substrate temperature of 300℃. During this process, O_3 was used as oxygen source. The fabricated memory capacitor without post-annealing is denoted as Z1. After the above processes, the memory capacitors were rapid thermal annealed (RTA) at 900℃ for 60s in N_2 and NH_3 atmosphere, denoted as Z2 and Z3, respectively. Finally, platinum (Pt) top electrodes with an area of cm^2 were deposited on the films, by using magnetron sputtering technique, at room temperature. Ag silver paste was spread on the back side of Si substrate, as the bottom electrodes. The interfacial structure of the memory capacitors was revealed by cross-sectional high-resolution transmission electron microscopy (HRTEM) images. To prepare the cross sectional sample of the memory structure for HRTEM, a standard technique was used, which including gluing two deposited structures, cutting, grinding, polishing, and thinning, via room temperature argon milling procedures. X-ray diffraction (XRD) was employed, to investigate the crystalline structure of ZrO_2 films. The electrical characteristics of the memory capacitors were measured using a Keithely 4200 semiconductor characterization system (4200 SCS), in dc sweeping mode and pulse mode.

3. RESULTS AND DISCUSSION

The XRD patterns of as-deposited and annealed ZrO_2 films are presented in Fig. 1. It is observed that as-deposited ZrO_2 films remain amorphous, while some crystalline peaks appeared after RTA at 900℃ in N_2 and NH_3 atmosphere, and the diffraction peaks are of tetragonal ZrO_2 phase. The selected area electron diffraction (SAED) pattern of the NH_3 annealed ZrO_2 film is shown in the inset of Fig. 1. The Polycrystalline diffraction rings correspond to the (111), (002), (202) and (113) planes of the tetragonal ZrO_2 phase, respectively.

The cross-section and interface quality of the NH_3 annealed memory capacitor was examined by HRTEM, as shown in Fig. 2. It can be seen that the thicknesses of TL, CTL and BL are 4 nm, 6 nm and 8 nm, respectively, and the interfaces are clear. The insets exhibit fast Fourier transform (FFT) analyses of selected areas, which reveal the crystallization characteristics. It is observed that the ZrO_2 charge trapping layer crystallizes, after post-annealing treatment. Meanwhile, Al_2O_3 films as blocking oxide still keep their amorphous structure.

Figure 3 illustrates the data retention characteristics of memory capacitors at 25℃, and 150℃. The charge loss was 11.6%, 5.7% and 4% up to 4×104s, for the three samples at 25℃, respectively. In order to predict the charge retention characteristics for a long time, according to the changing trend of the last three experimental data, we extrapolated the last two data, and supposed that the trend of charge loss fits a linear relation with the logarithm of retention time, up to ten years [6,9]. The extrapolation of the experimental results shows that the charge losses after ten years were 41.2%, 18% and 12.8%, respectively, suggesting that the NH_3 and N_2 annealing treatment could reduce the charge loss. The Z3 sample obtained optimum retention performance, which could be ascribed to the generation of deep level bulk charge traps, and reduced shallow level and interfacial traps in CTL [12]. These deep level traps are more immune to tunneling

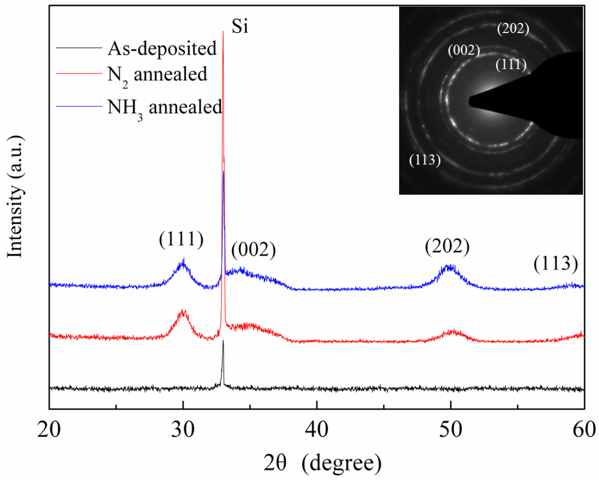

Fig. 1. XRD patterns of as-deposited and 900℃ annealed ZrO_2 films. The inset is the selected area electron diffraction pattern of NH_3 annealed ZrO_2 films.

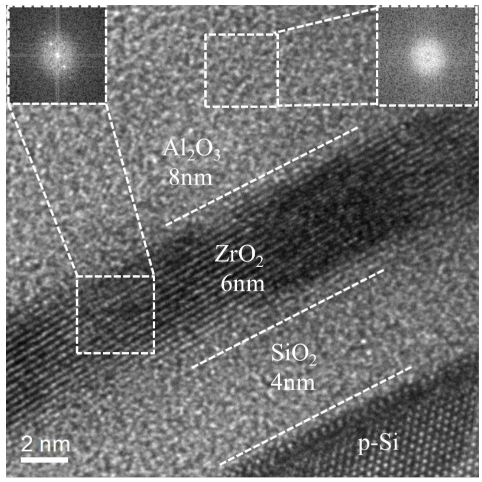

Fig. 2. High resolution transmission electron microscopy (HRTEM) of NH_3 annealed p-Si/SiO_2/ZrO_2/Al_2O_3 memory structure. The insets exhibit FFT analyses of selected areas.

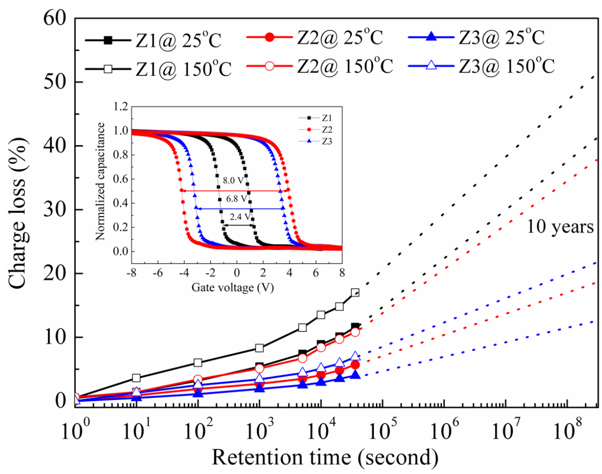

Fig. 3. Retention characteristics of the memory capacitors. The inset is high frequency (1MHz) C-V curves of the memory capacitors with identical sweeping gate voltage (±8 V).

of electrons back to the substrate. For the three samples, it was observed that the charge losses after ten years at 150℃ can be determined to be 52.3%, 37.5% and 22.3%, respectively, by extrapolating the experimentally measured charge loss curve. It is well know that the charge loss mechanisms are composed of two categories. The first one, including electrons tunneling from trap to band, electron trap to trap tunneling, and holes band to trap tunneling, is not temperature sensitive. The second category, coming from thermal excitation, is temperature dependent. Trap to band tunneling and thermal excitation are the dominant charge loss mechanisms, and jointly contribute to charge loss for memory devices [13-16]. In our case, the charge loss increased with increase of temperature resulting from thermal excitation, and more electrons were discharged via thermal excitation into the conduction band of the charge trapping layer, then tunneled back to the silicon substrate. The best retention characteristics of the Z3 sample at 150℃ should be attributed to the generated deep level bulk traps, which could effectively resist the thermal excitation. The inset shows high frequency (1MHz) C-V hysteresis memory windows of the memory capacitors, measured with identical sweeping gate voltage (±8 V). For the three samples, the hysteresis memory windows were measured to be 2.4 V, 6.8 V and 8.0 V, respectively. These results should be attributed to the increase of charge traps near the TL/ CTL interface, and bulk of CTL, after post annealing treatment. Compared with Z1 and Z3 samples, Z2 sample obtaining the largest memory window results, from generating more interfacial traps and oxygen vacancies between the TL/CTL interface [17]. Compared with N_2 annealing, although NH_3 annealing generates less traps, a lot of the traps are deep level bulk traps, which are the dominant factor of the retention characteristics, especially at high temperature.

Figure 4 shows the leakage current density-voltage (J-V), for Z1, Z2 and Z3 samples. It is observed that the leakage current is lower for Z2 and Z3, compared to Z1, suggesting that the post annealing in NH_3 or N_2 atmosphere could effectively improve the interface quality, and reduce the interfacial defects of TL/CTL, since the undesired interface traps can be effectively suppressed, since the nitrogen bl℃ked the atomic diffusion, and reduced the growth of the interfacial layer for Z3, by the NH_3 annealing [18]. The results indicated that NH_3 annealing treatment is a more effective method to improve the electrical performance, compared to N_2 annealing.

Figure 5 is the endurance performance of the three memory capacitors, and the program (solid symbols)/erase (open symbols) conditions were +8 V for 1 ms and -8 V for 1 ms, respectively. For the three memory capacitors, the memory window is degraded by 37%, 5% and 1.5% after 105 P/E cycles, respectively. For Z1 sample, the narrowest memory window resulted from the oxide traps and interface state generation at different locations depending on bias conditions, due to the memory structure being stressed for a long time [19]. On the other hand, the slight degradation of the memory window for Z2 and Z3 samples should be ascribed to producing stronger chemical bonds at the TL/CTL interface, and the interfacial quality and structure being improved after NH_3 or N_2 annealing treatment.

4. CONCLUSIONS

$Pt/Al_2O_3/ZrO_2/SiO_2/Si$ memory capacitors have been prepared, and the effects of annealing atmosphere (N_2 and NH_3) on the memory characteristics have been investigated. It was found that the memory windows were improved, after annealing treatment. Excellent endurance and retention characteristics, even at 150℃, have been achieved, by using NH_3 annealing. The results are attributed to deep level bulk charge traps, induced by using NH_3 annealing. It looks like the NH_3 annealed memory capacitor will be a potential candidate, in future nonvolatile flash memory device application.

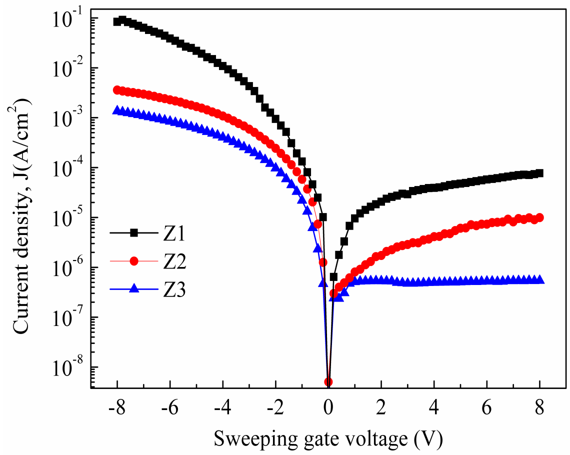

Fig. 4. Leakage current density-voltage (J-V) characteristics for Z1, Z2 and Z3 samples, respectively.

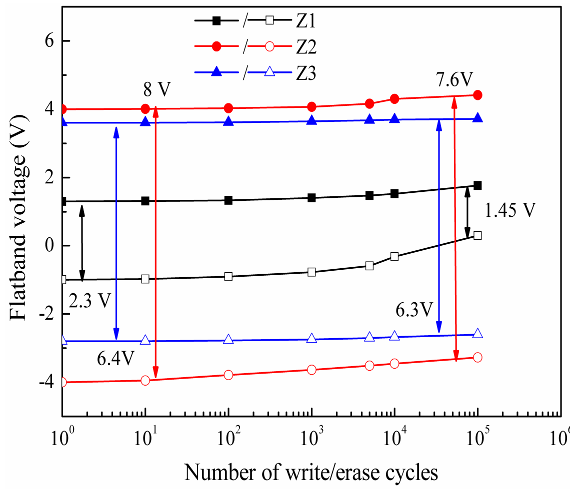

Fig. 5. Endurance performance of the memory capacitors.

ACKNOWLEDGMENTS

This work was financially supported by National Natural Science Foundation of China (Grant Nos. 11247318), the Science and Technology Research Key Project in the Henan Province Department of Education (Grant No. 13A140021), the Science and Technology Research Key Project in Henan Province Department of Education (Grant No. 14A140008), the National Natural Science Foundation of China (Grants No.11134004, 11174122 and 61176124), and the State Key Program for Basic Research of China (Grant No.2010CB934201).

REFERENCES

[1] S. H. Lee, Y. Jung, R. Agarwal, Nat. Nanotechnol. 2, 626 (2007) [DOI: http://dx.doi.org/10.1038/nnano.2007.291].

[2] J. K. Bu and M. H. White, Solid State electron. 45, 113 (2001) [DOI: http://dx.doi.org/10.1016/S0038-1101(00)00232-X].

[3] G. Zhang, X. P. Wang, W. J. Yoo, M. F. Li, IEEE Trans Electron Devices. 54, 3317 (2007) [DOI: http://dx.doi.org/10.1109/TED.2007.908888].

[4] Z. J. Tang, H. N. Xu, H. T. Li, C. Yan, Y. D. Xia, J. Yin, X. H. Zhu, Z. G. Liu, A. D. Li, and F. Yan, Microelectron. Eng. 88, 3227 (2011) [DOI: http://dx.doi.org/10.1016/j.mee.2011.06.025].

[5] J. H. Kim, J.B. Choi, IEEE Trans. Electron Devices. 51, 2048 (2004) [DOI: http://dx.doi.org/10.1109/TED.2004.838446].

[6] Z. J. Tang, Y. D. Xia, H. N. Xu, J. Yin, Z. G. Liu, A. D. Li, X. J. Liu, Y. Feng and X. L. Ji, Electrochem Solid State Lett. 14, G13 (2011) [DOI: http://dx.doi.org/10.1149/1.3518706].

[7] X. Zhu, Y. Yang, Q. Li, D. E. Ioannou, J. S. Suehle, C. A. Richter, Microelectron. Eng. 85, 2403 (2008) [10.1016/j.mee.2008.09.013]

[8] Z. J.Tang, X. H. Zhu, H. N. Xu, Y. D. Xia, J. Yin, Z. G. Liu, A. D. Li and F. Yan, Materials Letters, 92, 21 (2013) [DOI: http://dx.doi.org/10.1016/j.matlet.2012.10.024].

[9] Y. Zhou, J. Yin, H. N. Xu, Y. D. Xia, Z. G. Liu, A. D. Li, Y. P. Gong, L. Pu, F. Yan and Y. Shi, Appl. Phys. Lett. 97, 143504 (2010) [DOI: http://dx.doi.org/10.1063/1.3496437].

[10] Y. N. Tan, W. K. Chim. W. K. Choi, M. S. Joo and B. J. Cho, IEEE Trans. Electron Devices. 53, 654 (2006) [DOI: http://dx.doi.org/10.1109/TED.2006.870273].

[11] M. S. Joo, B. J. Cho, C. C. Yeo, D. S. H. Chan, S. J. Whoang, S. Matthew, L. K. Bera, N. Bala and D. L. Kwong, IEEE Trans. Electron Devices, 50, 2088 (2003) [DOI: http://dx.doi.org/10.1109/TED.2003.816920].

[12] L. Liu, J. P. Xu, F. Ji, J. X. Chen, and P. T. Lai, Appl. Phys. Lett. 101, 033501 (2012) [DOI: http://dx.doi.org/10.1063/1.4737158].

[13] A Roy. and M. H. White, Solid-State Electronics. 34, 1083 (1991) [DOI: http://dx.doi.org/10.1016/0038-1101(91)90104-7].

[14] Y. Hu and M. H. White, Solid State Electronics. 36, 1401 (1993) [DOI: http://dx.doi.org/10.1016/0038-1101(91)90036-X].

[15] S. J. Wrazien, Y. Zhao, J. D. Krayer and White M. H, Solid State Electronics. 47, 885 (2003) [DOI: http://dx.doi.org/10.1016/S0038-1101(02)00448-3].

[16] Y. Yang, M. H. White, Solid State Electronics. 44, 949 (2000) [10.1016/S0038-1101(00)00012-5].

[17] L. G. Gao, K. B. Yin, Y. D. Xia, L. Chen, H. X. Guo, L. Shi, J. Yin and Z. G. Liu, J Phys D Appl Phys. 42, 015306 (2009) [DOI: http://dx.doi.org/10.1088/0022-3727/42/1/015306].

[18] C. S. Lai, K. M. Fan, H. K. Peng, S. J. Lin, C. Y. Lee and C. F. Ai, Appl. Phys. Lett. 90, 172904 (2007) [DOI: http://dx.doi.org/10.1063/1.2975183].

[19] S. Yamada, Y. Hiura, T. Yamane, K. Amemiya, Y. Oshima, and K. Yoshikawa, IEDM Tech. Dig., 23 (1993) [DOI: http://dx.doi.org/10.1109/IEDM.1993.347407].