

Analytical Surface Potential Model with TCAD Simulation Verification for Evaluation of Surrounding Gate TFET

T.S.Arun Samuel[†], N.B.Balamurugan*, T.Niranjana* and B.Samyuktha*

Abstract – In this paper, a new two dimensional (2D) analytical modeling and simulation for a surrounding gate tunnel field effect transistor (TFET) is proposed. The Parabolic approximation technique is used to solve the 2-D Poisson equation with suitable boundary conditions and analytical expressions for surface potential and electric field are derived. This electric field distribution is further used to calculate the tunneling generation rate and thus we numerically extract the tunneling current. The results show a significant improvement in on-current characteristics while short channel effects are greatly reduced. Effectiveness of the proposed model has been confirmed by comparing the analytical results with the TCAD simulation results.

Keywords: Surrounding gate TFET, Surface potential, Electric field distribution.

1. Introduction

The primary challenges faced in scaling a complementary metal oxide semiconductor (CMOS) device are to ensure the increased functionality per unit cost and improvement in the performance of device. The Surrounding Gate MOSFETs is considered one of the most promising devices for down scaling below 100nm [1, 2]. By surrounding the channel completely, the gate gains increased the electrostatic control of the channel and short channel effects can be drastically suppressed [3]. Apart from the benefit of allowing a shorter channel, the SG MOSFETs can achieve a higher packing density due to their enhanced current drive compared to planar MOSFETs. However, even in SG MOSFET devices, Short channel effects (SCE) such as the threshold voltage roll-off, leakage current and the subthreshold swing degradation, cannot be neglected for channel lengths in nano meter regime. Hence, several new devices are being proposed to keep up the scaling law proposed by Gordon Moore, and among them, Tunnel field-effect transistor has been considered as a best alternative device in the standard CMOS for low power applications. Due to the built-in tunnel barrier, the TFET device suffers less short channel effects, in comparison with the conventional planar MOSFET devices. TFETs show a very small leakage current in the range of femto amperes (fA) [4], when the device is turned off. Also TFET offers much smaller V_t roll-off while scaling because threshold voltage depends on the band bending in small tunnel region, but not the whole

channel region.

In spite of these merits, one factor that deters the performance of a TFET is its low ON-current (I_{ON}). Hence a various number of methods are proposed to improve the I_{ON} of TFETs.

In order to enhance the ON current (I_{ON}), various design improvements in terms of band gap engineering [5], hetero junction TFETs [6] strained silicon [7], novel architectures like carbon nanotube TFETs [8], double gate (DG) TFET [9], Dual material gate (DMG) TFET [10] and DMG DGTFTs [11] have been proposed. Sandow et al., [12] proposed experimental studies on the performance of ultra-thin body SOI tunnel FETs depending on channel length, gate oxide thickness and source/drain doping concentrations. By reducing the gate oxide thickness from 4.5 nm to 3.5 nm leads to increase the maximum saturation current by a factor of 6. Kathy Boucart [9] proposed a novel design for a DG TFET, which is made up of high-K gate dielectric offers an ON-current as high as 0.23 mA for a gate voltage of 1.8 V, an OFF-current of less than 1 fA and the subthreshold swing of 57 mV/dec. However the ON current of the DG TFET is still to be improved. Sneha Saurabh [11] proposed a new DMDG TFET, incorporating with DMG structure and DG structure. This device offers excellent device performance like increased ON current, reduced OFF current, improved subthreshold slop and immunity against DIBL effects. However the device performances have been analyzed using 2-D device simulator ATLAS and I_{ON} current not reached the level of CMOS technology. Moreover they have discussed only drain current characteristics by varying the dual metal work functions.

The above models deal only with simulation and only a few analytical models were proposed. There are many methods to model the device analytically and to calculate the Surface potential, Electric field and drain current. It

[†] Corresponding Author: Dept. of Electronics and Communication Engineering, Thiagarajar College of Engineering, Madurai, India. (arunsamuel@tce.edu)

* Dept. of Electronics and Communication Engineering, Thiagarajar College of Engineering, Madurai, India. (nbbalamurugan@tce.edu, {niranjana, thangapandi, samyukthabalachandran}@gmail.com)

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includes superposition method, Green function method, parabolic approximation method, Fourier series expansion method and numerical methods. Lee [13] proposed a model for potential and electric field for Single material Gate TFET using superposition technique. Despite of the accuracy of above models, it involves a lot of mathematical complexity and makes its understanding difficult.

Vandenberghe et al [14] suggested that there are two different types of tunneling current happening in two locations in the TFET device, such as point tunneling and line tunneling. They developed a simple analytical model for these two different types of tunneling currents in the TFET using Kane's model. However, this model determines the tunnel current of a single-gate TFET, but there is no straightforward extension of the model to other gate configurations. Verhulst et al., [15] developed a new modeling framework, starting from the Vandenberghe [14] work and making a simplification, such that a direct comparison between a single-gate, double-gate, and gate-all-around (GAA) configuration can be made. This work also gives insight in the impact of the choice of tunnel path in two- or three-dimensional TFET configurations. However the effect of drain bias is not included to this model. Bardon [16] proposed potential and electric field model for a Double Gate TFET using pseudo 2-D solution. 1-D poisson's equation based modeling of TFET has been proposed by Verhulst [17].

In this paper, we propose a Surrounding gate TFET structure which enhances the I_{ON} current during device operation. The aim of this work is, to study the potential benefits offered by the Surrounding Gate TFET by using parabolic approximation technique for the first time, which is simple and accurate. The analytical model is developed using two dimensional solution of Poisson equation. This model is used to calculate the surface potential and electric field distribution in the device and the drain current I_{DS} is derived from the electric field using Kane's model. This paper is organized as follows: Section 2 shows model derivation of this work. The result and discussions are analyzed in Section 3 and Section 4 contains a summary of the conclusions.

2. Model Derivation

The cross section view of a Surrounding gate TFET is shown in Fig. 1. The coordinate system consists of a radial direction r , a vertical direction z , and an angular component θ in the plane of the radial direction. The source and drain is made of highly doped p-type and n-type regions respectively. The intermediate channel region is made of a moderately doped n-type layer. Silicon-di-oxide (SiO_2) is used as the gate dielectric. Based on the positive or negative potential applied to the gate terminal, the device behaves as n type TFET and p type TFET respectively. If a positive gate voltage is applied, the

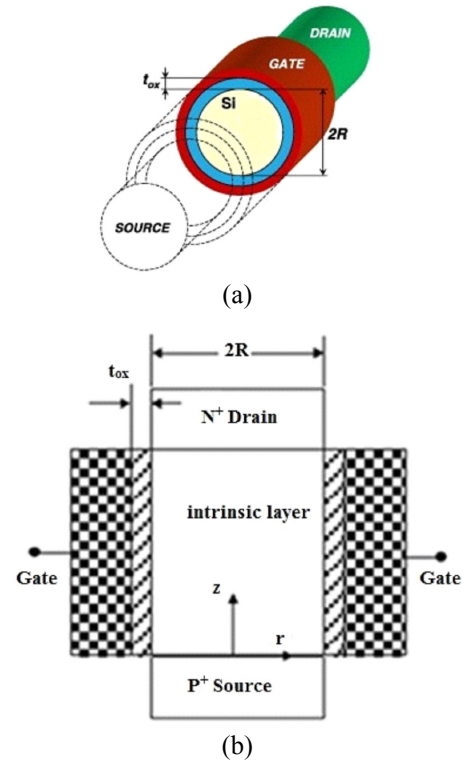


Fig. 1. Surrounding gate TFETs: (a) Schematic diagram; (b) Cross sectional diagram.

Table 1. Process parameters for simulated surrounding gate TFET

Quantities	Symbol	value
Doping of source	N_A	10^{20}cm^{-3}
Doping of drain	N_D	10^{20}cm^{-3}
Metal work function	ϕ_m	4.5eV
Oxide thickness	t_{OX}	2nm
Silicon body thickness	R	10nm
Channel length	L	20nm

transistor behaves as a n-TFET and a negative gate voltage is applied, the transistor behaves as a p-TFET. The device physical parameters are summarized in Table 1. Increasing the positive voltage on the gate narrows the energy barrier between the source and intrinsic region. Then electrons tunnel from the valence band of the p-doped source to the conduction band in the intrinsic body and then move toward the n-doped drain by drift diffusion.

2.1 Surface potential

For the simplicity of derivation, it has been assumed that the TFET is operated in the subthreshold region where mobile carriers are negligible and that source-channel and drain-channel junctions are abrupt. No depletion in the source and drain region has been assumed. To obtain potential distribution throughout the device and the channel potential at the SiO_2 -Si interface, the 2-D Poisson's/Laplace Equation used is given as:

$$\frac{1}{r} \frac{\partial}{\partial r} \left(r \frac{\partial \varphi(r, z)}{\partial r} \right) + \frac{\partial^2 \varphi(r, z)}{\partial z^2} = 0 \quad (1)$$

To solve the 2-D Poisson's Equation for n channel surrounding gate TFET, the parabolic approximation approach is employed. The parabolic approach is applied to estimate the potential distribution over the 2-D space (along the device length and device depth) and the potential solution is given as:

$$\varphi(r, z) = C_0(z) + C_1(z)r + C_2(z)r^2 \quad (2)$$

Where the arbitrary constants $C_0(z)$, $C_1(z)$ and $C_2(z)$ are functions of z only.

The boundary conditions required for the solution of Eq. (1) are,

(a) The surface potential $\varphi_s(z)$ is a function of z only.

$$\varphi(R, z) = \varphi_s(z) \quad (3)$$

(b) The electric field in the center of the silicon pillar is zero.

$$\left. \frac{\partial \varphi(r, z)}{\partial r} \right|_{r=0} = 0 \quad (4)$$

(c) The electric field at the silicon / oxide interface is continuous.

$$\left. \frac{\partial \varphi(r, z)}{\partial r} \right|_{r=R} = \frac{\epsilon_{ox}}{\epsilon_{si} R} \left(\frac{\psi_G - \varphi_s(z)}{\ln \left(1 + \frac{t_{ox}}{R} \right)} \right) \quad (5)$$

Here $C_f = R \ln \left(1 + \frac{t_{ox}}{R} \right)$

(d) The potential at the source end is

$$\varphi(0, 0) = \varphi_s(0) = V_{bi} \quad (6)$$

(e) The potential at the drain end is

$$\varphi(r, L) = \varphi_s(L) = V_{bi} + V_{ds} \quad (7)$$

Where V_{bi} is the built in potential. $V_{bi} = \frac{KT}{q} \ln \left(\frac{N_A N_D}{n_i} \right)$

E_G is Band gap energy, q is elementary charge, V_{GS} is Gate to Source voltage, V_{DS} is Drain to Source voltage, ϵ_{si} is relative permittivity of silicon and ϵ_{ox} is relative permittivity of silicon dioxide.

Applying all the boundary conditions to Eq. (2), the

coefficients $C_0(z)$, $C_1(z)$ and $C_2(z)$ can be rewritten as functions of surface potential $\varphi_s(z)$, i.e.,

$$C_0(z) = \varphi_s(z) - \frac{R C_f}{2 \epsilon_{si}} (\psi_G - \varphi_s(z)) \quad (8)$$

$$C_1(z) = 0 \quad (9)$$

$$C_2(z) = \frac{1}{2R} \frac{C_f}{\epsilon_{si}} (\psi_G - \varphi_s(z)) \quad (10)$$

Substituting the Eq. (8-10) in (2), we get

$$\varphi(r, z) = \varphi_s(z) - \frac{R C_f}{2 \epsilon_{si}} (\psi_G - \varphi_s(z)) + \frac{1}{2R} \frac{C_f}{\epsilon_{si}} (\psi_G - \varphi_s(z)) r^2 \quad (11)$$

The surface Potential $\varphi_s(z)$ can be obtained by solving the Poisson's Eq. (1) using (11).

$$\frac{d^2 \varphi_s(z)}{dz^2} - K^2 \varphi_s(z) = -K^2 \psi_G \quad (12)$$

Where,

$$K^2 = \frac{2C_f}{R \epsilon_{si}}$$

$$\psi_G = V_{GS} - \varphi_m + \chi + \frac{E_g}{2}$$

By solving the second-order differential Eqs. (12), we get,

$$\varphi_s(z) = A e^{Kz} + B e^{-Kz} + \psi_G \quad (13)$$

χ is the electron affinity. λ is the characteristics length. This natural length is an easy guide for choosing device parameters.

The coefficients of A and B can be expressed as,

$$A = V_{bi} - \psi_G - \frac{\left\{ e^{LK} V_{biS} - (V_{biD} + V_{DS}) \right\} - \left\{ e^{LK/2} \psi_G \left(2j \sinh \left(\frac{LK}{2} \right) \right) \right\}}{2j \sinh(LK)} \quad (14)$$

$$B = \frac{\left\{ e^{LK} V_{biS} - (V_{biD} + V_{DS}) \right\} - \left\{ e^{LK/2} \psi_G \left(2j \sinh \left(\frac{LK}{2} \right) \right) \right\}}{2j \sinh(LK)} \quad (15)$$

2.2 Electric field

The electric-field distribution along the channel length

can be obtained by differentiating the surface potential. The lateral electric field can be written as,

$$E_z = -\frac{\partial\phi(r, z)}{\partial z} = \frac{\partial\phi_s(z)}{\partial z} = K(Ae^{Kz} - Be^{-Kz}) \quad (16)$$

The vertical electric field can be written as,

$$E_r = \frac{\partial\phi(r, z)}{\partial r} = 2C_2(z)r \quad (17)$$

2.3 Drain current

The flow of current I_{DS} in a surrounding gate TFET is based on Band-to-Band Tunneling (BTBT) of electrons from the valance band of the source to the conduction band of the channel region. The tunneling generation rate (G) can be calculated using Kane's model [18, 19]. The total drain current is then computed by integrating the band to band generation rate over the volume of the device.

$$I_{DS} = q\pi r^2 \iint G(r, z) dr dz \quad (18)$$

For the calculation of tunneling Generation rate (G), Kane's Model has been employed [18, 19]

$$G(E) = A_{kane} \frac{|E|^2}{\sqrt{E_g}} e^{-\left[\frac{B_{kane}}{|E|} \frac{E_g^{3/2}}{|E|} \right]} \quad (19)$$

Where,

$$A_{kane} = \frac{q^2 \sqrt{2m_{tunnel}}}{h^2 \sqrt{E_g}}$$

$$B_{kane} = \frac{\pi^2 E_g^{3/2} \sqrt{m_{tunnel}} / 2}{qh}$$

$$\frac{1}{m_{tunnel}} = \frac{1}{m_h m_0} + \frac{1}{m_e m_0}$$

$|E|$ is the magnitude of the electric field which is defined as $|E| = \sqrt{E_r^2 + E_z^2}$ and E_g is the energy band gap. m_0 is the rest mass of an electron, m_e and m_h are the electron and hole effective masses respectively.

3. Result and Discussion

To verify the accuracy of the analytical model, two-dimensional device simulation has been performed by using TCAD Sentaurus [20]. The models available in TCAD to simulate band-to-band tunneling are Kane's Band-to-Band model, Hurkx's Band-to-Band model,

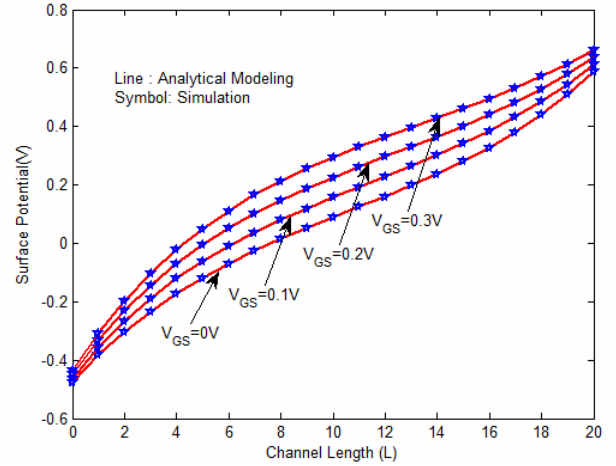


Fig. 2. Surface potential profiles of surrounding gate-TFET for Channel Length $L=20\text{nm}$ and $V_{DS}=0.1\text{V}$ with different gate biases.

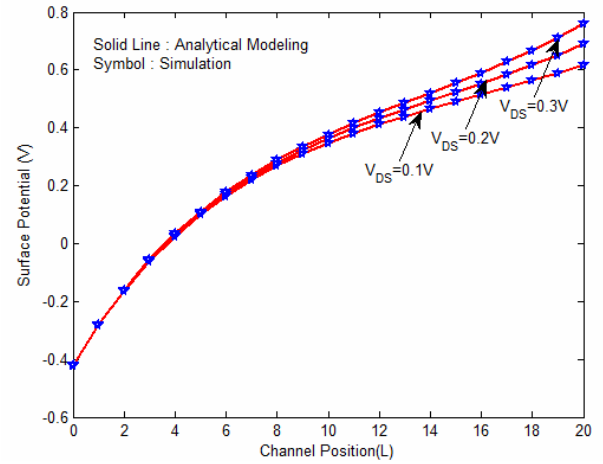


Fig. 3. Surface potential profiles of surrounding gate-TFET for channel length $L=20\text{nm}$ and $V_{GS}=0.4\text{V}$ with different V_{DS} .

Schenk's Band-to-Band model and the dynamic Non Local Band-to-Band model. In our work the Kane's model is used to evaluate the band-to-band generation rate. The proposed analytical model, results have been compared with simulation results.

Fig. 2 shows the calculated surface potential profile for different gate voltage of the surrounding gate TFET structure along with the simulated potential profile. As the gate voltage increases, the potential in the lightly doped region increases. The analytical results have been compared with the TCAD simulated results and a good agreement is achieved.

Fig. 3 shows the calculated surface potential profile for different drain voltages of the surrounding gate TFET structure for a channel length of $L=20\text{nm}$ along with the simulated potential profile. As the drain voltage increases, the potential near the drain region increases. But there is no significant change in potential near the source region.

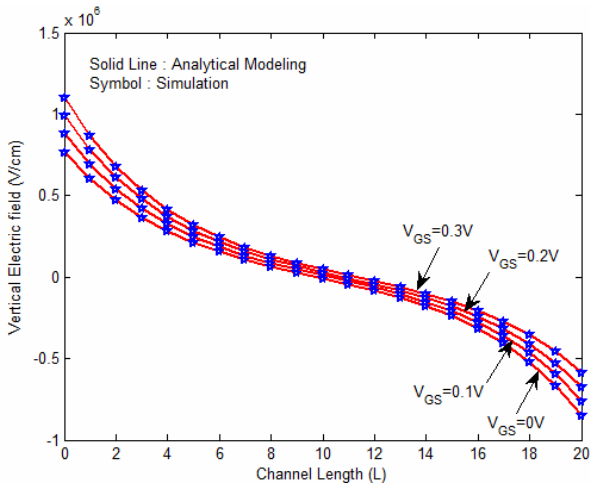


Fig. 4. Vertical electric field of surrounding gate-TFET for Channel length $L = 20\text{nm}$ and $V_{DS} = 0.5\text{V}$ with different gate biases.

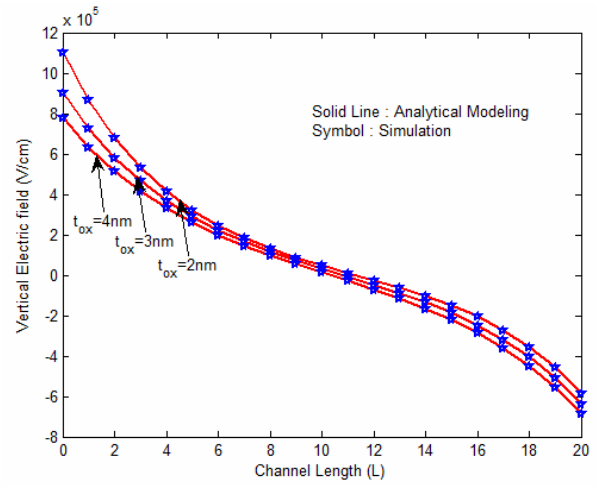


Fig. 6. Vertical electric field of a Surrounding gate TFET with different gate oxide thicknesses

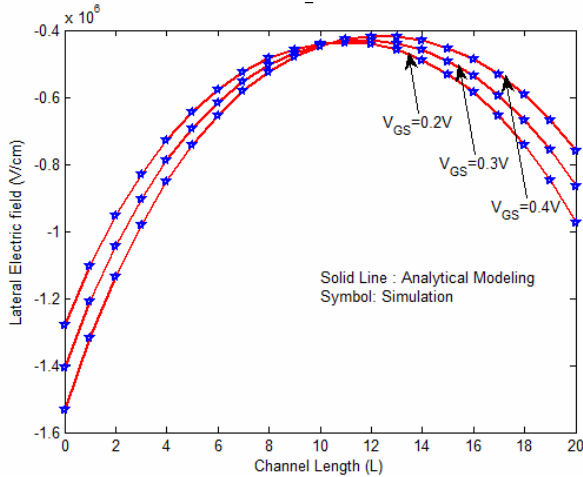


Fig. 5. Lateral electric field of surrounding gate-TFET for Channel length $L = 20\text{ nm}$ and $V_{DS} = 0.5\text{ V}$ with different gate biases

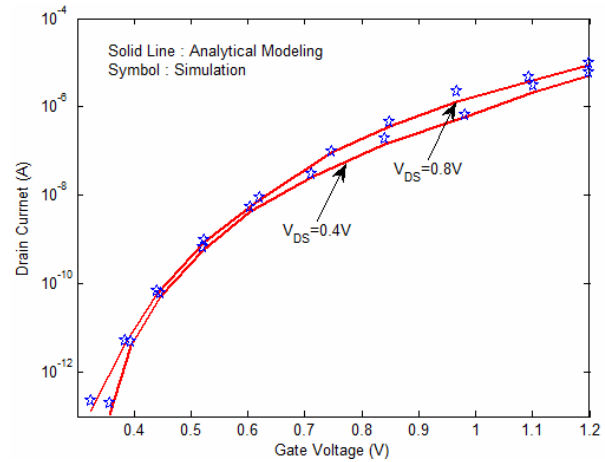


Fig. 7. I_D - V_{DS} characteristics of surrounding gate TFET for channel length $L=20\text{ nm}$ with varies drain voltage V_{DS}

Hence we deduce that the drain voltage has no impact on the tunneling generation rate on the source side. The results have been compared with the simulated results obtained from the simulation software, and a good agreement is achieved between the two results.

Fig. 4 shows the calculated and simulated values of vertical electric field distribution along the channel position for different values of gate voltages. It is evident from the figure that the peak of the vertical electric field appears near the source side. This leads to increase in tunneling generation rate. Due to this effect the tunneling current gets increased. From the results it is clearly understood that the calculated values of the analytical model tracks the simulated values very well.

Fig. 5 shows that calculated and simulated values of lateral electric field with channel length $L_{CH}=20\text{nm}$ for different gate voltages of the Surrounding gate TFET

structure. Lateral electric field is mainly contributed by the Drain to Source bias of the device. As the source-drain bias became more prominent and causes a raise in lateral electric field, which in turn decreases the gate control over the channel. When gate voltage is varied, the change of lateral electric field is less when compared with that of vertical electric field in the channel region. It is clearly seen from the figure that the lateral electric field is less dominant on this device structure. The analytical results are in excellent agreement with simulation results.

The vertical electric field against the channel length ($L=20\text{nm}$) has been plotted in Fig. 6 for surrounding gate TFET with different values of gate oxide thickness. It may be observed from the figure that the dependence of the vertical electric field on the channel length can considerably be increased by reducing the thickness of the gate oxide.

Fig. 7 shows the modeled and simulated values of I_D -

V_{DS} characteristics of surrounding gate TFET with drain voltages 0.4V and 0.8V. For the positive values of V_{GS} , electrons tunnel from valence band in p+ source region to conduction band in channel region and the tunneling current gets increased. Here in this region, the device behaves as an n type surrounding gate TFET. Analytical results are in excellent agreement with simulation results.

4. Conclusion

In this work, the surrounding gate TFET structure has been analyzed and its performance improvement over different parameters is discussed. The analytical model is based on two-dimensional Poisson's equation which is solved using parabolic approximation. The analytical expressions of surface potential, lateral electric field and vertical electric field have been calculated. In this model, components of lateral electric field and vertical electric field can be used for calculating the distribution of tunneling generation rate and numerically extract the tunneling current. Based on the generation rate and electric fields, we have obtained the $I_{DS}-V_{GS}$ characteristics. From the presented results, it can be concluded that the surrounding gate structure provides wide range of benefits to the TFET performance. The results clearly demonstrate the excellent immunity against SCEs such as reduced leakage current and improved ON current offered by the surrounding gate TFET structure against the decreasing channel length. The proposed model can be expected to be successfully applied in fabrication scenarios of advanced VLSI design CMOS technologies.

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T. S. Arun Samuel was born in Marthandam, India in 1983. He received his Bachelors of Engineering degree from the department of Electronics and Communication from Madurai Kamaraj University, Madurai, India and Masters Degree in Computer and Communication from Anna University, Chennai in 2004 and 2006 respectively.

After working as Lecturer in Francis Xavier Engineering College, Tirunelveli, he is currently pursuing Ph.D degree in the Department of Electronics and communication engineering, Thiagarajar College of engineering, Tamilnadu, India under Anna University Chennai. His research interests include Multi gate transistors and Tunnel Field effect Transistors.



N. B. Balamurugan received his B.E and M.E degrees, both in electronics and communication engineering from the Thiagarajar College of Engineering (TCE), Tamilnadu, India. He has obtained his Ph.D degree in nano-electronics at Anna University, India.

From 1998 to 2004, he worked as a lecturer in R.V.S.college of engineering and technology, Tamilnadu, India. He is currently as an Assistant Professor in the Department of Electronics and Communication Engineering, Thiagarajar College of Engineering (TCE), Tamilnadu, India. He has published more than 50 research papers as sole or joint author in the field of device modeling and simulation. His research interests include analytical modeling and simulation of semiconductor device structures like Nanoscale SOI MOSFETs, Nanowire Transistors Tunnel FET and Quantum Effects in Multigate MOSFETs.



T. Niranjana was born in Thirumangalam, Madurai, and Tamilnadu, India on 1994. She is currently pursuing the B.E., degree in the Department of Electronics and Communication Engineering from Thiagarajar College of Engineering, Madurai. Her interests include VLSI Device Modeling and

Digital Electronics.



B. Samyuktha was born in Srirangam, Trichy, Tamilnadu, India on 1993. She is currently pursuing the B.E., degree in the Department of Electronics and Communication Engineering from Thiagarajar College of Engineering, Madurai. Her interests include VLSI Device Modeling and Digital Elec-tronics.