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A Compact Quantum Model for Cylindrical Surrounding Gate MOSFETs using High-k Dielectrics

P. Vimala† and N. B. Balamurugan*

Abstract – In this paper, an analytical model for Surrounding Gate (SG) metal-oxide- semiconductor field effect transistors (MOSFETs) considering quantum effects is presented. To achieve this goal, we have used variational approach for solving the Poission and Schrodinger equations. This model is developed to provide an analytical expression for inversion charge distribution function for all regions of device operation. This expression is used to calculate the other important parameters like inversion charge density, threshold voltage, drain current and gate capacitance. The calculated expressions for the above parameters are simple and accurate. This paper also focuses on the gate tunneling issue associated with high dielectric constant. The validity of this model was checked for the devices with different dimensions and bias voltages. The calculated results are compared with the simulation results and they show good agreement.

Keywords: Surrounding gate MOSFETs, Quantum effects, Inversion charge density function, Variational approach.

1. Introduction

Surrounding gate (SG) MOSFETs have been proposed to extend the scaling limit of conventional MOSFETs to 10nm gate length and beyond, owing their excellent control of the short-channel effects and high current driving ability [1-5]. Several classical models have been developed for SG MOSFETs. A compact model should include the quantum effects too.

One the quantum effect is known as energy quantization. The effect of quantization of electronic energy becomes significant for 10 nm and thus it is extremely important to consider quantum effects in MOSFET models. In nanoscale regime, the SG MOSFETs show a different behaviour in comparison to their bulk MOSFETs counter parts is the inversion charge because it is strongly confined in the channel of these devices. As consequence, one of the most interesting parameters that can be modeled is the average inversion layer penetration (defined as the inversion layer centroid [6-8]), which can be used to quantify the influence of quantum effects on the inversion charge of the MOSFETs [7] as well as in the channel capacitance. In this respect, the accurate calculation of these parameters is essential to develop good compact models to be used in circuit simulators. The second effect is that the direct tunneling of carriers between the gate electrode and silicon substrate known as gate tunneling. A solution to this gate leakage problem is the replacement of the silicon di-oxide with a material of higher dielectric constant (a concept abbreviated as high-k) [9], [10].The high dielectric constant means that the insulator can be thicker for a given gate capacitance, while presumably allowing exponentially less tunneling current than the oxide. These two phenomena should be incorporated into the classical model to make it complete.

Some models have been established for QM effects of Si Surrounding gate MOSFETs. The exact modeling of SG MOSFETs, which determines the charge distribution and current in the device is a complicated task. The reason is that the complete solution of the problem has to be obtained by solving the coupled Poisson and Schrodinger equation. Yuan [11] developed an analytical model for threshold voltage shift in the surrounding gate MOSFETs considering quantum confinement. Yu-Sheng [12] described the quantum effects in surrounding gate MOSFET and Moreno [13] has studied the quantum effects in the square GAA MOSFETs. However, extensive studies are not done to analyse the quantum effects in surrounding gate MOSFETs. Mathematical complexities of the above models are impractical for compact modeling. Roldan [14] have developed a model for centroid and inversion charge of Surrounding Gate MOSFETs including quantum effects. The wave functions as a function of different device parameters were obtained from the numerical simulator used by them. A good analytical model which simplifies the above problems is still to be developed. Our model is based on the analytical solution of Poisson's-Schrodinger equation using variational approach. This approach involves guessing a reasonable, parametric form for a trial wave function ($\psi_0(r)$).

Therefore, the purpose of this paper is to derive an

† Corresponding Author: Dept. of Electronics and Communication Engineering, Thiagarajar College of Engineering, Madurai, India. (vimalapalanichamy@tce.edu)
* Dept. of Electronics and Communication Engineering, Thiagarajar College of Engineering, Madurai, India. (nbbalamurugan@tce.edu)
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accurate analytical quantum model for cylindrical surrounding gate MOSFETs .The rest of the paper is organized as follows: Section 2 presents the development of quantum analytical model for SG MOSFET by solving the coupled Poisson and Schrodinger equations. Section 3 gives the influence of quantization on device terminal parameters namely centroid, inversion charge density and I-V, C-V characteristics are extracted as closed form functions of radius, inversion charge density and bias voltage for different high-k dielectrics. Model verification and descriptions of main results are presented in section 4. Finally the conclusions are given in section 5.

2. Quantum Modeling

The structure and schematic and cross section view of the SG MOSFET is shown in Fig. 1 with radius of semiconductor cylinder R , dielectric gate insulator thickness t_{high-k} . For this structure, we solved the Poisson and Schrodinger equations (P-S) using variational approach [15] to obtain the quantum effects.

Modeling the quantum effects with a very high accuracy involves solving the coupled P-S self-consistently. The variational technique represents a completely different way of getting approximate energies and wave functions for quantum mechanical systems. Therefore, to model quantum effects, the method used in this paper refers to the variational approach which involves an analytical approximation of ground state energy based itself initially on the choice of wave function. Moreover, in order to simplify the different equations, we can focus exclusively on the lowest-energy subband wavefunction. By using several trial wave functions, we found the optimum wave function for SG MOSFETs as given below:

$$\psi_o(r) = a_0\sqrt{1/R}\,\sin\left[\frac{\pi(r+R)}{2R}\right]\exp\left[\frac{-b_0(r+R)}{2R}\right] \quad (1)$$

where a_0 and b_0 are the unknown parameters.

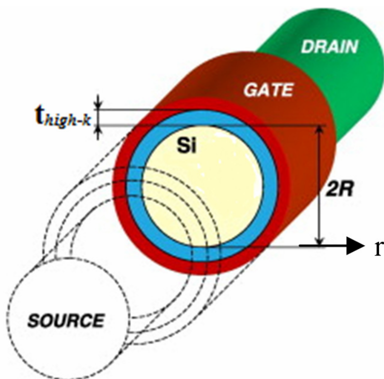

Fig. 1. Schematic and Cross section of the silicon SG MOSFETs

Normalization of (1) meaning gives an expression of a_0 in terms of b_0 .

Normalization of (1), which means $\int_0^R \psi_0^2(r)dr = 1$ gives,

$$a_0 = \sqrt{\frac{2b_0\left(b_0^2+\pi^2\right)}{e^{-2b_0}\left(2b_0^2 e^{b_0} + \pi^2\left(e^{b_0}-1\right)\right)}} \quad (2)$$

Considering the eigenfunction of (1), we use the variational approach to solve the Poisson equation as follows,

$$\frac{d^2\phi(r)}{dr^2} + \frac{1}{r}\frac{d\ \phi(r)}{dr} = \frac{q}{\varepsilon_{si}}N_{inv}\left|\psi_0(r)\right|^2 \quad (3)$$

where q is the electronic charge, $n(r)$ is the electron density, ε_{si} is the silicon permittivity and $\phi(r)$ is the electric potential of silicon region. Solving (3) analytically, we obtained the electric potential in terms of b_0 .

The 1D Schrodinger equation is written as,

$$\frac{-h^2}{2m_e}\frac{d^2\psi_0(r)}{dr^2} + (-q)\phi(r)\psi_0(r) = E_0\psi_0(r) \quad (4)$$

where, h is the Plank's constant, $m_e = 0.916m_0$ is the effective mass of electrons in lower energy level with (100) orientation, E_0 is the lowest subband energy. The value of kinetic and potential energies in the lowest subband is given by,

$$E_{0(kin)} = \frac{-h^2}{2m_e}\int_0^R \psi_0(r)\frac{d^2\psi_0(r)}{dr^2}dr$$
$$E_{0(pot)} = -q\int_0^R \psi_0^2(r)\phi(r)dr \quad (5)$$

From (5), the lowest subband total energy is written as,

$$E_0 = \left\langle E_{0(kin)}\right\rangle + \left\langle E_{0(pot)}\right\rangle \quad (6)$$

In the quantum variational approach, b_0 is evaluated by minimizing E_0, i.e., $dE_0/db_0 = 0$. A good approximation for b_0 is derived as,

$$b_0 \approx R\pi^2\left(\frac{5}{6}\frac{qm_x Q_{inv}}{\varepsilon_{si}h^2}\right) \quad (7)$$

Note that the variational parameter (b_0) is dependent on the inversion charge density (Q_{inv}) and silicon radius R .

3. Compact Surrounding Gate MOSFET Model

For the compact quantum modeling purpose the parameters like inversion charge centroid, threshold voltage, inversion charge density, gate capacitance and drain current are extracted from the Poisson-Schrodinger equations. In this section, we develop an analytical model for the above parameters of SG MOSFETs which includes the quantum effects.

$$Q_{inv} = C_{TOTAL} \left(-\frac{2C_{TOTAL}V_{th}^2}{Q_0} + \sqrt{\left(\frac{2C_{TOTAL}V_{th}^2}{Q_0}\right)^2 + 4V_{th}^2 \ln^2\left(1+\exp\left(\frac{V_{GS}-V_T+\Delta V_T-V}{2V_{th}}\right)\right)} \right) \tag{8}$$

In the classical case, the density maximum is always located directly at the interface. But in the quantum mechanical case, the electrons are distributed more toward the center of the silicon body. Based on [14], the expression of inversion-charge density is given in (8).

The total capacitance is given by,

$$\frac{1}{C_{TOTAL}} = \frac{1}{C_{ox\ high-k}} + \frac{1}{C_{Semi}} \tag{9}$$

where, $C_{ox\ \text{high-k}}$ and C_{semi} are calculated as,

$$C_{ox\ high-k} = \frac{\varepsilon_{high-k}}{R\ln\left(1+\frac{t_{high-k}}{R}\right)} \tag{10}$$

$$C_{Semi} = \frac{\varepsilon_{si}}{\left(R-x_I\right)\ln\left(1+\frac{x_I}{R-x_I}\right)} \tag{11}$$

where ε_{high-k} is the permittivity of high-k dielectric material. x_I is the inversion charge centroid is calculated using wavefunction given in Eq. (1).

The inversion layer centroid is obtained by,

$$x_I = \int_0^R r\psi_0^2 dr \tag{12}$$

The final expression for SG centroid is given in Eq. (13). The centroid model is validated for various values of R and N_{inv} .

$$x_I = \frac{Ra_0^2 e^{-2b_0}}{b_0\left(b_0^2+\pi^2\right)^2} \left(-b_0^2\left(3+b_0\right)\pi^2 - \left(1+b_0\right)\pi^4 + e^{b_0}\left(2b_0^4 + b_0^2\pi^2 + \pi^4\right)\right) \tag{13}$$

The drain current in SG MOSFET is obtained with the assumption that the mobility is independent of the position in the channel. It is expressed as,

$$I_{DS} = \mu \frac{2\pi R}{L} \int_0^{V_D} Q_{inv}(V)dV \tag{14}$$

To calculate the drain current we have to solve (8) for $V=0$ at the source end, $Q_{inv}=Q_s$ and $V=V_d$ at the drain end, $Q_{inv}=Q_d$. Based on [16], the drain current expression is obtained in terms of inversion charge density as given in Eq. (15).

$$I_{DS} = \mu \frac{2\pi R}{L}\left[2V_{th}\left(Q_s-Q_d\right) + \frac{Q_s^2-Q_d^2}{2C_{ox\ \text{high-k}}} + V_{th}Q_0 \ln\left(\frac{Q_d+Q_0}{Q_s+Q_0}\right)\right] \tag{15}$$

where μ is the mobility constant.

4. Results and Discussions

In this section, the accuracy of the proposed model is examined with the simulation results. The accuracy of the proposed model is verified using the commercially available TCAD Sentaurus device simulator. The set of parameters used for simulation are shown in Table-1. In this section, we will also review the influence of various

Table 1. Nomenclature of symbols

Symbol	Description	Values
ϕ_m	Metal work function	4.10eV
L	Channel Length	60nm
t_{high-k}	Gate oxide thickness	1 to 3nm
R	Silicon radius	1 to 10nm
N_A	Accepter Concentration	10^{15}

Table 2. Different gate dielectric materials and their high-k constant values

Dielectric Material	Dielectric Constant
SiO_2	$k=3.9$
Si_3N_1	$k=7.5$
Al_2O_3	$k=10$
$LaAlO_3$	$k=15$
HfO_2/ZrO_2	$k=25$
TiO_2	$k=40$

high-k gate dielectrics in cylindrical surrounding gate MOSFETs. The analysis was performed for a wide range of proposed gate dielectric high-k values such as 3.9, 7.5, 10, 15, 25, and 40. Table 2 shows the different gate dielectric materials and their corresponding high-k constant values.

The threshold voltage is examined in Fig. 3 with different silicon radius at different high-k dielectric constant. The threshold voltage value is decreases with the high-k dielectric constant increases. This reduction does not correspond to the decreased limit of inaccuracy of the classical case. But demonstrate the lowering of threshold voltage values in both classical and quantum approach and thus, resulting in small difference in threshold voltage for a given silicon radius value. The reduced threshold voltage promises a choice of low power consuming device together with low switching action, thereby improving the characteristics appreciably for fast switching applications.

Fig. 2 shows the inversion charge density variation with gate voltage at different high-k configurations together with different parameters. The trend of inversion charge density with gate voltage is in accordance with device physics. The replacement of high-k material shows an improved device performance with increased inversion charge density as compared with SiO_2 dielectric. This can be explained as; the high-k device offers high surface potential in comparison to SiO_2 device. This high potential results in inversion of carriers at reduced gate voltage and thus, offering more carriers in channel region. Thus, the insulating layer material is significant for obtaining device characteristics and is required to be monitored for optimum performance.

The drain current variations with drain voltage and gate source voltage are plotted in Figs. 4 and Fig. 5 respectively with different gate insulator materials. High-k materials are found to be promising to increase the drive current performance of MOSFETs. This enhanced performance is due to the fact that replacing the conventional SiO_2 layer with high-k layer results in high value of surface potential, thus increasing the inversion charge density. This increased

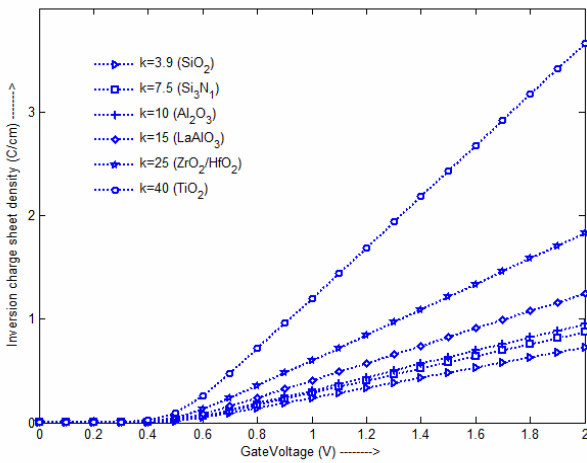

Fig. 2. Inversion charge density versus gate voltage at different High-k dielectric.

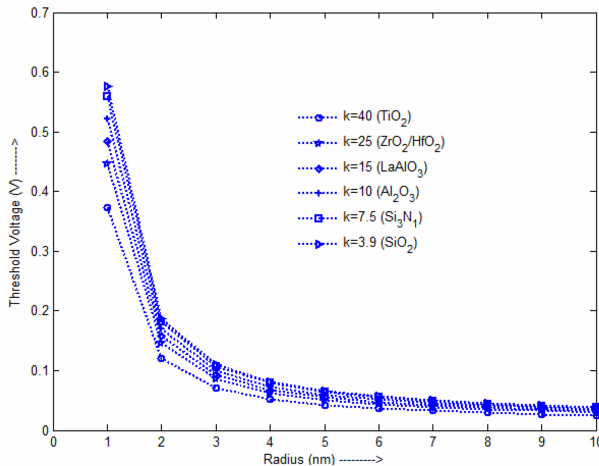

Fig. 3. Threshold voltage variations with silicon radius at different High-k dielectric

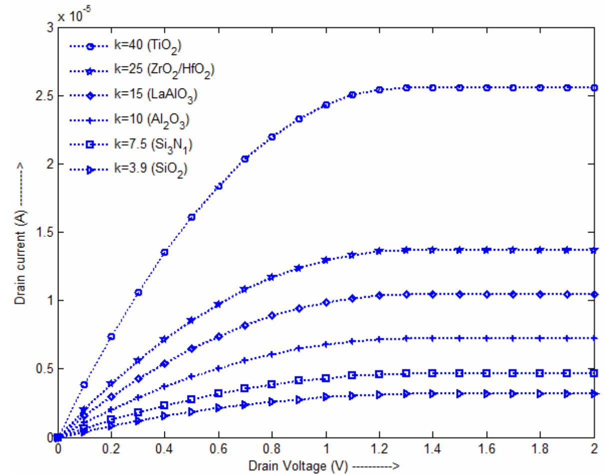

Fig. 4. Variation of drain current with gate voltage of cylindrical surrounding gate MOSFETs at different dielectric thickness

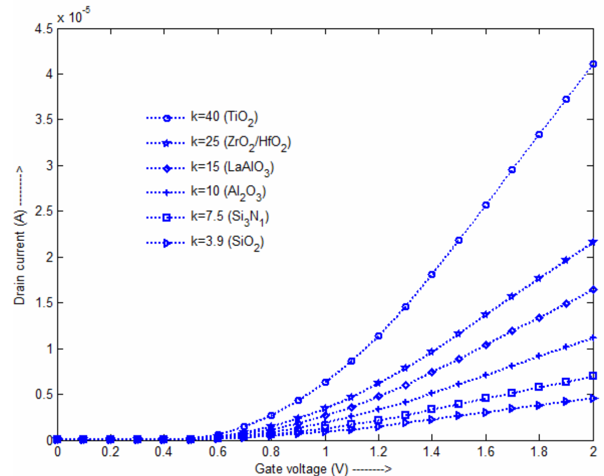

Fig. 5. I-V characteristics of cylindrical surrounding gate MOSFETs with R=8nm.

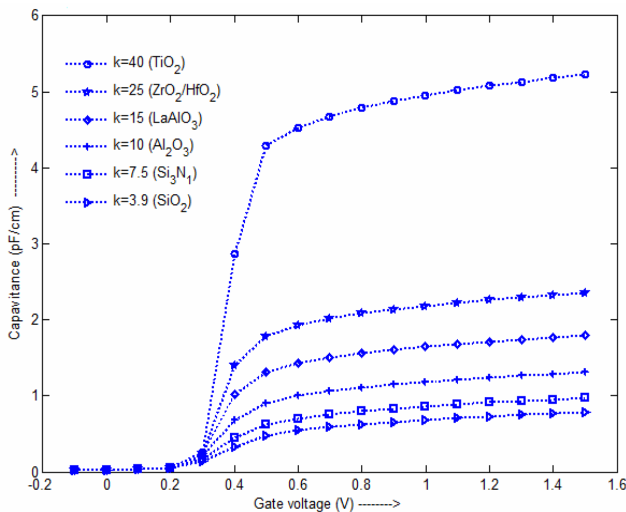

Fig. 6. Gate capacitance characteristics of different high-k dielectric for different gate voltages

surface potential thereby reduces the device threshold voltage, and increased carrier density leads to rise in device field effect mobility. All these effects i.e. increased surface potential, increased carrier density, reduced threshold voltage and increases mobility results in high drain current for circuit driver applications.

The gate capacitance of a trigate MOSFET may be obtained from dQ_{inv}/dV_{gs} . The gate capacitance variation with gate source voltage is shown in Fig. 6. It can be seen from the figure that introduction of high-k materials though offers high peak of gate capacitance compare with SiO_2 layer characteristics. This is due to the fact that for the initial gate voltages approximately 0v to 0.2v, the value of gate capacitance is abruptly zero. Then the capacitance value shoots up to its maximum due to high-k dielectric layer. The device characteristic with SiO_2 layer superimposes on device characteristics with TiO_2. This shows an alternative to conventional oxide layer, which is facing the physical limit to scale down in order to meet the requirement of scaled devices.

5. Conclusion

In this paper, we have presented an analytical energy quantization model for SG MOSFETs. The model is based on the variational approach, which takes into account of the silicon radius and gate to source voltage. The model has been tested by means of a comparison with simulation data for various device dimensions and bias values. We have developed the analytical model for other device parameters like inversion charge centroid, inversion charge, and drain current by considering quantum effects. The influences of high-k dielectric constants are also included in this model to reduce the gate tunneling current. A very good agreement between the modeled and simulated data was achieved for all the device parameters. Therefore the proposed approach is appropriate for the modeling of surrounding MOSFETs in the presence of quantum effects.

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P.Vimala received her B.E and M.E degrees, both in electronics and communication engineering from Anna University, Chennai, Tamilnadu, India. She is currently pursuing the Ph.D degree in the Department of Electronics and Communication Engineering, Thiagarajar College of Engineering (TCE), Tamilnadu, India under Anna University, Chennai. She is awarded with Women Scientist Fellowship for three years for her research work from Department of Science and Technology (DST), New Delhi, Government of India. Her research interests focused on Quantum Modeling and Simulation of Multigate MOSFETs. She is currently engaged in the modeling of Energy quantization in tri-gate MOSFETs and analyzing its performance using the Synopsis TCAD Simulation tool.

N. B. Balamurugan received his B.E and M.E degrees, both in electro-nics and communication engineering from the Thiagarajar College of Engin-eering (TCE), Tamilnadu, India. He has obtained his Ph.D degree in nano-electronics at Anna University, India. From 1998 to 2004, he worked as a lecturer in R.V.S.college of engineering and technology, Tamilnadu, India. He is currently as an Assistant Professor in the Department of Electronics and Communication Engineering, Thiagarajar College of Engineering (TCE), Tamilnadu, India. He has published more than 50 research papers as sole or joint author in the field of device modeling and simulation. His research interests include modeling and simulation of semiconductor device structures.