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# ESL-Γ-Z- Source Inverter

**Lei Pan*, Hexu Sun†, Beibei Wang**, Yan Dong*** and Rui Gao****

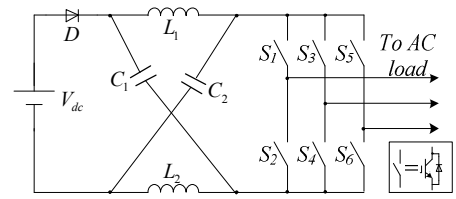
**Abstract** – On the basis of the traditional ZSI (Z-source inverter), this paper presents a ESL-Γ-ZSI, which uses a unique Γ-shaped impedance network and an extended SL network for boosting its output voltage in addition to their usual voltage-buck behavior. The inverter can increase the boost factor through adjusting shoot-through duty ratio and increasing the number of inductors. Capacitor voltage stress of ESL-Γ-ZSI is a constant when 1>D>0, and ESL-Γ-ZSI has small inductor current stress. The working principle of ESL-Γ-ZSI and comparison with the classical ZSI and SL- ZSI are analyzed in detail. The power loss comparison between ESL-Γ-ZSI and Cuk converter is analyzed detailedly. Simulation and experimental results are given to demonstrate the operation features of the inverter.

**Keywords**: ESL Network, Capacitor voltage stress, Γ-shaped, Inductor current stress.

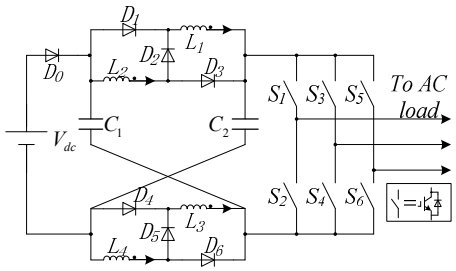
## 1. Introduction

Modern power electronic applications, especially those directly connected to the grid, usually require some voltage boosting. Traditional voltage-source inverters (VSIs) are therefore not satisfactory since they can only step down voltages. To add boost functionality, dc-dc boost converters can be placed before the VSIs. Alternatively, single-stage buck-boost inverters can be used like the Cuk, SEPIC and other similar dc-ac inverters. However, these inverters do not have been intensive follow-up researched. On the contrary, research in another buck-boost inverter, named as Z-source inverter shown in Fig. 1 (a) [1], has been proposed.

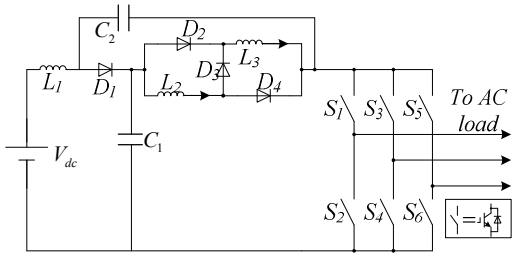
In recent years, various Z-source inverter (ZSI) topologies have been presented in numerous diversified studies [1-4]. Some of the studies are focused on modeling and control [5-8], modulation strategy [9-12], applications [13-16], and the development of new topologies [17-24]. In [19-21], the focus is on improving the boost factor of the ZSI. For instance, in [19], inductors, capacitors, and diodes are added to the Z- impendence network to produce a high dc link voltage for the main power circuit from a very low input dc voltage. In [20] and [21], switched-inductor ZSI (SL-ZSI, shown in Fig. 1(b)) and switched-inductor quasi-ZSI (SL-qZSI, shown in Fig. 1(c)) are successful combination of the ZSI and switched-inductor structure, and provide strong step-up inversion to overcome the boost limitation of the classical ZSI. In [22, 23], two inductors of the impedance Z-network are replaced by a transformer. In [22], Trans-ZSI can obtain high boost factor, when the turns ratio of the transformer windings is over 1. In [23], Γ-ZSI can obtain high boost factor by varying the turns ratio of the transformer within the narrow range, (1, 2]. In [24], it proposed an improved Z-source inverter, which can reduce the capacitor voltage stress and suppress the inrush




(a) The classical ZSI




(b) SL-ZSI




(c) SL-qZSI

**Fig. 1.** Conventional impedance-network inverter topologies

† Corresponding Author**:** Control Science and Engineering School, HeBei University of Technology, Tianjin, China. (hxsun@hebut.edu.cn)
* Control Science and Engineering School, HeBei University of Technology, Tianjin, China; School of Control and Mechanical Engineering, Tianjin Chengjian University, Tianjin, China. (panlei 4089@163.com)
** School of Control and Mechanical Engineering, Tianjin Chengjian University, Tianjin, China. (wbbking@163.com, gaorui223@126.com)
*** Control Science and Engineering School, HeBei University of Technology, Tianjin, China. (dongyan73@hebut.edu.cn)
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surge of Z-source capacitors and inductors.

Despite the aforementioned merits, the aforementioned Z-source inverter topologies also show the following drawbacks: 1) capacitor voltage stress is increased with the increase of shoot-through duty ratio, thus high-voltage or large capacity capacitors should be used, which may result in large volume, high cost, and reducing the life span of system; 2) inductor current stress is large, and this characteristic may also lead to large volume and high cost; 3) it regulates boost factor only by adjusting the shoot-through duty ratio, and boost factor is very small with short shoot-through zero state.

To solve the aforesaid drawbacks in aforementioned Z-source inverter, a new Z-source inverter topology is presented with extended SL network and unique Γ-shaped impedance network without transformer. The operation principle and comparison with the classical ZSI and SL-ZSI reveal the merits of the proposed topology, which are also verified in both simulation and experiment.

## 2. ESL-Γ- Z- Source Inverter

Different to the original ZSI, ESL-Γ-ZSI has just one capacitor, and is composed of an extended SL network, a capacitor, and an extra inductor as shown in Fig. 2. The proposed topology provides an extended SL network in front of the inverter bridge, unlike the traditional topology, so there is no inrush current flowing to the main circuit at startup.

Like the classical ZSI, ESL-Γ-ZSI has extra shoot-through zero states besides the traditional six active and two zero states. Thus, the operating principles of the proposed inverter are similar to those of the classical ZSI. For the purpose of analysis, the operating states are simplified into shoot-through and nonshoot-through states. Fig. 3 shows the equivalent circuits of ESL-Γ-ZSI.

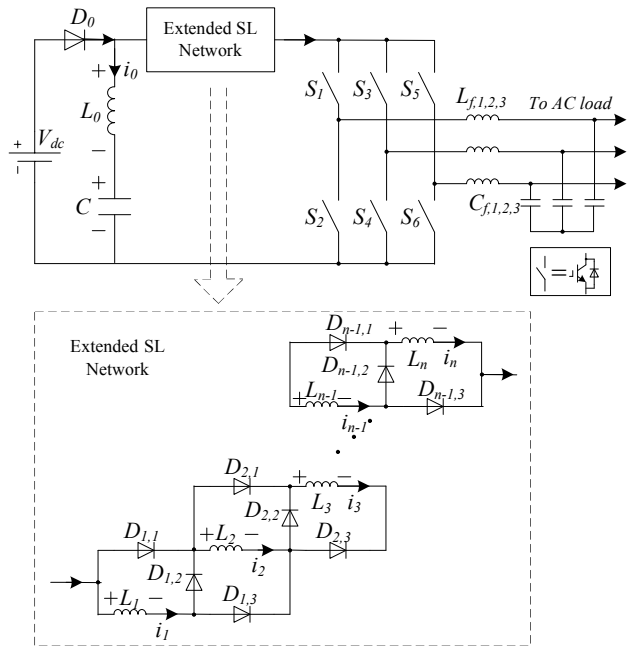



**Fig. 2.** Proposed topology for ZSI with extended SL network ($L_1 = L_2 = L_3 = \ldots = L_{n-1} = L_n = L$, $n \geq 2$).

In the nonshoot-through state, as shown in Fig. 3(a), $D_{1,2}$, $D_{2,2}$, … , $D_{n-1,2}$ and $D_{n,2}$ are on, while $D_0$, $D_{1,1}$, $D_{1,3}$, $D_{2,1}$, $D_{2,3}$, … , $D_{n-1,1}$, $D_{n-1,3}$, $D_{n,1}$ and $D_{n,3}$ are off. $L_1$, $L_2$, …, $L_{n-1}$ and $L_n$ are connected in series. $C$, $L_0$, $L_1$, $L_2$, …, $L_{n-1}$ and $L_n$ transfer energy to the main circuit. The corresponding voltages across $L_0$, $L_1$, $L_2$, …, $L_{n-1}$ and $L_n$ in this state are $V_{0\_non}$, $V_{1\_non}$, $V_{2\_non}$, $V_{3\_non}$, …, $V_{n-1\_non}$ and $V_{n\_non}$, respectively. Thereby, (1) and (2) can be obtained.

$$V_{1\_non} + V_{2\_non} + \cdots + V_{n\_non} + V_i = V_{0\_non} + V_c \quad (1)$$

$$-V_{0\_non} = V_{1\_non} = V_{2\_non} = \cdots = V_{n\_non} \quad (2)$$

(3-6) and (7) can be concluded, from (1) and (2).

$$V_{0\_non} = -\frac{1}{n+1}V_c + \frac{1}{n+1}V_i \quad (3)$$

$$V_{1\_non} = \frac{1}{n+1}V_c - \frac{1}{n+1}V_i \quad (4)$$

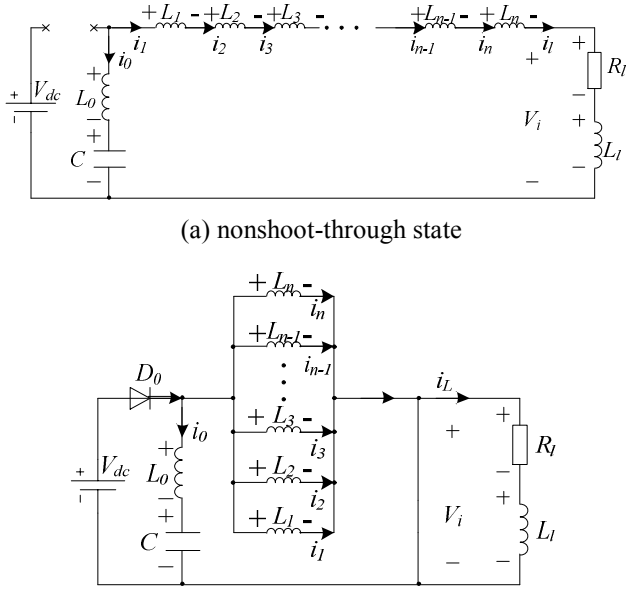
$$V_{2\_non} = \frac{1}{n+1}V_c - \frac{1}{n+1}V_i \quad (5)$$

$$\vdots$$

$$V_{n-1\_non} = \frac{1}{n+1}V_c - \frac{1}{n+1}V_i \quad (6)$$

$$V_{n\_non} = \frac{1}{n+1}V_c - \frac{1}{n+1}V_i \quad (7)$$

In the shoot-through state, as shown in Fig. 3(b), the inverter side is shorted by both the upper and lower switching devices of any phase leg. During the shoot-through state, $D_{1,2}$, $D_{2,2}$, … , $D_{n-1,2}$ and $D_{n,2}$ are off, while



(a) nonshoot-through state

(b) shoot-through state

**Fig. 3.** Operating states for ESL-Γ-ZSI

$D_0$, $D_{1,1}$, $D_{1,3}$, $D_{2,1}$, $D_{2,3}$, … , $D_{n-1,1}$, $D_{n-1,3}$, $D_{n,1}$ and $D_{n,3}$ are on. $L_1$, $L_2$, …, $L_{n-1}$ and $L_n$ are connected in parallel, and $C$, $L_0$, $L_1$, $L_2$, …, $L_{n-1}$ and $L_n$ store energy, obtaining

$$V_1 = V_2 = \cdots = V_{n-1} = V_n = V_{dc} \quad (8)$$

$$V_0 + V_c = V_{dc} \quad (9)$$

Applying the volt-second balance principle to each inductor [5], (10-12) and (13) are obtained, as follows.

$$B = \frac{2+(n-1)D}{1-D} \quad (10)$$

$$I_0 = 0 \quad (11)$$

$$I_L = I_1 = I_2 = \cdots = I_{n-1} = I_n = \frac{2+(n-1)D+\frac{L_l}{L}D}{1-D}\frac{V_{dc}}{R_l} \quad (12)$$

$$I_l = \frac{2+(n-1)D}{R_l}V_{dc} \quad (13)$$

(10) can be divided into two parts 1/(1-$D$) and [1+($n$-1)$D$]/(1-$D$). 1/(1-$D$) is produced by $L_0$ and $C_0$, and [1+($n$-1)$D$]/(1-$D$) is produced by $L_1$, $L_2$, …, and $L_n$. The existence of $L_0$ makes the voltage of $C_0$ become a constant $2V_{dc}$.

When the load is resistive, (14) is concluded, as follows.

$$I_L = I_1 = I_2 = \cdots = I_{n-1} = I_n = \frac{2+(n-1)D}{R_l(1-D)}V_{dc} \quad (14)$$

## 3. Features Analysis

### 3.1 Boost ability and stress analysis

Voltage adjustability ability, capacitor voltage stress and inductor current stress are important parameters for ZSI. Table 1 shows the each stress for ESL-Γ-ZSI, the classical ZSI and SL-ZSI [20].

Compared with the classical ZSI and SL-ZSI, the proposed inverter can increase the voltage boost inversion ability through adjusting short shoot-through zero state or the number of inductors as shown in Fig. 4. From Fig. 4, it can be seen that boost factor is increased with the increasing of shoot-through duty ratio and the increasing of the number of inductors.

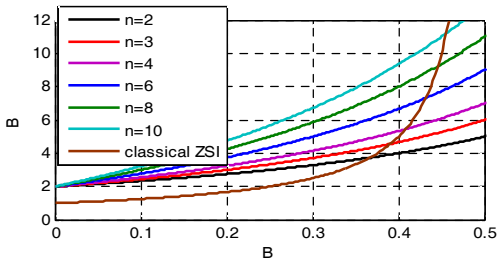
In addition, Fig. 4 shows the boost factor comparison among the classical ZSI, SL-ZSI and ESL-Γ-ZSI. In Fig. 4, through adjusting the number of inductors, boost factor of ESL-Γ-ZSI can be larger than that of SL-ZSI and the classical ZSI with short shoot-through zero state. Average value for boost factor change rate of ESL-Γ-ZSI is far less than that of SL-ZSI and the classical ZSI. This characteristic makes the boost fa ctor change of ESL-Γ-ZSI is not very large, when the shoot-through duty ratio is changed. This characteristic also makes the control of ESL-Γ-ZSI is easier than that of SL-ZSI and the classical ZSI, when the shoot-through duty ratio is near 0.3 for SL-ZSI and near 0.5 for the classical ZSI.

Capacitor voltage stress comparison is described in Fig. 5. In ESL-Γ-ZSI, capacitor voltage stress is a constant $2V_{dc}$ in 0<D<1. But capacitor voltage stress is increased with the increasing of boost factor or shoot-through duty ratio in SL-ZSI and the classical ZSI.

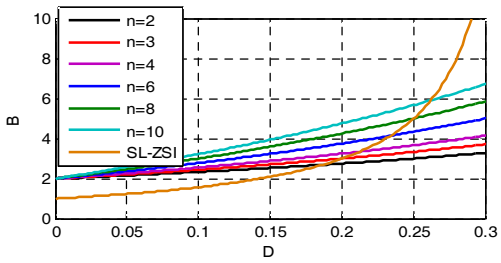
Fig. 6 shows the inductor current stress in the classical ZSI, ESL-Γ-ZSI and SL-ZSI. In Fig. 6(a), it shows the inductor current stress of ESL-Γ-ZSI and SL-ZSI. The inductor current stress of ESL-Γ-ZSI is increased with the increasing of shoot-through duty ratio and the increasing of the number of inductors. Comparing Fig. 4(b) and Fig. 6(a),

**Table 1.** Stress comparison in the case of the same $d$ and $v_d$

| | ESL-Γ-ZSI | SL-ZSI | The classical ZSI |
|---|---|---|---|
| $B$ | $\frac{2+(n-1)D}{1-D}$ | $(1+\mathrm{D})/(1-3\mathrm{D})$ | $1/(1-2\mathrm{D})$ |
| $V_c$ | $2V_{dc}$ | $(1+\mathrm{D})V_{dc}/(1-3\mathrm{D})$ | $\frac{1-\mathrm{D}}{1-2\mathrm{D}}V_{dc}$ |
| $I_l$ | $\frac{2+(n-1)D}{R_l}V_{dc}$ | $\frac{(1-\mathrm{D})(1+\mathrm{D})}{(1-3\mathrm{D})}\frac{V_{dc}}{R_l}$ | $\frac{(1-\mathrm{D})}{(1-2\mathrm{D})}\frac{V_{dc}}{R_l}$ |
| $I_L$ | $\frac{2+(n-1)D}{1-D}\frac{V_{dc}}{R_l}$ | $\frac{(1-\mathrm{D})^2(1+\mathrm{D})}{(1-3\mathrm{D})^2}\frac{V_{dc}}{R_l}$ | $\frac{(1-\mathrm{D})^2}{(1-2\mathrm{D})^2}\frac{V_{dc}}{R_l}$ |




(a)




(b)

**Fig. 4.** Boost factor curves for ESL-Γ-ZSI under different n, SL-ZSI and the classical ZSI

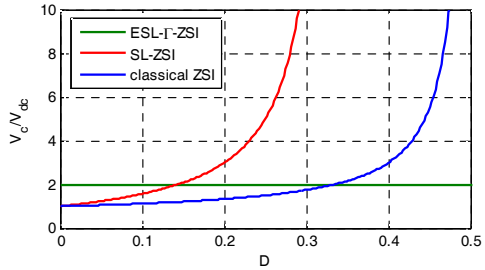
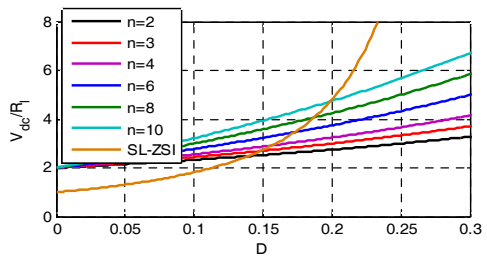


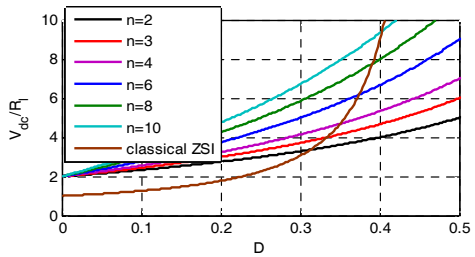

**Fig. 5.** Capacitor voltage stress for ESL-Γ-ZSI, SL-ZSI and the classical ZSI

the inductor current stress of ESL-Γ-ZSI is smaller than that of SL-ZSI, when the boost factor is equal to each other. Table 2 shows the inductor current stress comparison between ESL-Γ-ZSI and SL-ZSI, when the boost factor is equal to each other.

Comparing Fig. 4(a) and Fig. 6(b), the inductor current stress of ESL-Γ-ZSI is also smaller than that of the classical ZSI, when the boost factor is equal to each other. Table 3 shows the inductor current stress comparison between ESL-Γ-ZSI and the classical ZSI, when the boost factor is also equal to each other.




(a)




(b)

**Fig. 6.** Inductor current stress comparison between ESL-Γ-ZSI under different n, SL-ZSI, and the classical ZSI

**Table 2.** Inductor current stress comparison between ESL-Γ-ZSI and SL ZSI

| Voltage gain | D | L-ZSI($I_L/(\frac{V_{dc}}{R_l})$) | | | | | SL-ZSI ($I_L/(\frac{V_{dc}}{R_l})$) |
|---|---|---|---|---|---|---|---|
| | | n=2 | n=4 | n=6 | n=8 | n=10 | |
| 2.69 | 0.19 | 2.69 | | | | | 4.03 |
| 3.35 | 0.21 | | 3.35 | | | | 5.74 |
| 4.14 | 0.23 | | | 4.15 | | | 8.14 |
| 5.00 | 0.25 | | | | 5.00 | | 11.25 |
| 5.91 | 0.26 | | | | | 5.91 | 15.05 |

**Table 3.** Inductor current stress comparison between ESL-Γ-ZSI and the classical ZSI

| Voltage gain | D | L-ZSI($I_L/\frac{V_{dc}}{R_l}$) | | | | | The classical ZSI ($I_L/\frac{V_{dc}}{R_l}$) |
|---|---|---|---|---|---|---|---|
| | | n=2 | n=4 | n=6 | n=8 | n=10 | |
| 3.73 | 0.37 | 3.73 | | | | | 5.60 |
| 5.45 | 0.41 | | 5.45 | | | | 10.39 |
| 7.32 | 0.43 | | | 7.32 | | | 17.31 |
| 9.24 | 0.45 | | | | 9.24 | | 26.23 |
| 11.19 | 0.46 | | | | | 11.19 | 37.12 |

## 3.2 Power loss analysis and comparison

In order to simplify analysis, we just consider the parasitic resistance of inductor, the parasitic resistance of capacitor, and the forward conduction loss of diode. The parasitic resistance of inductor, the parasitic resistance of capacitor, and forward conduction loss of diode are the same in ESL-Γ-ZSI and Cuk converter. The impact of the parasitic resistances and the forward voltage drop of diodes on the current is also ignored.

### *3.2.1 Nonshoot-through state power loss of ESL-Γ-ZSI*

Fig. 7(a) describes the equivalent circuit of ESL-Γ-ZSI under considering the power loss, and the power loss is

$$P_1 = (n+1)[(1-D)I_L]^2R_r + (n-1)(1-D)I_LV_f + [(1-D)I_L]^2r_r \quad (15)$$

where $R_r$ is the parasitic resistance of inductor; $r_r$ is the parasitic resistance of capacitor; $V_f$ is the forward voltage drop of diode.

### *3.2.2 Shoot- through state power loss of ESL-Γ-ZSI*

In this mode, the equivalent circuit of ESL-Γ-ZSI is described in Fig. 7(b), and the power loss is

$$P_2 = n(DI_L)^2R_r + [1+(2n-1)D]I_LV_f + [(1-D)I_L]^2R_r + [(1-D)I_L]^2r_r \quad (16)$$

So, the power loss of ESL-Γ-ZSI under the step- up mode is

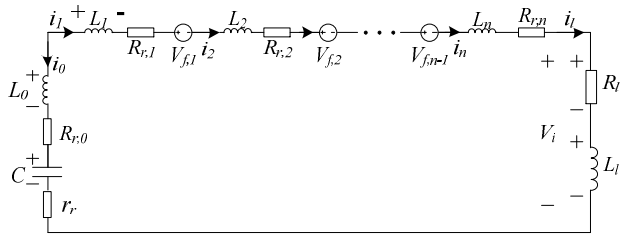
$$\begin{aligned} P_3 = P_1 + P_2 &= R_r\left(\frac{V_{dc}}{R_l}\right)^2[2+(n-1)D]^2 \\ &\left[\frac{nD^2}{(1-D)^2}+n+2\right] + 2r_r\left(\frac{V_{dc}}{R_l}\right)^2[2+(n-1)D]^2 \\ &+\frac{n(1+D)[2+(n-1)D]}{1-D}\frac{V_fV_{dc}}{R_l} \\ &= A1\left(\frac{V_{dc}}{R_l}\right)^2R_r + B_1\left(\frac{V_{dc}}{R_l}\right)^2r_r + C_1\frac{V_fV_{dc}}{R_l} \end{aligned} \quad (17)$$

When the ESL-Γ-ZSI works in step- down mode, the equivalent circuit of ESL-Γ-ZSI, in steady state, is described in Fig. 8. And the power loss is

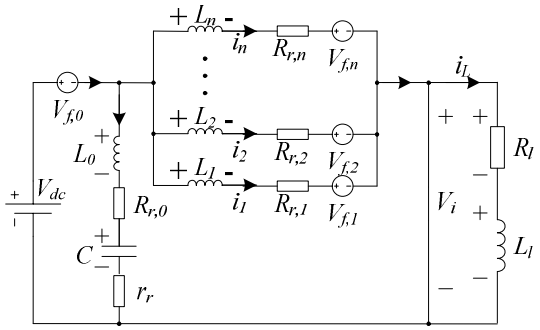
$$P_4 = \frac{V_{dc}-nV_f}{nR_r+R_l}nV_f + \left(\frac{V_{dc}-nV_f}{nR_r+R_l}\right)^2nR_r \quad (18)$$

Assuming $V_f$ is far less than $V_{dc}$, $R_r$ is far less than $R_l$, and n is a small constant, (18) can be simplified as follows

$$\begin{aligned} P_5 &= \frac{V_{dc}}{R_l}nV_f + \left(\frac{V_{dc}}{R_l}\right)^2nR_r \\ &= A_2\left(\frac{V_{dc}}{R_l}\right)^2R_r + C_2\frac{V_fV_{dc}}{R_l} \end{aligned} \quad (19)$$



(a) nonshoot-through state



(b) shoot-through state

**Fig. 7.** Operating states for ESL-Γ-ZSI under step-up state and considering power loss

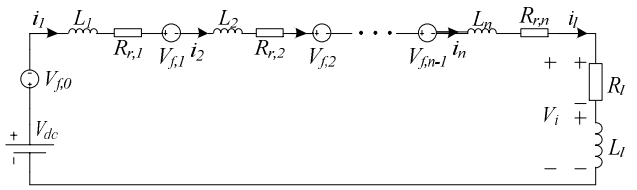


**Fig. 8.** Operating states for ESL-Γ-ZSI under step-down state and considering power loss

### *3.2.3 Power loss analysis for cuk converter*

Cuk converter has two working modes and the boost factor is D′/(1-D′) [25]. In the first working mode as shown in Fig. 9(a), ignoring the loss of switching device, the power loss is

$$P_6 = (D'I_1)^2 R_r + (D'I_2)^2 (R_r + r_r) \tag{20}$$

where D′ is the duty ratio of switching device in Cuk converter.

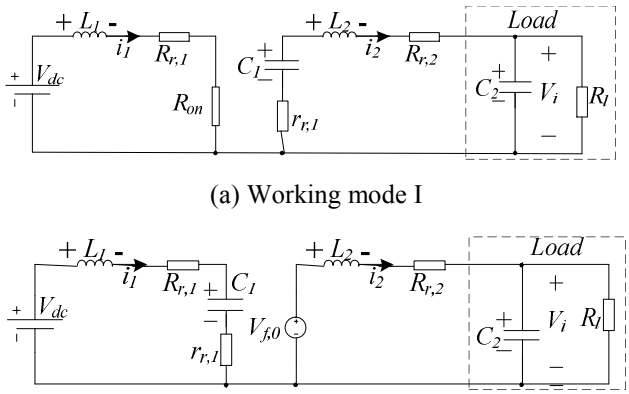
In the second working mode as shown in Fig. 9(b), the power loss is

$$P_7 = [(1-D')I_1]^2 (R_r + r_r) + V_f (1-D') I_2 + [(1-D')I_2]^2 R_r \tag{21}$$

In Cuk converter,

$$I_1 = \left(\frac{D'}{1-D'}\right)^2 \frac{V_{dc}}{R_l} \tag{22}$$

$$I_2 = -\frac{D'}{1-D'} \frac{V_{dc}}{R_l} \tag{23}$$



(a) Working mode I



(b) Working mode II

**Fig. 9.** The equivalent circuit for Cuk converter

So, the power loss of Cuk converter is obtained from (20)~ (23).

$$P_8 = \left[\frac{D'^6}{(1-D')^4} + \frac{2D'^4}{(1-D')^2} + D'^2\right]\left(\frac{V_{dc}}{R_l}\right)^2 R_r + \frac{2D'^4}{(1-D')^2}\left(\frac{V_{dc}}{R_l}\right)^2 r_r + \frac{D'V_f V_{dc}}{R_l} = A_3\left(\frac{V_{dc}}{R_l}\right)^2 R_r + B_3\left(\frac{V_{dc}}{R_l}\right)^2 r_r + C_3 \frac{V_f V_{dc}}{R_l} \tag{24}$$

### *3.2.4 Power loss comparison*

Fig. 10 shows the power loss curves for Cuk converter and ESL-Γ-ZSI.

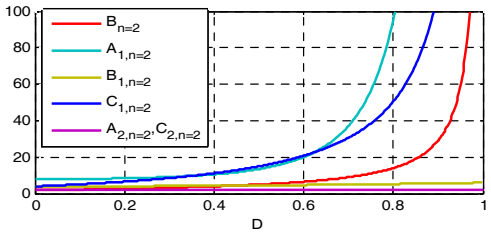
In Fig. 10, we can see the power loss of ESL-Γ-ZSI is increased with the increasing number of inductors and diode and the increasing of shoot- through duty ratio. In addition, the boost factor is also increasing with the increasing number of inductor and diode and the increasing of shoot- through duty ratio. So, in order to contain a better cost performance, we should consider the boost factor and power loss at the same time.

In step- up mode and under the same boost factor, we can know, from Fig. 10, the power loss of $R_r$ in ESL-Γ-ZSI is lower than that of Cuk converter, the power loss of $r_r$ in ESL-Γ-ZSI is also lower than that of Cuk converter. However, the power loss of diode in ESL-Γ-ZSI is larger than that of Cuk converter.

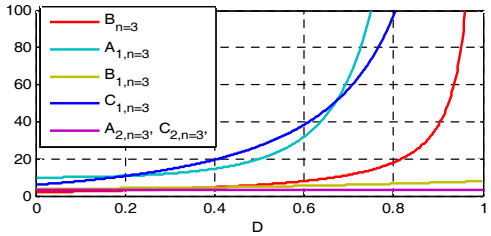
When the working mode is step- down as shown in Fig. 10, the power loss of $R_r$ in ESL-Γ-ZSI is larger than that of Cuk converter and the power loss of diode in ESL-Γ-ZSI is also larger than that of Cuk converter. But power loss of $r_r$ in Cuk converter is larger than that in ESL-Γ-ZSI.

## 3.3 Inrush current and voltage overshoot analysis

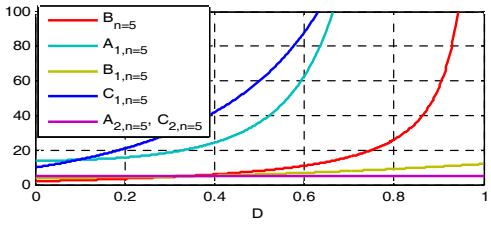
The Z-source impedance network is the energy storage and filtering element for the ZSI. The purpose of the inductors is to limit the current ripples through the devices during boost mode with the shoot-through state. Moreover,



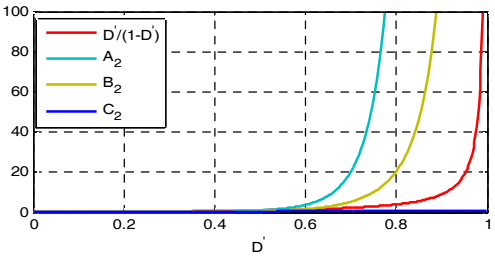

(a) Power loss of ESL-Γ-ZSI under n=2




(b) Power loss of ESL-Γ-ZSI under n=3




(c) Power loss of ESL-Γ-ZSI under n=5




(d) Power loss of Cuk converter

**Fig. 10.** Power loss comparison between ESL-Γ-ZSI and Cuk converter.

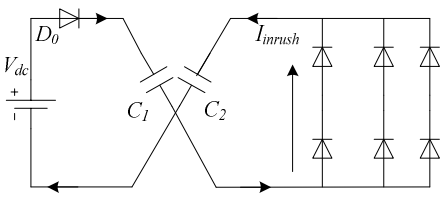



**Fig. 11.** Startup equivalent circuit for the classical ZSI and SL-ZSI.

the purpose of the capacitors is to absorb the current ripples and maintain a constant voltage to keep the ac output voltage sinusoidal.

In the classical Z-source impedance network and SL Z-source impedance network, there are two capacitors which cause the problem of inrush current and voltage overshoot

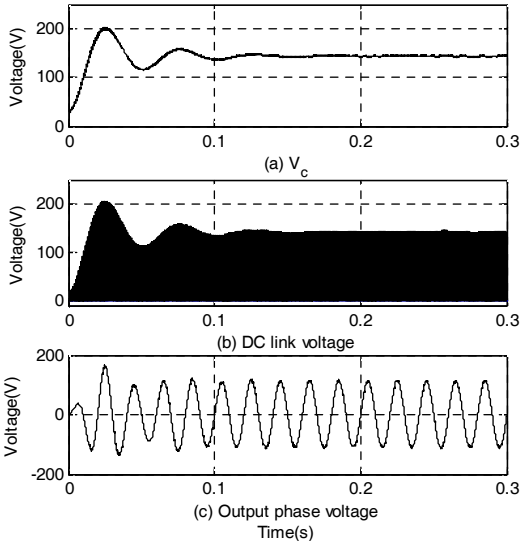



**Fig. 12.** Simulation results using maximum boost control for SL-ZSI under M = 0.8 and D=0.2.

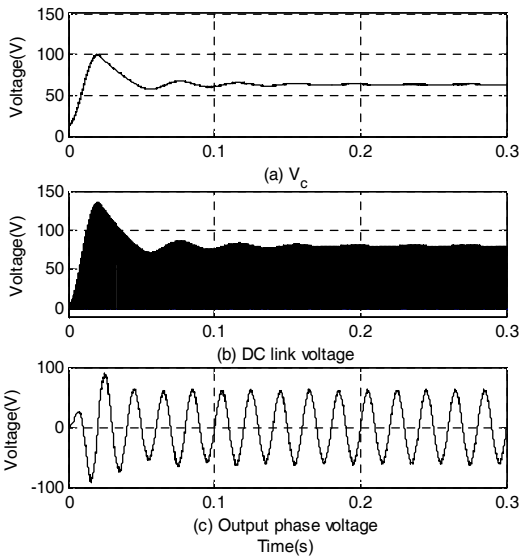



**Fig. 13.** Simulation results using maximum boost control for the classical ZSI under M = 0.8 and D=0.2.

at startup. Startup equivalent circuit for the classical ZSI and SL-ZSI is shown in Fig. 11. The initial voltage across the Z-source capacitors is zero, huge inrush current flows to the diode $D_0$, and the Z-source capacitors are immediately charged to $V_{dc}/2$. Then, the Z-source inductors and capacitors resonate, generating the current and voltage spikes. This phenomenon will result in a large harmonic content and voltage overshoot in the dc link voltage and output ac voltage, increase voltage ratings of all the components, and result in long transition process, as shown in Figs. 12 and Fig. 13.

In addition, the peak dc-link voltage will change when there is a step change in the input voltage or undesired interference though $V_c$ keeps constant. This phenomenon will also result in the output voltage overshoot.

In ESL-Γ-Z-source impedance network, there is no loop for inrush current at startup as shown in Fig. 2, and the proposed topology provides inrush current suppression and improves the transition process. But there is still inrush current in ESL-Γ-ZSI, and the analysis is as follows.

At startup, the initial voltage across the Z-source capacitor is zero, and $C_0$ is charged by $V_{dc}$ through $L_0$. When the Z-source capacitor is charged to near $V_{dc}$ and the shoot-through state is coming, the resonance of the ESL-Γ-Z-source inductors and capacitor is happening, and the inrush current in the proposed ESL-Γ-ZSI is appeared. This problem can be improved by adopting soft start method which is not discussed in this paper. But, the inrush current of the proposed ESL-Γ-ZSI is lower than that of SL-ZSI and the classical ZSI, the problem of voltage overshoot is improved, and the transition process is shortened.

However, if the ESL-Γ-Z-source impedance network works in DCM mode, the dc link voltage is increasing infinitely, the output voltage will be uncontrollable and the system is unstable. In order to avoid the problem causing by the DCM mode, a snubber circuit is introduced as shown in Fig. 14.

A group of capacitor and resistance combination, which capacitor $C_s$ and resistance $R_s$ are in series, is right across PN of the inverter bridge. In Fig. 14, if the current to the inverter is in DCM mode, the snubber circuit provides an absorbing path for the inductor current. In addition, the snubber circuit can absorb a part of high frequency inductor current in normal operation and a part of inrush current at startup. Moreover, if the dc link voltage which is disturbed by other undesired interference has a step change, the snubber circuit provides an extra absorbing path for the extra current, and helps to reduce the overshoot voltage across the device. Fig. 15 shows the simulation results for ESL-Γ-ZSI under n=2, M=0.7 and D=0.3.

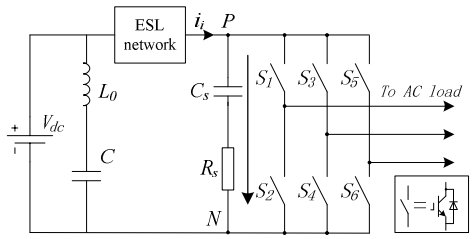



**Fig. 14.** Snubber circuit for ESL-Γ-ZSI

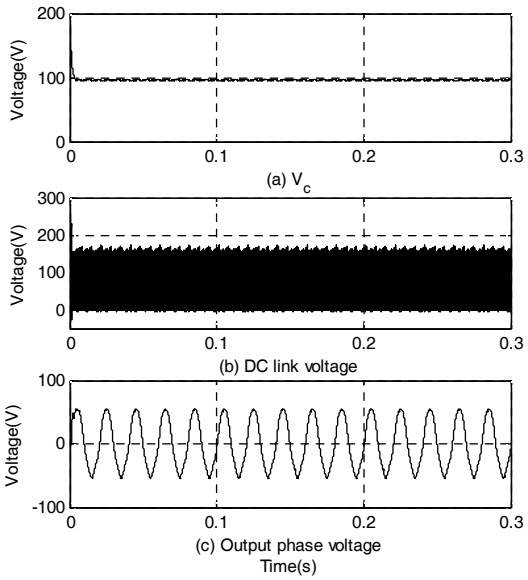



**Fig. 15.** Simulation results for ESL-Γ-ZSI under n=2, M=0.7 and D=0.3.

## 4. Simulation and Experimental Results

To verify the aforementioned theoretical results, two simulation examples and two experimental examples for ESL-Γ-ZSI are given. Matlab/Simulink is used to realize the simulation, and a prototype has been constructed with IPM (Intelligent Power Module) devices and dsPIC6010A as main controller. In the simulation and experiment, maximum boost control method is adopted [8], and the system parameters are shown in Table 4.

**Table 4.** System parameters

| | | | |
|---|---|---|---|
| $L_1$= $L_2$= $L_3$= $L_4$ =L | 47μH | C | 1000μF |
| $L_f$ | 1mH | $C_f$ | 22μF |
| Switching frequency | 10 kHz | $R_l$ | 10 Ω |
| $R_s$ | 20k | $C_s$ | 0.1uF/1000V |

### 4.1 Simulation result I

This example is the voltage inversion from dc 48 V to ac 37.3Vrms and n=2.

Assuming D=0.2 and M=0.8, B=2.75 and (25) can be concluded.

$$v_p = M\,B\frac{V_{dc}}{2} = 52.8V \tag{25}$$

(25) is the phase peak voltage, which implies that the line-to-line voltage is 64.7Vrms or 91.4 V peak. Fig. 16 shows the simulation results.

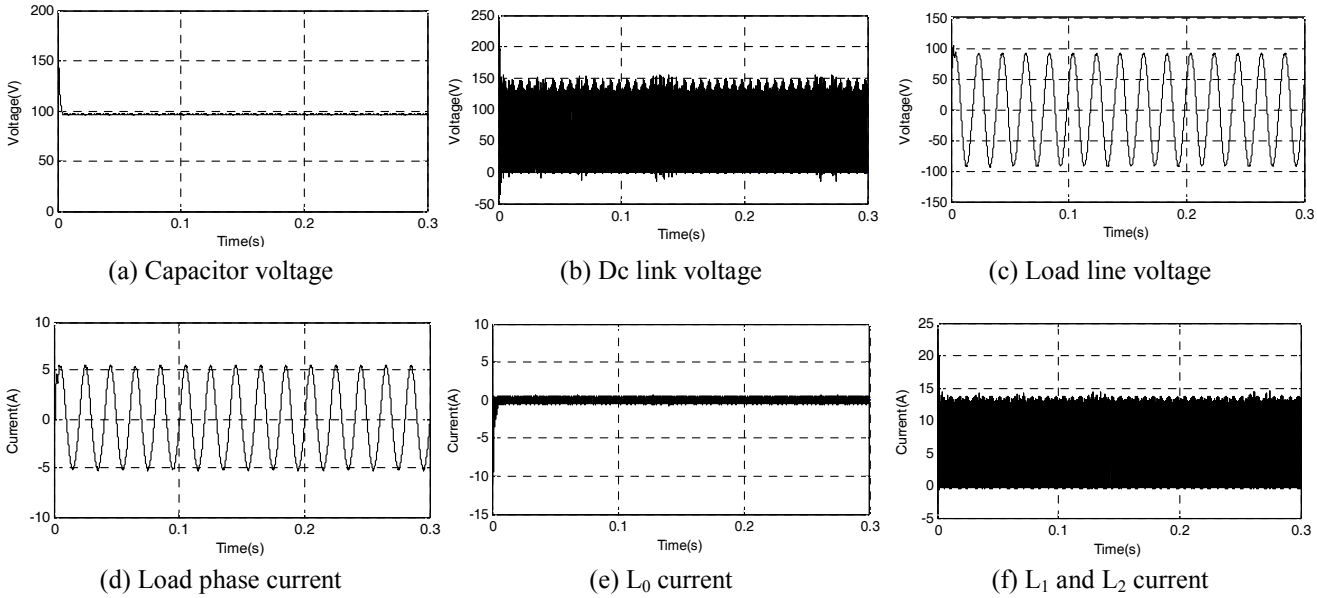
### 4.2 Simulation result II

This example is the voltage inversion from dc 48 V to ac 39Vrms and n=2. Assuming D=0.3 and M=0.7, B=3.29 and (26) can be concluded.

$$v_{ac} = M\,B\frac{V_{dc}}{2} = 55.3V \tag{26}$$

(26) is the phase peak voltage, which implies that the line-to-line voltage is 67.7Vrms or 95.7V peak. Fig. 17 shows the simulation results.

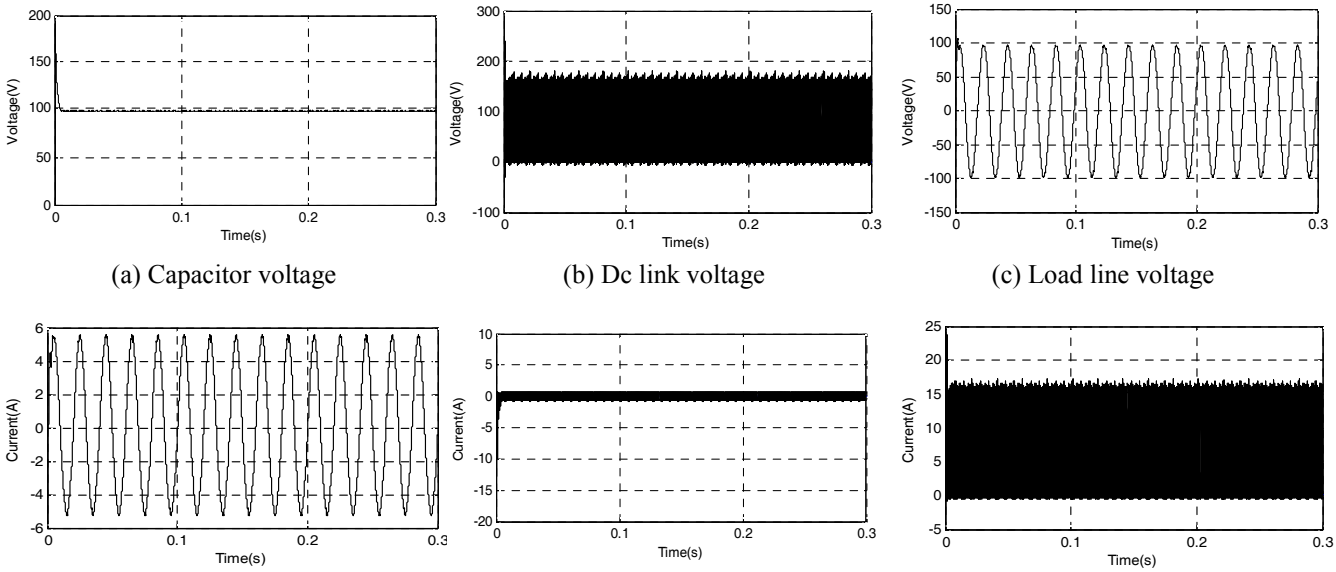
From Figs. 16 and Fig. 17, we can see that, in the steady state, capacitor voltages are boosted to 96V; the output ac




(a) Capacitor voltage (b) Dc link voltage (c) Load line voltage

(d) Load phase current (e) $L_0$ current (f) $L_1$ and $L_2$ current

**Fig. 16.** Simulation results under n=2, D=0.2 and M=0.8




(a) Capacitor voltage (b) Dc link voltage (c) Load line voltage

(d) Load phase current (e) $L_0$ current (f) $L_1$ and $L_2$ current

**Fig. 17.** Simulation results under n=2, D=0.3 and M=0.7

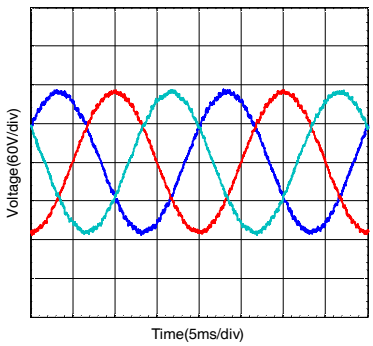
voltages are 91.4V peak and 95.7V peak, respectively; the output ac currents are 5.28A peak and 5.53A peak, respectively; the average currents of $L_0$ are close to zero; the inductor currents of SL cells are near 13A and 16A, respectively; the DC link voltages are near 130V and 160V, respectively.

There is inrush current which is appeared at startup and the inrush current is caused by the resonance of the ESL-Γ-Z-source inductors and capacitor. This phenomenon causes the voltage overshoot in capacitor voltage, dc link voltage, and output ac voltage. As shown in Figs. 16 and Fig. 17, the capacitor voltages are immediately charged from 0V to 145V and 160V, respectively; the currents of $L_0$ are decreased from 0A to -9A and -10A, respectively; the inductor currents of SL cells are increased from 0A to 20A and 24A, respectively; the DC link voltages are increased from 0V to 200V and 250V, respectively. However, the inrush current and the voltage overshoot are not very large, the response speed of system is very fast, and the transient process is less than 10ms.

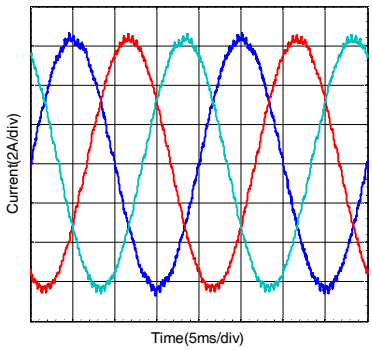
### 4.3 Experimental result I

This example is the voltage inversion from dc 48 V to ac 44.1Vrms and n=4.

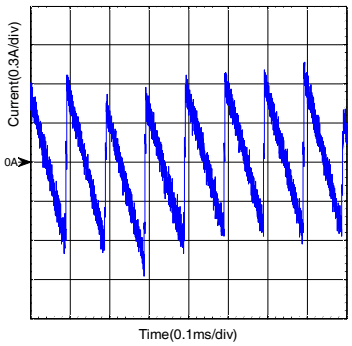
Assuming $D = 0.2$ and $M = 0.8$, $B = 3.25$ and (27)



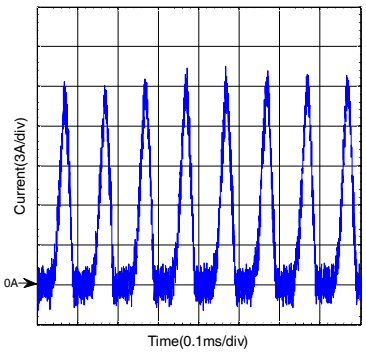

(a) Load line voltage



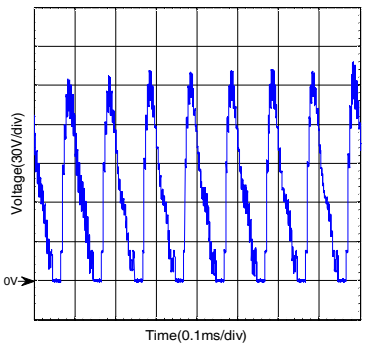

(b) Load phase current



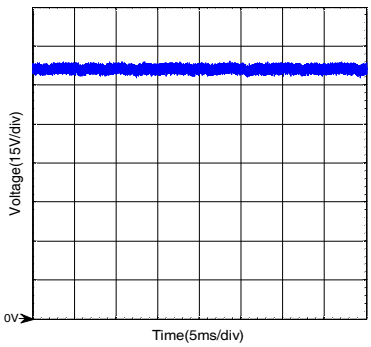

(c) $L_0$ current




(d) $L_1$ and $L_2$ current

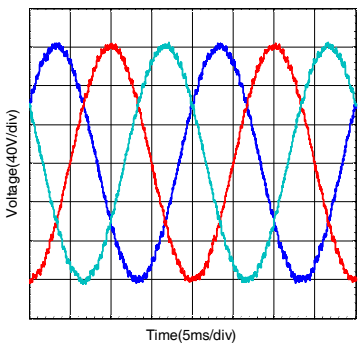



(e) DC link voltage

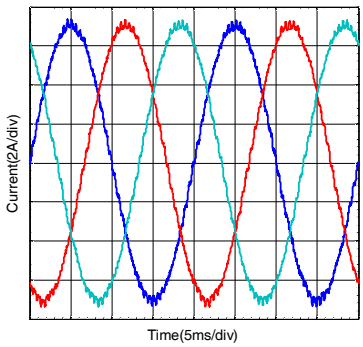



(f) Capacitor voltage

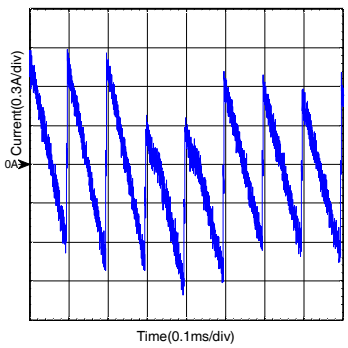
**Fig. 18.** Experimental results I.



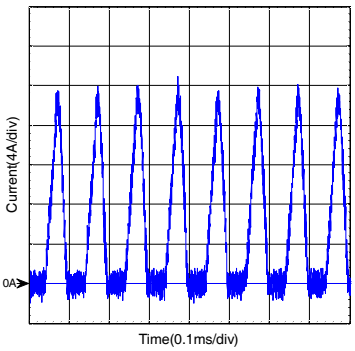

(a) Load line voltage



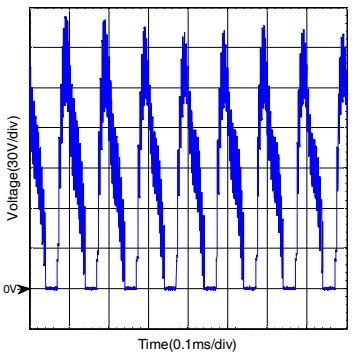

(b) Load phase current



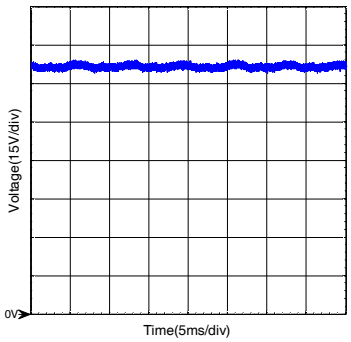

(c) $L_0$ current




(d) $L_1$ and $L_2$ current




(e) DC link voltage




(f) Capacitor voltage

**Fig. 19.** Experimental results II.

can be concluded.

$$v_p = M\,B\frac{V_{dc}}{2} = 62.4V \quad (27)$$

(27) is the phase peak voltage, which implies that the line-to-line voltage is 76.4Vrms or 108 V peak as shown in Fig. 18.

### 4.4 Experimental result II

This example is the voltage inversion from dc 48 V to ac 49.2Vrms and n=4.

Assuming D=0.3 and M=0.7, B=4.14 and (28) can be concluded.

$$v_p = M\,B\frac{V_{dc}}{2} = 69.6V \quad (28)$$

(28) is the phase peak voltage, which implies that the line-to-line voltage is 85.2Vrms or 120.5 V peak as shown in Fig. 19.

From Figs. 18 and Fig. 19, it can be seen that, in the steady state, capacitor voltages are boosted to 96V; the output ac voltages are 108V peak and 120.5V peak, respectively; the output ac currents are 6.24A peak and 6.96A peak, respectively; the average currents of $L_0$ are close to zero; the inductor currents of SL cells are near 16A and 20A, respectively; the DC link voltages are near 160V and 200V, respectively.

All the simulation and experimental results are quite consistent with the theoretical analysis results. The operating characteristic of ESL-Γ-ZSI is therefore validated.

## 5. Conclusion

This paper has presented a novel ESL-Γ-ZSI by improving the existing traditional Z-source impedance network. The proposed inverter employs a unique Γ shape Z source network and extended SL network to couple the low dc voltage energy source to the main circuit of the inverter. In ESL-Γ-ZSI, the capacitor voltage stress is a constant $2V_{dc}$ avoiding the disadvantage that capacitor voltage stress is increased with the increase of shoot-through duty ratio in the classical Z source inverter and SL-ZSI.

ESL-Γ-ZSI provides an extended SL network in front of the inverter bridge, so there is no inrush current flowing to the main circuit at startup. The inverter can increase the boost factor through adjusting shoot-through duty ratio and increasing the number of inductors. The inductor current stress of ESL-Γ-ZSI is smaller than that of SL-ZSI and the classical ZSI, when the boost factor is equal to each other.

Both the simulation and experimental results demonstrate its advantages. Therefore, the proposed inverter could be widely used in the engineering applications using impedance-type power inverters.

## Acknowledgements

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**Lei Pan** He is a lecturer of Tianjin Chengjian University and is currently pursuing the Ph.D. degree at HeBei University of Technology, Tianjin. His research interests are power converters and motor drives.

**Hexu Sun** He received the Ph.D. degrees from Northeastern University, Liaoning, China, in 1993. He is currently a Professor of HeBei University of Technology and an IEEE Senior Member. His research interests include power electronics for utility applications, electric motors, distributed power generation and the control for engineering system.