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Chopper Controller Based DC Voltage Control Strategy for Cascaded Multilevel STATCOM

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Abstract – The superiority of CMI (Cascaded Multilevel Inverter) is unparalleled in high power and high voltage STATCOM (Static Synchronous Compensator). However, the parameters and operating conditions of each individual power unit composing the cascaded STATCOM differ from unit to unit, causing unit voltage disequilibrium on the DC side. This phenomenon seriously impairs the operation performance of STATCOM, and thus maintaining the DC voltage balance and stability becomes critical for cascaded STATCOM. This paper analyzes the case of voltage disequilibrium, combines the operation characteristics of the cascaded STATCOM, and proposes a new DC voltage control scheme with the advantages of good control performance and stability. This hierarchical control method uses software to achieve the total active power control and also uses chopper controllers to enable that the imbalance power can flow among the capacitors in order to keep DC capacitor voltages balance. The operating principle of the chopper controllers is analyzed and the implementation is presented. The major advantages of the proposed control strategy are that the number of PI regulators has been decreased remarkably and accordingly the blindness of system design and debugging also reduces obviously. The simulation reveals that the proposed control scheme can achieve the satisfactory control goals.

Keywords: STATCOM, Voltage disequilibrium, Voltage balancing, Chopper controller, Hierarchical control

1. Introduction

Cascaded STATCOM is characterized by large voltage levels, small harmonic current, high system efficiency, small and few passive components and ease of expansion [1-3], and hence leading the trend of FACTS (Flexible Alternative Current Transmission Systems) technology development [4]. Moreover, it's an effective way to solve the power quality problems in high voltage and high power applications. Therefore, it has attracted widespread attention both in academic and industrial fields [5].

In cascaded STATCOM, due to the 3-phase unbalance compensation and the differences in component parameters and working states, different power units will receive or send different amount of active power, which results in voltages rising in the DC link of some power units and dropping in other units. This is known as the DC voltage unbalance [6-8]. The good performance of the device and the current control strategies are all based on the perfect consistency of the power units. Maintaining the voltage stability and balance is the basis for cascaded STATCOM to operate safely and reliably for a long time. Thus, the research on reducing the DC voltage unbalance is extremely essential [9].

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Currently, the DC link voltage control strategies fall into two categories [7]. One refers to the hardware-based methods, such as the control method by paralleling resistors [10], the balancing method by energy exchanging on AC line [11], the balancing method by energy exchanging on DC line [10-13], and the control strategy based on the unity-power-factor (UPF) 4-quadrant VSR [13]. These approaches almost employ the same hardware devices like PWM rectifiers [5, 13], diode bridges, or combination of inverters and isolated transformers [10, 12]. Through these hardware circuits adopted by the hardware-based method, the consumed energy can be compensated to maintain the balance and stability of DC capacitor voltages. The only differences among these methods lie in their topologies, sources of energy and energy flow paths.

The hardware-based methods have some merits such as fast response, small steady state error, effective voltage control, reliable and stable operation performance, and hence find the wide practical applications [10, 11]. A typical hardware method reported in [3, 12] uses the combination of a multi-winding phase shifting transformer and uncontrollable rectifiers. Ref. [14, 15] reported the 10kV/±75Mvar STATCOM produced by ALSTOM in 1999 and this famous project adopted the DC voltage balancing method by energy exchanging on AC line [11]. Ref. [16] reported that the 10kV/±50Mvar STATCOM installed at the 220KV Xijiao Substation in Shanghai in 2006 adopted the balancing method by energy exchanging on DC line

[10]. The world-famous 35kV/±200Mvar STATCOM constructed in 2011 by China Southern Power Grid Co., Ltd also adopted the balancing method by paralleling resistors controlled through PWM mode IGBTs [17].

However, the hardware-based methods require too many hardware components and have some drawbacks in weight, volume and efficiency, causing high hardware cost and inconvenience for system extension [7], although these approaches are widely applied in some world-famous projects.

Software-based methods include such approaches as the individual voltage balancing strategy based on direct voltage error [18], the balancing method based on power error regulating [19, 20], the active voltage vector superposition strategy [21], and the phase angle superposition method [22]. By using the closed-loop feedback control, the software-based methods measure the DC capacitor voltages of power units and regulate the output through the voltage error or the power error. The principal idea is to utilize pulse width modulation and phase angle modulation to regulate the charging and discharging time of power components. Consequently, these methods realize the regulation of DC link voltage and noticeably reduce the hardware cost. So, the software-based methods represent a further development trend of the DC voltage control in cascaded STATCOM.

However, for the cascaded devices with large amount of power units, these methods have to control many variables and loops. For example, the phase angle superposition method [22] uses (3N+7) PI regulators, where N is the number of power units in a phase. Control strategies in [18-21] use 3(N+1) PI regulators. However, there has been no scientific method to design the parameters of the PI regulators so far. In addition, the coupling situations for control loops increase dramatically, leading to more difficulties for controller design and system debugging [7].

Furthermore, the software-based methods are based on the traditional error control technology such as PID control and hysteresis control, which will cause a certain time delay because these methods are not effective until the error has produced and has been measured by the sensors. In addition, finding the best parameters of the PI regulators depends on the precise mathematical model the current cascaded STATCOM lacks. Therefore, it is usually difficult to find the suitable parameters for the multitudinous PI controllers employed to regulate the active/reactive current and DC voltage to achieve a satisfactory dynamic response and good robustness, as Lehn has pointed out in [23]. So in practice, the trial-and-error method is widely adopted, although it causes too much blindness in the process of system design and debugging.

Besides the common drawbacks aforementioned, some particular control methods still pose unique challenges. Ref. [19] proposed an individual voltage balancing strategy to realize independent modulation control over each power unit, in which an active component is superposed to the CMI output voltage. However, the cosine value of the current phase angle is included in the denominator [21]. Therefore, any system adopting this method is very sensitive to disturbance due to the zero-crossing point of the cosine value. Another balancing control method proposed in [20] has a disadvantage that it has poor regulation capability under small reactive current and is easily affected by the accuracy of phase-locked loop (PLL).

Generally speaking, software-based methods depend less on hardware, which lend them significant advantages in weight, volume and cost. However, they show slow response and large steady state error. The intrinsic problems of such schemes could not be eliminated. Therefore, the software-based methods are still mainly adopted by the lab researches and have not yet been applied in the high voltage and high power products for industry [7, 10]. However, almost all of the worldwide famous cascaded STATCOMs use hardware-based methods.

By considering the merits and demerits of the software-based and hardware-based methods, a new method, the chopper controller based DC voltage control strategy for cascaded STATCOM, is proposed in this paper, which is expected to possess some following qualities: 1, Good steady state performance (steady state error as small as possible), meaning the stable and balanced DC voltage; 2, Good dynamic performance, i.e. the fast response and good robustness; 3, Easy to design the control parameters and the control parameters are as few as possible. Therefore, the system will be easy to debug and produce for industry; 4, The hardware is few as possible. Thus, the volume is small and the weight and the cost are low; 5, Easy to expand and enlarge the scope of use as wide as possible.

As the proposed method possesses the good control performance inherited from the hardware methods and the hierarchical control idea inherited from the software methods, it can realize the goals of stability and reliability without any noticeable increase of hardware cost. In this paper, the principles of chopper controllers and the hierarchical control for DC voltage are given and the circuit topology is described. Emphasis is given to the operating principles of balancing circuit, working modes, generation of the driving signals. Theoretical analysis and the simulation results verify the effectiveness and practicability of the control strategy.

2. Cascaded STATCOM Based on CPS-SPWM

2.1 System configuration of cascaded STATCOM

System configuration of cascaded STATCOM is shown in Fig. 1, where u_{si}, i_{ci} and L_i (I = a, b, c) are the grid voltages, device's output currents and the linking inductors, respectively. The H-bridge inverter shown in Fig. 1 is the power unit. Its DC capacitor serves as power storage while R_{dc} is the equivalent resistance. When N power units are

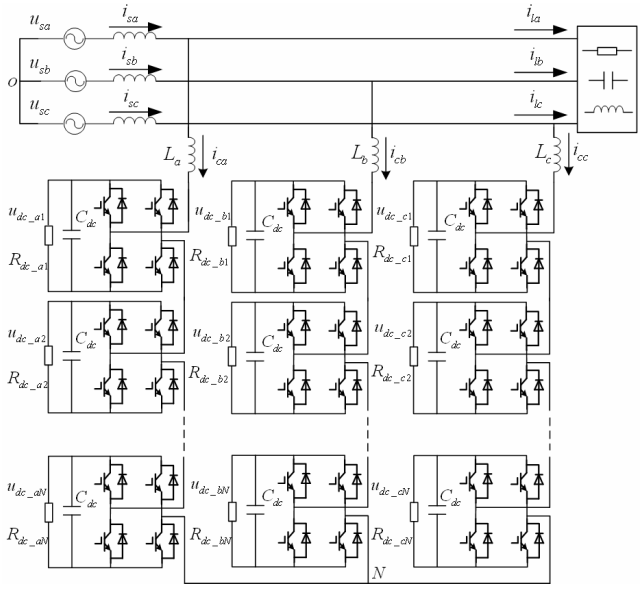


Fig. 1. Cascaded multilevel STATCOM

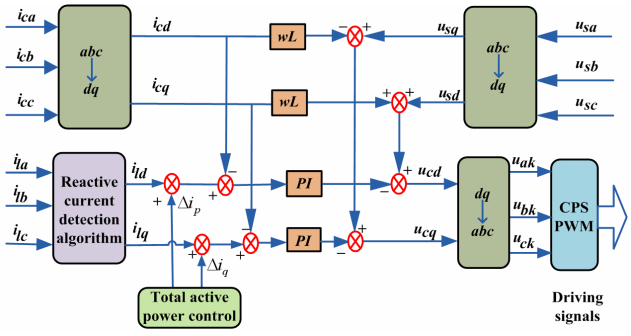


Fig. 2. System control strategy

connected in serial, the cascaded multilevel inverter is formed. The energy flowing between the STATCOM and the load is regulated through the magnitude and phase of the CMI output voltage. It is determined by the active power consumed by the device and the reactive power coming from the load [24].

2.2 System control strategy of cascaded STATCOM

Cascaded STATCOM uses the feed forward decouple control strategy [21], as shown in Fig. 2, where i_{li} (i=a, b, c) are the load currents. The modulation of the CMIs utilizes the CPS-SPWM (Carrier Phase Shifted Sinusoidal Pulse Width Modulation) technology [13], which could improve the equivalent switching frequency, reduce the harmonics, and minimize the size of passive filter components. The basic principle of the modulation technique is that all the power units of a CMI share the same sinusoid modulation signal while each unit uses carrier waves with 180^0/N degree apart according to the sequence of power units. In a power unit, the carrier waveforms for the two bridge arms are reversed. Thus the CMI in each phase could generate a maximum of 2N+1 voltage levels.

3. Chopper Controller Based Control Strategy

Chopper controller based voltage control strategy proposed in this paper consists of two layers. The upper layer is to control the total active power based on software design while the lower layer control is to balance the DC voltage of power units through chopper controllers.

3.1 Total active power control

Due to the loss (e.g. switching loss), the DC voltage of STATCOM will gradually decrease. The decrease rate is determined by the active power consumption rate. In other words, the reduction of DC voltage reflects the active power consumption by the device. Therefore, the total DC voltage drop of power units has a positive correlation with the total active power demanded by the system. With regard to the negative feedback control principle, the control algorithm of total active power (the fundamental positive sequence active power) can be derived, as shown in Fig. 3, where u_r is the voltage reference of DC capacitors and u_{dc_ai}, u_{dc_bi}, u_{dc_ci} are the DC voltages of the Power Unit i in Phase A, B and C, respectively.

Using this method to inject the power units with the active power could compensate the power loss, which leads to the DC voltage drop. When the syst achieves equilibrium, the following equation holds:

$$u_d = Nu_r \tag{1}$$

Where u_d is the equivalent DC CMI voltage.

Meanwhile, since the component parameters and the operating conditions of different power units are different, the DC voltages of power units are also not consistent. Therefore, after maintaining the DC CMI voltage at the designated value stably, we still have to rationally distribute the active power to make sure that the individual

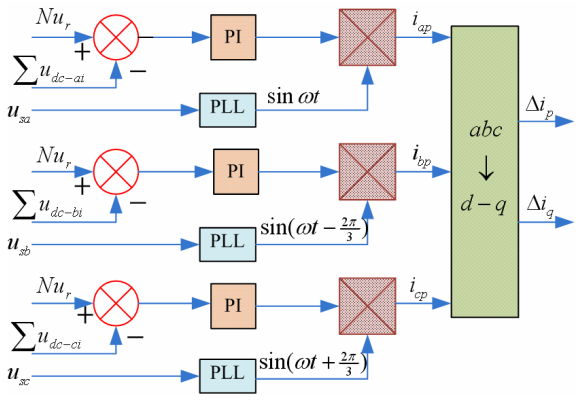


Fig. 3. Total active power control

DC capacitor voltages of power units are equal to each other. Similarly, the power units in different phases also demand different active currents, and the active power control should include the total active power control and the equilibrium control among phases. However, this effect is slight and generally negligible. In this paper, the focus is on the voltage consistency among power units. Therefore, let us assume the parameters in each phase are consistent and thus the balance control among phases is not considered.

3.2 Voltage balance control for power units

The hardware employed in this paper is depicted in Fig. 4, where diode D_1 and switch T_1 construct the path for positive power flow while D_2 and T_2 compose the path of negative power flow. Thus, the chopper circuit can realize the bidirectional power flow. The fully controlled switch could be IGBT or MOSFET which is characterized by high frequency and low voltage rating.

The connection between chopper circuits and power units is shown in Fig. 5. The DC capacitor C_1 and C_2 are connected via two chopper controllers. The chopper circuits allow the unbalanced power to flow between power units and distribute the active power to achieve voltage equilibrium, which is shown by the shadow region in Fig. 5. Actually, an extra resistor R_{extra} is added to the voltage balancing loop in series to limit the balancing current in a reasonable range.

Obviously, the employed auxiliary circuit cannot interfere with the normal operation of CMIs. In Fig. 5,

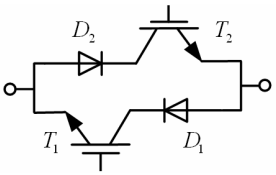


Fig. 4. Topology of chopper controller

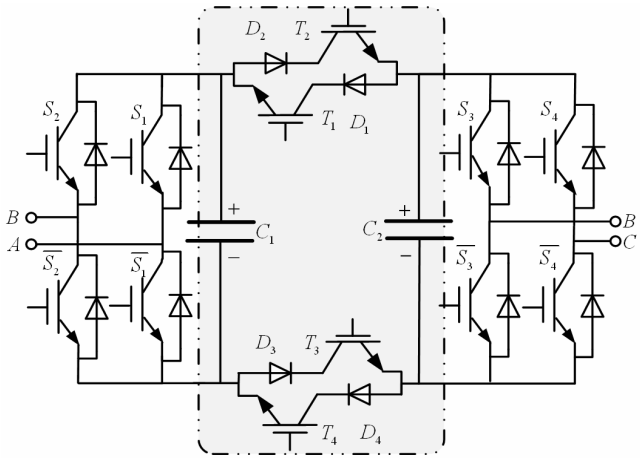


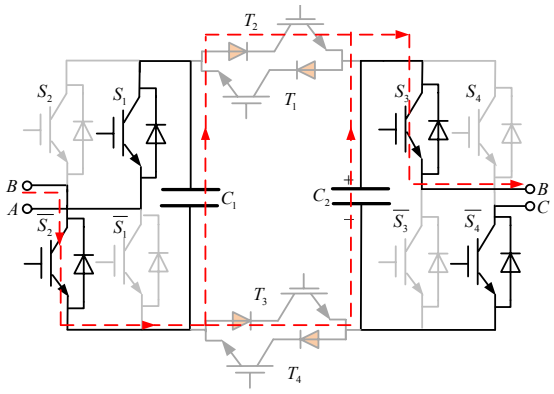
Fig. 5. Topology of units shunting by chopper controllers

switches S_1 and S_2 could operate in 4 different combination modes: 00,01,10,11. If the DC voltage of a power unit is defined as U_{dc}, the corresponding output voltage is 0, $-U_{dc}$, U_{dc}, 0. Likewise, two units connected by the chopper controllers have 16 operation modes, as shown in Fig. 6.

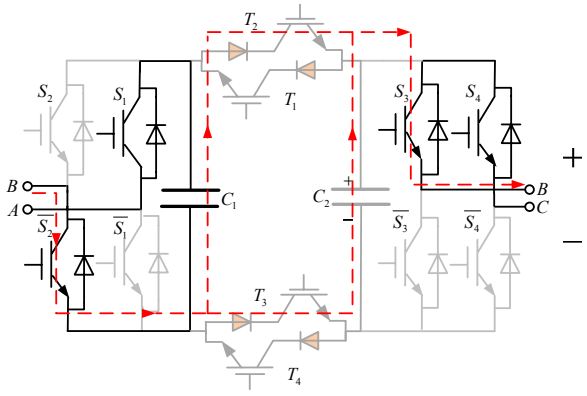
In Fig. 6(a), $S_1S_2S_3S_4$ work at the combination mode 1010, making the output voltages of these two units be U_{dc}. At this time, $\overline{S_2}$, T_2, S_3 and C_1 compose a short circuit path for circulating current. $\overline{S_2}$, T_3, S_3 and C_2 form another short circuit path which is paralleled with the previous one. These two short circuit paths will cause large current discharge of C_1 and C_2, and hence the CMI cannot operate normally. Thus, the chopper controller switch T_2T_3 must be turned off, known as the combination mode 00. As the operation states of T_1T_4 will not affect the main circuit, their combination modes could be any one of 00, 01, 10 or 11. In order to simplify the logic expression and minimize the operation errors, their combination mode is assigned to be 00. Therefore, $T_1T_2T_3T_4$ becomes 0000. Likewise, when $S_1S_2S_3S_4$ operate at the combination modes 1010, 1010, 1100, 1101, 0010, 0011, 0100 or 0101, there will be two paralleled short circuit circulation paths, shown as the regions inside the dashed lines in Fig. 6(a, b, g, h-j, o, p), respectively. At this time, $T_1T_2T_3T_4$ should work in the combination mode 0000 to avoid the short circuit.

In Fig. 6(c), $S_1S_2S_3S_4$ work in the mode 1000. There is no circulation path and turning on or off the chopper controller will not affect the operation of CMI at this time. Therefore, the chopper controllers should work in the voltage balancing state. The DC voltages of power units could be balanced through the power flow as $T_1T_2T_3T_4$ work in the combination mode 1111. Likewise, when $S_1S_2S_3S_4$ work in the modes 1000,1001,1110,1111, 0000,0001,0110 and 0111, there will be no short circuit circulation path and the chopper controllers work in the voltage balancing state, as shown in Fig. 6(c-f, k, l-n), respectively. At this time, $T_1T_2T_3T_4$ work in the mode 1111.

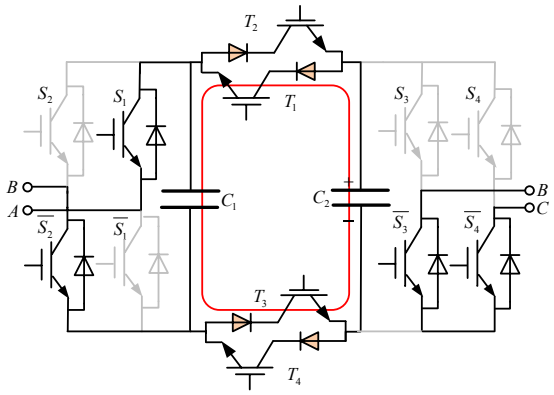
Based on the previous analysis, the working principles can be summarized as follows: 1. Switches in a pair of chopper controllers operate in the synchronous state, meaning they are on or off at the same time. 2. Chopper switch's working state is related to the switches of its adjacent power units, but not affected by the magnitude and the direction of the output current in CMIs. The switching frequency of chopper switches is two times than that of power units. 3. If there is a short circuit circulation path, the chopper controllers cannot work in the voltage balancing mode. 4. If the right arm of upper power unit has the opposite logical working condition with the left arm of the downward power unit, the short circuit circulation paths exist. 5. If a short circuit circulation path is formed, there must be another one, and these two paths are paralleled.



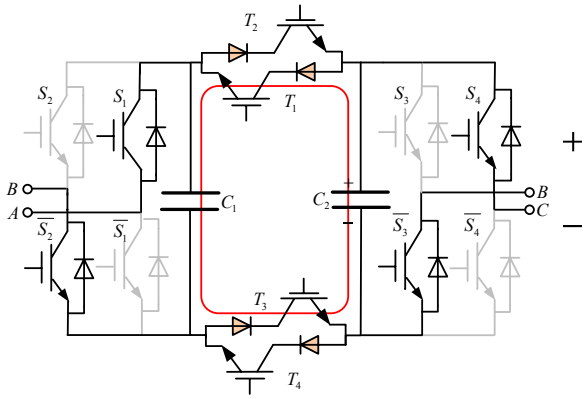
(a) Mode 1



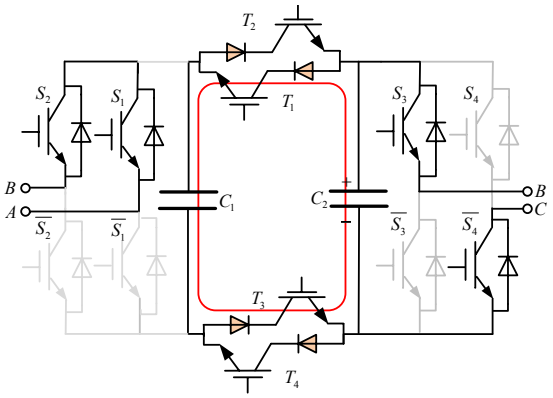
(b) Mode 2



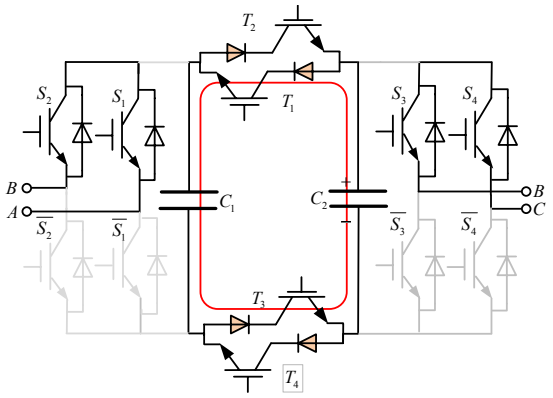
(c) Mode 3



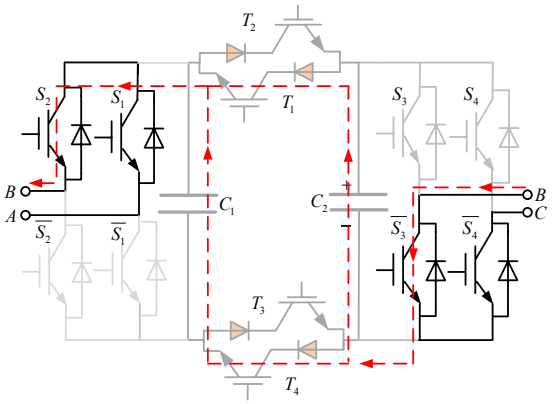
(d) Mode 4



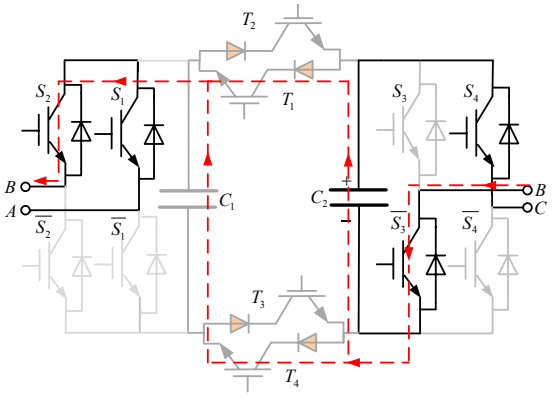
(e) Mode 5



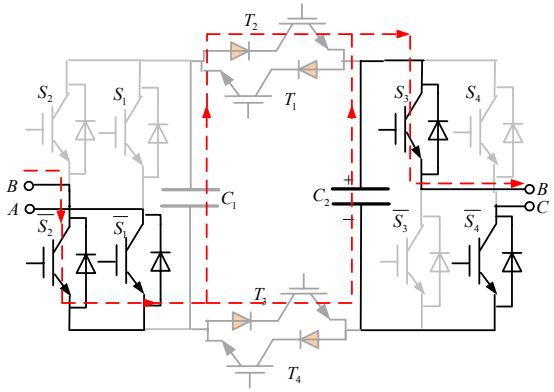
(f) Mode 6



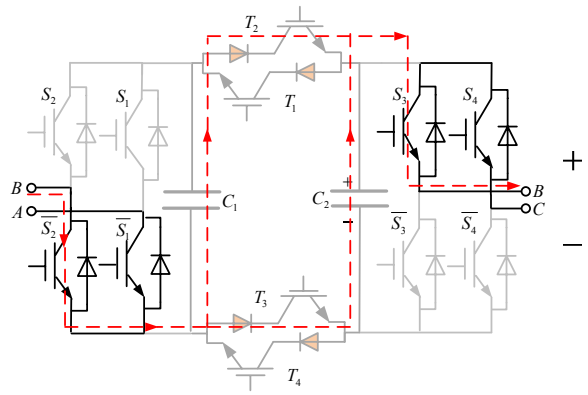
(g) Mode 7



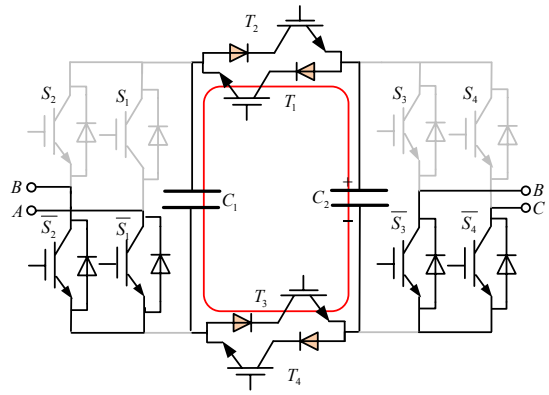
(h) Mode 8



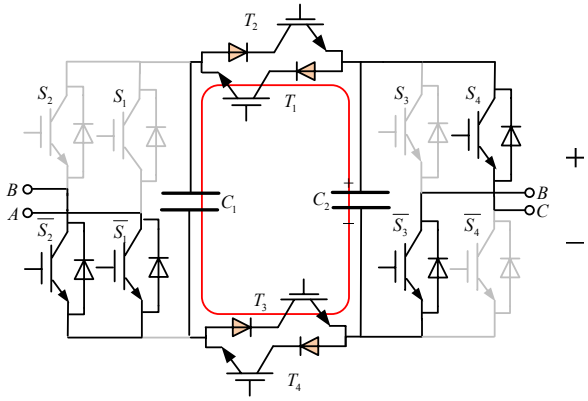
(i) Mode 9



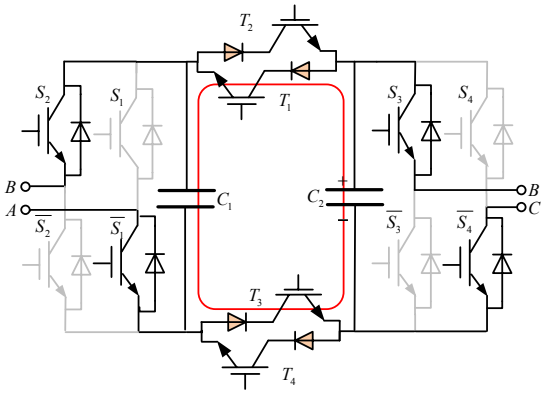
(j) Mode 10



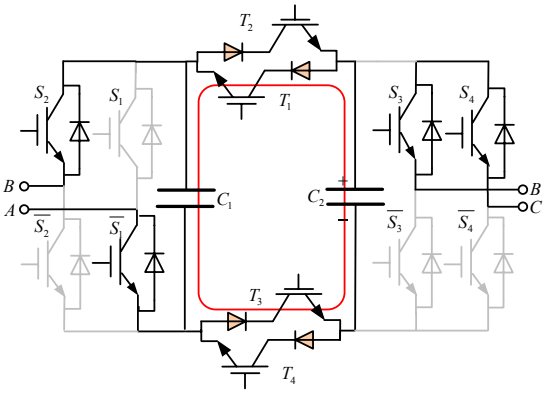
(k) Mode 11



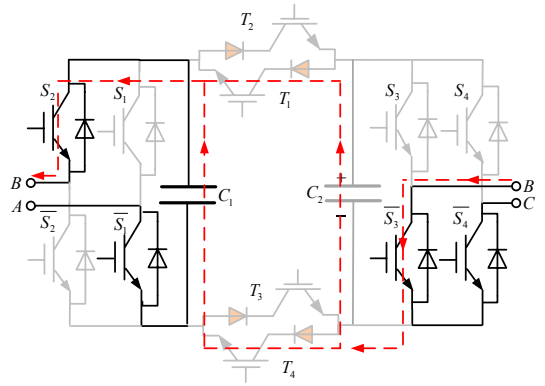
(l) Mode 12



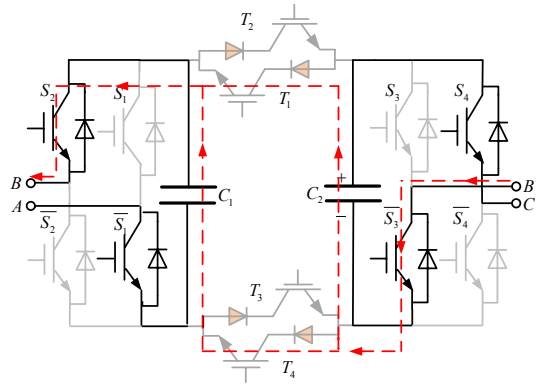
(m) Mode 13



(n) Mode 14



(o) Mode 15



(p) Mode 16

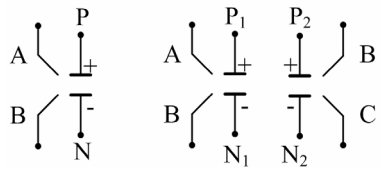
Fig. 6. Operation principle of chopper controllers

3.3 Extension to the N-Unit-Series-Connected CMI

In order to verify that the method could be extended to any amount of power units, the power unit is simplified firstly, as shown in Fig. 7(a). *A* and *B* are the midpoints of the left arm and the right arm, respectively. The points *P* and *N* represent the positive and negative poles of DC capacitor. When A connects to *P* and *B* connects to *N*, the output voltage of power unit is $+U_{dc}$. The voltage becomes $-U_{dc}$ if *A*, *N* and *B*, *P* are connected. If *A* and *B* connects simultaneously to *P* or *N*, the output voltage will be 0. Likewise, Fig. 5 could be simplified as Fig. 7(b), where the midpoint of the second power unit's left arm is connected with the midpoint of the first power unit's right arm, which is all signed by *B*.

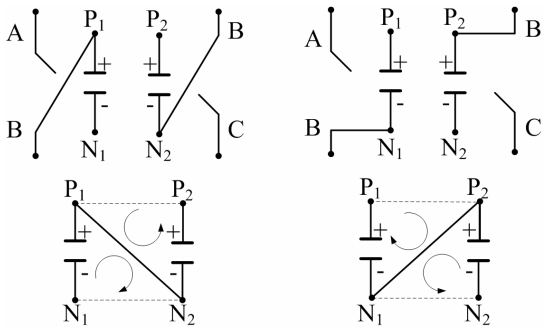
According to the simplification, the short circuit circulation path in Fig. 6 could be depicted as Fig. 8. The fourth operating principle mentioned above indicates that the existence of short circuit circulation paths should be determined by the right arm of the first power unit and the left arm of the second power unit.

If *B* is connected to N_2 and P_1 in chorus, which means P_1 connects to N_2, S_2 and S_3 must be S_2S_3=01. Therefore the first Short Circuit Circulating Mode (SCCM) also exists when $S_1S_2S_3S_4$ are X01X, where X means either 0 or 1, corresponding to the Mode 7, 8, 15, 16 in Fig. 6. At this time, the switches of chopper controllers are off and the short circuits are thus avoided. If *B* is connected to N_1 and P_2 in chorus, respectively, which means P_2 connects to N_1, S_2 and S_3 must be S_2S_3=10. Therefore the second SCCM also exists when $S_1S_2S_3S_4$ are X10X, where X means either 0 or 1, corresponding to the Mode 1, 2, 9, 10 in Fig. 6. At this time, the switches of chopper controllers are off and the short circuits are thus avoided.



(a) (b)

Fig. 7. Simplified power unit and Fig. 5



(a) The first SCCM (b) The second SCCM

Fig. 8. Simplified short circuit circulation paths

Both the first and second SCCM cannot exist between any two different power units when the SCCM of the two adjacent capacitors is avoided, which can be demonstrated as follows. In the CMI, composed by *N* power units, it is supposed that *T* (*1*<*T*< *N*) power units are chosen randomly and continuously, as shown simply in Fig. 9.

Case 1: the first SCCM.

Assuming P_1 and N_T are short-circuited at a certain time, which is determined by the operation state of the CMI, we can demonstrate that there is no equivalent path $\overrightarrow{P_1N_1}$ through which the capacitor C_1 can be shorted. Otherwise, the following equation should be true.

$$\begin{aligned}\overrightarrow{P_1N_1}&=\overrightarrow{P_1N_T}+\overrightarrow{N_TN_{T-1}}\cdots+\overrightarrow{N_{t+1}N_t}\cdots+\overrightarrow{N_2N_1}\\&=\overrightarrow{P_1N_T}+\sum_{i=2}^{T}\overrightarrow{N_iN_{i-1}}\end{aligned}\tag{2}$$

Firstly, $\overrightarrow{N_iN_{i-1}}$ means the path from point N_i to N_{i-1}. The existence of this path depends on the state of the chopper controller between points N_i to N_{i-1}. Based on the fourth principle as stated above, the state of the chopper controllers can be obtained.

Secondly, $\overrightarrow{P_1N_T}$ means the path from P_1 to N_T. Obviously, there are multiple routes $\overrightarrow{P_1N_T}$ changed by the switches of these *T* power units. But as points P_1 and N_T have the equal potential (they are shorted as mentioned previously and this short circuit case may appear at a certain time for the CMI), so there are only two choices for the CMI to form Path $\overrightarrow{P_1N_T}$.

1. One is the route that will not pass the capacitors C_i ($1 \le i \le T$).
2. The other one is the route which will go through the capacitors and its positive passing (from *P* to *N*) times equal to the negative passing (from *N* to *P*) times. If not, points P_1 and N_T cannot have the same potential.

Therefore, there must be *k* paths working in the first SCCM and *k-1* paths working in the second SCCM to build the route from the positive pole P_1 to the negative pole N_T. In all, at least *2k-1* chopper controllers work in the SCCM isolated condition. Thus, no equivalent path $\overrightarrow{P_1N_1}$ works in the first SCCM and can short capacitor C_1. *k* is subject to the range as follows:

$$1 \le k \le T/2 \quad k \in Z \tag{3}$$

As Fig. 9 shows, a specific example is given. In this

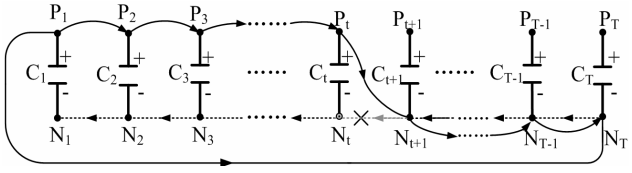


Fig. 9. The simplified first SCCM among power units

example, the path $\overrightarrow{P_1N_T}$ forms by the route as follows.

$$\overrightarrow{P_1N_T}=\overrightarrow{P_1P_2}+\overrightarrow{P_2P_3}+\cdots+\overrightarrow{P_tN_{t+1}}+\cdots+\overrightarrow{N_{T-1}N_T} \tag{4}$$

There is 1 path $\overrightarrow{P_1N_{t+1}}$ working in the first SCCM and 0 paths working in the second SCCM. As a result, the path $\overrightarrow{N_{t+1}N_t}$ is blocked to avoid this SCCM, which is determined by the fourth principle afore-mentioned. So the path $\overrightarrow{P_1N_1}$ working in the first SCCM cannot be formed between any two power units.

Case 2: the second SCCM.

For the same reason, if it is assumed that points P_T and N_1 are short-circuited at a certain time, there must be *k-1* paths in the first SCCM and *k* paths in the second SCCM within the route $\overrightarrow{P_TN_1}$, which means at least *2k-1* chopper controllers work in the SCCM isolated condition. In this case, the path $\overrightarrow{P_1N_1}$ working in the second SCCM is determined by the following expression.

$$\begin{aligned}\overrightarrow{P_1N_1}&=\overrightarrow{P_1P_2}\cdots+\overrightarrow{P_tP_{t+1}}\cdots+\overrightarrow{P_{T-1}P_T}+\overrightarrow{P_TN_1}\\&=\sum_{i=1}^{T-1}\overrightarrow{P_iP_{i+1}}+\overrightarrow{P_TN_1}\end{aligned} \tag{5}$$

Also a specific example is given to explain, as Fig. 10 shown. In this example, the path $\overrightarrow{P_TN_1}$ forms by the route as follows.

$$\begin{aligned}\overrightarrow{P_TN_1}=&\overrightarrow{P_TN_T}+\overrightarrow{N_TN_{T-1}}+\overrightarrow{N_{T-1}P_{T-1}}\\&+\cdots\overrightarrow{P_{t+1}N_t}+\cdots\overrightarrow{N_3P_2}+\overrightarrow{P_2N_1}\end{aligned} \tag{6}$$

There are 2 paths $\overrightarrow{P_2N_1}$ and $\overrightarrow{P_{t+1}N_t}$ working in the second SCCM and 1 path $\overrightarrow{N_3P_2}$ working in the first SCCM. The path $\overrightarrow{P_TN_1}$ goes through the capacitors twice and its positive passing (from P_T to N_T) times equals to the negative passing (from N_{T-1} to P_{T-1}) times. As a result, these paths $\overrightarrow{P_1P_2}$, $\overrightarrow{P_2P_3}$ and $\overrightarrow{P_tP_{t+1}}$ are blocked to avoid the SCCM, which is determined by the fourth principle afore-mentioned. So, the path $\overrightarrow{P_1N_1}$ working in the second SCCM cannot be formed between any two power units.

Consequently, there is also no path working in the second SCCM. In other words, there is no equivalent path $\overrightarrow{P_1N_1}$ which works in the first or second SCCM and can short C_1. Obviously, C_1 can be any one of the N power units.

According to the analysis above, the conclusion can be safely drawn as follows: If a pair of neighboring power units does not have a short circuit path, there will be no such path in any pair of power units or among random power units. Therefore, the algorithm proposed by this paper could be extended to any amount of power units even if it is derived by two power units. This algorithm is demonstrated to avoid coupling and allow for easy expansion.

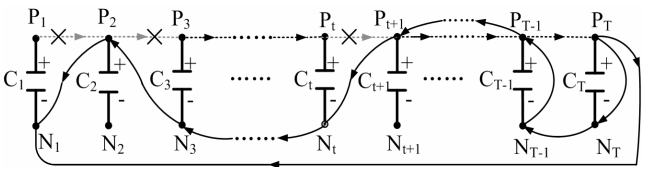


Fig. 10. The simplified second SCCM among power units

3.4 Implementation

Based on the analysis above, a conclusion can be drawn that the logic variables $T_1T_2T_3T_4$ are determined by the logic states $S_1S_2S_3S_4$. Truth table in Table 1 expresses their relationship.

According to the truth table, Eq. (7) can be derived,

$$Q_1=T_1=T_2=T_3=T_4=S_2\odot S_3 \tag{7}$$

Similarly, based on the operational rules, the general

Table 1. Switch logic of units and chopper controllers

S_1	S_2	S_3	S_4	T_1	T_2	T_3	T_4
0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	1
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	0	1	1	1	1
0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	1
1	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	0	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1

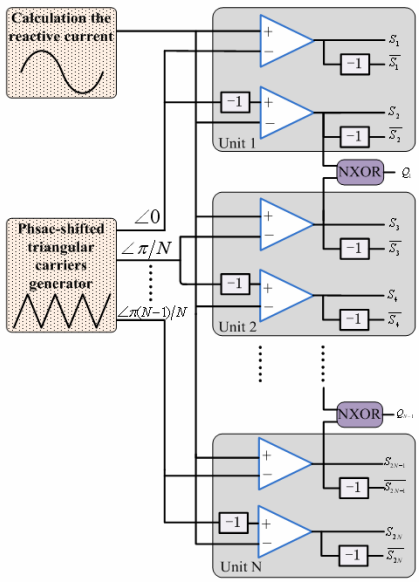


Fig. 11. Generation method of driving signals

switch logic of the chopper controllers can be deduced,

$$Q_{N-1} = S_{2N-2} \odot S_{2N-1} \tag{8}$$

Based on this equation and the CPS-SPWM rule [21], it is easy to get the generation method of the driving signals of the power units and its shunting chopper controllers, as illustrated in Fig. 11.

4. Performance Analysis

It's very important to evaluate the hardware investment and research on the chopper controller circuit's performance, which will affect the performance of the new strategy proposed by this paper.

The equivalent circuit of the voltage balancing loop between the two capacitors is illustrated in Fig. 12. R_{esr} and C_e are the equivalent series resistance and the equivalent capacitance of the voltage balancing loop, respectively. ΔU is the initial voltage difference. $u_e(t)$ and $i_b(t)$ are the voltage difference and the balancing current, respectively.

$$R_e = R_{esr} + R_{extra} \tag{9}$$

$$C_e = \frac{C_1 C_2}{C_1 + C_2} = \frac{C}{2} \tag{10}$$

$$u_e(t) = \Delta U e^{-\frac{1}{R_e C_e} t} \tag{11}$$

$$i_b(t) = \frac{u_e(t)}{R_e} = \frac{\Delta U}{R_e} e^{-\frac{1}{R_e C_e} t} \tag{12}$$

It is clear that the small steady error means small voltage difference, small balancing current and low hardware cost.

From (12), the energy loss $\Delta E_{1\leftrightarrow 2}$ caused by the voltage balancing between the capacitors C_1 and C_2 is given by

$$\Delta E_{1\leftrightarrow 2} = \lim_{t\to\infty} \int_0^t R_e \cdot i_b^2(t) dt = \frac{1}{4} C \left(\Delta U\right)^2 \tag{13}$$

Based on (13), the total energy loss ΔE can be calculated as

$$\Delta E = \sum_{i=1}^{N-1} \Delta E_{i\leftrightarrow i+1} = \frac{1}{4} C \sum_{i=1}^{N-1} \left(\Delta U_{i\leftrightarrow i+1}\right)^2 \tag{14}$$

Obviously, the energy loss is independent of the impedance R_e in the balancing circuit. In other words, the additional hardware for the voltage balancing control will not affect the system efficiency, only increasing the hardware cost slightly. Therefore, the value of the additional resistor R_{extra} is determined by the expected steady error and the affordable voltage/current rate of the chopper controllers. Ref. [7] gives a concrete design method which has comprehensively considered the hardware cost, the affordable voltage/current rate and the balancing control performance.

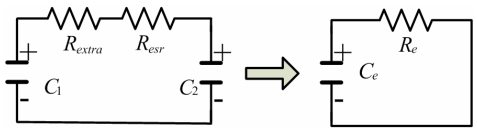


Fig. 12. Equivalent circuit of the voltage balancing loop

From (14), we know that all the DC voltage control methods will cause energy loss invariably, which is determined by the essential characteristics of DC capacitor voltages' disequilibrium. Nevertheless, Expression (14) is not convenient to predict and evaluate the total energy loss. Hence, this paper analyzes this issue from another perspective.

Assuming that the DC capacitor voltage offset of power unit *i* is ε_i, and its voltage u_i can be described by

$$u_i = u_r + \varepsilon_i \tag{15}$$

Therefore, the DC CMI voltage u_d is deduced.

$$u_d = \sum_{i=1}^{N} u_i = \sum_{i=1}^{N} \left(u_r + \varepsilon_i\right) = N u_r + \sum_{i=1}^{N} \varepsilon_i \tag{16}$$

From (1) and (10), the fact that the sum of the individual voltage offset is zero can be found easily.

$$\sum_{i=1}^{N} \varepsilon_i = 0 \tag{17}$$

Based on the Capacitor-Energy Formula and from (17), the energy loss ΔE can be deduced by

$$\begin{aligned} \Delta E &= \sum_{i=1}^{N} \frac{1}{2} C u_i^2 - \sum_{i=1}^{N} \frac{1}{2} C u_r^2 \\ &= \sum_{i=1}^{N} \frac{1}{2} C (u_r + \varepsilon_i)^2 - \sum_{i=1}^{N} \frac{1}{2} C u_r^2 \\ &= \frac{1}{2} C \sum_{i=1}^{N} \varepsilon_i^2 + C u_r \sum_{i=1}^{N} \varepsilon_i = \frac{1}{2} N C \sigma^2 \end{aligned} \tag{18}$$

Where

$$\sigma^2 = \frac{1}{N} \sum_{i=1}^{N} \varepsilon_i^2$$

σ^2 represents the voltage variance, which reflects the degree of the DC capacitor voltage unbalance.

When the system is in the steady state, every power unit can keep its voltage stable and balanced with the chopper controller based DC voltage control strategy. Therefore, ε_i can be approximated as zero, as well as the energy loss ΔE. Based on the previous discussion, we know that the

energy loss can be designed to be arbitrarily small on condition that the system parameters are reasonable and the DC voltage control strategy can ensure good performance.

Moreover, almost all the software-based methods must use the information of every DC capacitor voltage's changing trend. Thus, all the DC voltages of the power units must be detected simultaneously. But the new control strategy needs only one physical quantity that is the DC CMI voltage used by the upper layer control. Considering that the new strategy can ensure that the individual DC voltage is stable and balanced, we can deduce that the DC CMI voltage can be calculated based on (1) and only one DC capacitor voltage should be detected. Consequently, the hardware cost and microprocessor resource, which are spent by the high DC voltage sensors and signals processing (e.g. signals' acquisition, analysis and calculating), can be cut down significantly. Based on the previous discussion, that the new strategy provides a cost advantage compared to the existing technologies is gotten.

It's necessary to explain that this new scheme has two defects. One is that the added chopper controllers will reduce the system reliability. But with the development of design capability and manufacturing engineering, the reliability of the semiconductor switching device is high enough. So the effect caused by the first defect is negligible. Another defect is that the SCCM may cause the CMI fail to operate properly and efficiently. When the chopper controller operates from the voltage balancing state to the SCCM isolating state and if the chopper controller is not turned off in time, the afore-mentioned issue will occur. This problem can be solved by setting dead time which is chosen to be just a few microseconds for the fast switching devices, as is often the case with avoiding the cross-conduction current through a half-bridge inverter leg.

5. Simulation Verification

In this section, a cascaded STATCOM comprised in each phase by a 5-unit-series-connected CMI has been built by using Matlab/Simulink to verify the effectiveness of the proposed scheme. Wiring between chopper controllers and its adjacent power units is shown in Fig. 5. In order to simulate the active power loss absorbed by the operating power units, a resistor is shunted to the DC capacitor. Obviously, the resistances of these resistors are different to each other for the different parameters and distinct operation modes of the power units. A list of the system parameters considered in this simulation is included in Table 2.

Table 2. Parameters of the simulation model

Parameters	Value	Parameters	Value
Power Source	6kV/50Hz	Rdc_1	550Ω
Switch Frequence	1kHz	Rdc_2	500Ω
Load Resistance	100Ω	Rdc_3	510Ω
Load Inductance	160mH	Rdc_4	540Ω
DC capacitors	5000uF	Rdc_5	530Ω
DC Voltage	2500V	Rextra	1Ω

Obviously, cascaded STATCOMs without the DC voltage control cannot work normally and the capacitor voltages of each power unit will fall quickly. At this time, the cascaded STATCOM acts as a harmonic generator for the system.

5.1 Operation with the total active power control

Fig. 13 shows the simulation results when only the total active power control is implemented. In Fig. 13(a), the DC CMI output voltage keeps stable and maintains at 12.5kV with small steady-state error, about 0.23V. Fig. 13(b) shows that the DC capacitor voltages' imbalance aggravates with time elapsing, though the total voltage of DC side is maintained. The maximum voltage difference reaches 250V within 3 minutes. This difference attributed to the variation of active energy loss results in a lot of serious influence. First, the DC voltage imbalance leads CMI output voltage/current waveforms to distort, and the levels of the AC CMI voltage have aggravating ripples. Second, the distorting CMI output waveforms make source current distorted and the distortion is positively correlated with the voltage imbalance. Third, the CMI operates as a harmonic generator at this moment. The fact that some capacitors are overcharging and others are undercharging reveals that the active power isn't allocated reasonably and the active power allocating strategy should be employed.

5.2 Operation with the proposed control strategy

Fig. 14 displays the simulation results when the new

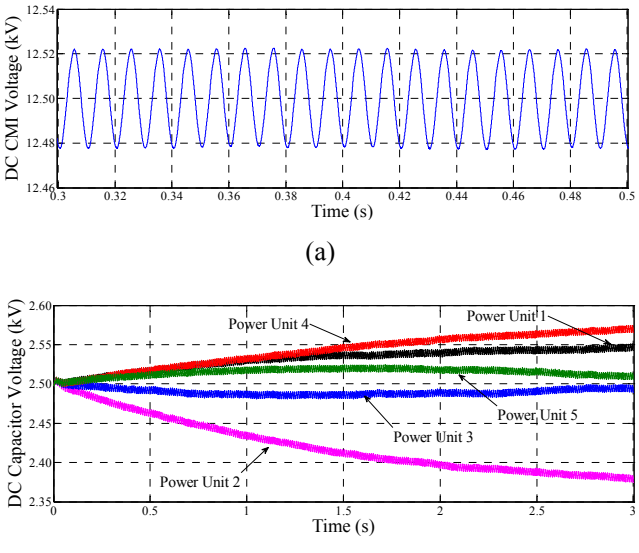
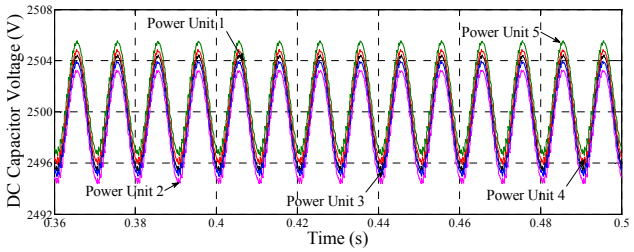
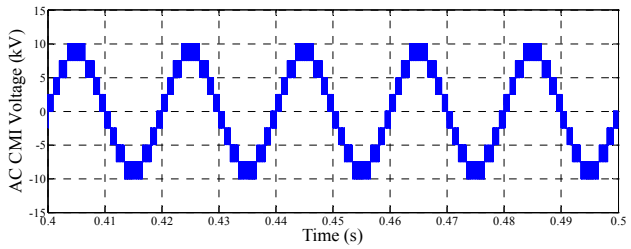


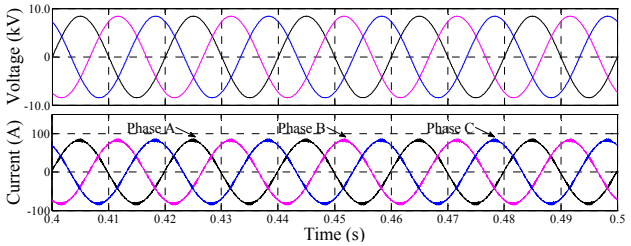
Fig. 13. Operation with the total active power control



(a)



(b)

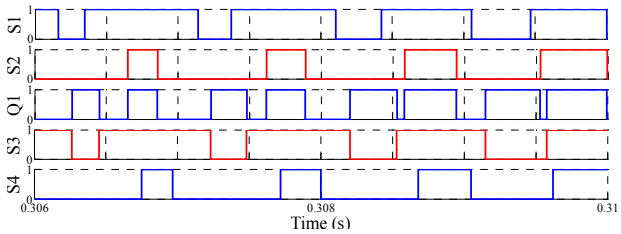


(c)

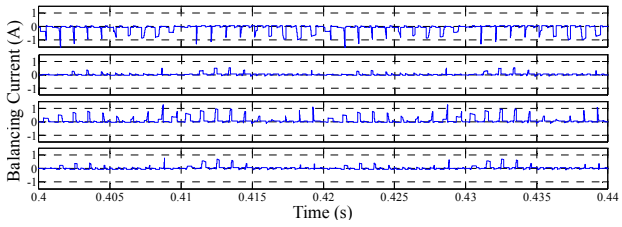
Fig. 14. Operation with the chopper controller based DC voltage control strategy

control strategy is employed. The DC CMI output voltage remains stable and maintains at 12.5kV, which is the same with the Fig. 13(a). Fig. 14(a) reveals that the system is able to hold the voltage of the five capacitors within a tiny range across 2.5kV which is the designated voltage, costing only little time for dynamic adjustment. The largest voltage deviation is about 0.8V out of 2.5kV and that of the cascaded STATCOM with the software-based methods may be several tens of volts, indicating that this strategy accomplishes the targets of stability and balance of the DC voltages. Therefore, the CMI output voltage/current waveforms and the modulation waveform are regular and smooth, and the THD of the AC CMI voltage is only 17.21%, as shown in Fig. 14(b). Best stabilization and balance of the DC voltage ensure that the STATCOM operates in the stable and high-efficiency state. Fig. 14(c) shows the compensated source voltage and current whose waveforms without any distortion and phase difference, indicating the STATCOM has a good performance with the new control strategy.

Fig. 15(a) reveals the fact that the chopper controllers' switch frequency is twice that of the power units also agrees with the theoretical result. Fig. 15(b) indicates that the chopper controller currents are satisfactorily low,

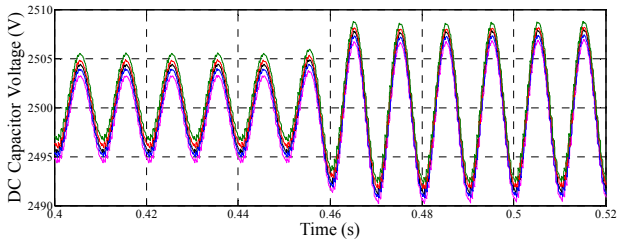


(a)

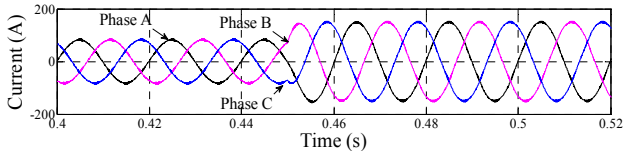


(b)

Fig. 15. Balancing currents and driving signals waveforms



(a)



(b)

Fig. 16. Operation with load transient

because the largest peak value is below 1A and the mean values are of approximately 0A in this model. Tiny currents and voltages mean little dissipation, high efficiency and low hardware cost.

5.3 Operation with load transient

Fig. 16 displays the simulation results when the load has been changed to 50Ω and 80mH suddenly. The load current value increases from 75A to 150A suddenly at 0.45s. The steady-state value of DC CMI voltage still holds at 12.5kV and the fluctuation range increases from 42V to 81V within 0.01s. In Fig. 16(a), individual capacitor voltage keeps 2.5kV with tiny steady error and the fluctuation range increases from 9.8V to 16.3V within 0.01s. The CMI output current and the source current have the same changing trend as well as the physical quantities described

above, increasing from 40A to 75A and from 82A to 150A without any oscillation, also within 0.01s, showing in Fig. 16(b). Fig. 16 indicates that the cascaded STATCOM with the new control strategy has good dynamic performance and steady-state performance.

6. Conclusion

Keeping the DC voltages of cascaded STATCOM stable and balanced is significant for its reliability and safety. Due to the different parameters and working modes of power units, DC capacitor voltages cannot maintain the reference value and are different from each other. The existing strategies can be categorized as hardware-based and software-based methods. The former can reach good performance but cost too much. The latter does not need so many facilities but it is impractical in high-power devices. Neither of them can achieve the best performance with the lowest cost simultaneously. This paper proposes a new control method with a combination of the chopper controllers and the hierarchical control to fulfill the control targets. Both theoretical analysis and simulation results verify that the strategy can be extended for STATCOM composed by N-unit-series-connected CMI. The major advantages of the proposed control strategy are that the number of PI regulators can be reduced remarkably and accordingly the blindness of system design and debugging also decreases obviously. For its excellent performance, good robustness, easy expansion, few control parameters and low hardware cost, it is practical in high power and high voltage equipment. The simulation results reveal that the proposed control scheme could achieve the desired control goals.

Acknowledgements

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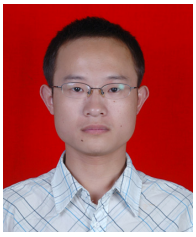

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