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Performance Analysis of a Novel Reduced Switch Cascaded Multilevel Inverter

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Abstract

Multilevel inverters have been widely used for high-voltage and high-power applications. Their performance is greatly superior to that of conventional two-level inverters due to their reduced total harmonic distortion (THD), lower switch ratings, lower electromagnetic interference, and higher dc link voltages. However, they have some disadvantages such as an increased number of components, a complex pulse width modulation control method, and a voltage-balancing problem. In this paper, a novel nine-level reduced switch cascaded multilevel inverter based on a multilevel DC link (MLDCL) inverter topology with reduced switching components is proposed to improve the multilevel inverter performance by compensating the above mentioned disadvantages. This topology requires fewer components when compared to diode clamped, flying capacitor and cascaded inverters and it requires fewer carrier signals and gate drives. Therefore, the overall cost and circuit complexity are greatly reduced. This paper presents modulation methods by a novel reference and multicarrier based PWM schemes for reduced switch cascaded multilevel inverters (RSCMLI). It also compares the performance of the proposed scheme with that of conventional cascaded multilevel inverters (CCMLI). Simulation results from MATLAB/SIMULINK are presented to verify the performance of the nine-level RSCMLI. Finally, a prototype of the nine-level RSCMLI topology is built and tested to show the performance of the inverter through experimental results.

Key words: Modulation Index (MI), Unipolar Sinusoidal Pulse Width Modulation (USPWM), Saw Tooth Multicarrier USPWM (STMC USPWM), Total Harmonic Distortion (THD), Triangular Multicarrier USPWM (TMC USPWM), Unipolar Sine Multicarrier USPWM (USMC USPWM)

I. INTRODUCTION

Multilevel power conversion was first introduced more than two decades ago. The general concept involves utilizing a higher number of active semiconductor switches to perform power conversion in small voltage steps. There are several advantages to this approach when compared with the conventional power conversion approach. The smaller voltage steps lead to the production of higher power quality waveforms, and they reduce both the voltage (*dv/dt*) stress on the load and the electromagnetic compatibility concerns [1]. Another important feature of multilevel inverters is that their semiconductors are wired in a series-type connection, which allows operation at higher voltages. However, this series connection is typically made with clamping diodes, which eliminates overvoltage concerns. Furthermore, since the switches are not truly series connected, their switching can be staggered. This reduces the switching frequency which reduces the switching losses.

One clear disadvantage of multilevel power conversion is the higher number of semiconductor switches required. It should be pointed out that lower voltage rated switches can be used in the multilevel inverter. Therefore, the active semiconductor cost is not appreciably increased when compared with two level cases. However, each active semiconductor added requires associated gate drive circuits and adds further complexity to the converter mechanical layout. Another disadvantage of multilevel power converters is the fact that the small voltage steps are typically produced by isolated voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readily available, and series capacitors require voltage balancing [2]. To some extent, the voltage balancing can be addressed by using redundant switching states, which exist due to the high number of semiconductor devices. However, for a complete

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solution to the voltage-balancing problem, another multilevel inverter may be required [3].

In recent years, there has been a substantial increase in interest in multilevel power conversion. Recent research has involved the introduction of novel inverter topologies and unique modulation strategies. However, the most recently used inverter topologies, which are mainly addressed as applicable multilevel inverters, are the neutral-point clamped (NPC) inverter, the flying capacitor inverter, and the cascade inverter. Among these, the cascade inverter topology is the most attractive, since it requires the least number of components and increases the number of levels in the inverter without requiring high ratings on individual devices while increasing the power rating of the inverter [4].

Some applications for these new converters include industrial drives [5], flexible ac transmission systems (FACTS) [6]–[8], and vehicle propulsions [9], [10]. One area where multilevel inverters are particularly suitable is that of renewable photovoltaic energy where efficiency and power quality are of great concern to researchers [11].

Some new approaches have been recently suggested such as a topology utilizing low-switching-frequency high power devices [12]. Although this topology has some modification to reduce output voltage distortions, the general disadvantage of this method is that it has significant low-order current harmonics. It is also unable to exactly manipulate the magnitude of the output voltage due to an adopted pulse width modulation (PWM) method [13].

Another approach is selection based on a set target which can be either the minimum switches used or the minimum dc voltage used. It also requires different voltage source values which are defined according to the target selection [14]. However, this approach requires basic units which are connected in series, and the basic units require more switches than the proposed topology. Another disadvantage of this topology is that the power switches and diodes need to have a different rating which is a major drawback of the topology.

The proposed topology is a symmetrical topology since all the values of all the voltage sources are equal. However, there are asymmetrical topologies [15] which require different voltage sources. This criterion makes it necessary to arrange the dc power supplies according to a specific relation between the supplies. Differences in the ratings of the switches in this topology are also a major drawback. This problem also occurs in similar topologies [16]–[18]. Some of the high frequency switches in this topology should approximately withstand the maximum overall voltage which makes its application limited to high-voltage products. In [19], a new approach has been proposed that decreases the number of required dc supplies by inserting a transformer instead. The main disadvantage of this approach is the need to add so many transformer windings which will increase the overall volume and cost of the inverter.

This paper presents an overview of a new multilevel inverter topology referred to as a RSCML inverter. It is based on a multilevel DC link (MLDCL) topology. This topology requires a smaller number of components when compared to conventional topologies. It is also more efficient since the inverter has a component which operates the switching power devices at line frequency. Therefore, there is no need for all the switches to work in high frequency which leads to simpler and more reliable control of the inverter. Different multicarrier PWM techniques which use triangular carrier waveforms, saw tooth carrier waveforms and unipolar sine carrier waveforms are simulated for a 1KW, 3φ, nine-level RSCMLI using MATLAB/SIMULINK. The fundamental output voltage and the percentage of THD are observed and compared for different switching frequencies and modulation indexes. These results are verified by building an experimental prototype of a single phase nine level RSCML inverter and implementing the different multicarrier PWM techniques on it.

II. Conventional Cascaded Multilevel Inverter

The single-phase structure of a three-phase nine-level conventional cascaded inverter is illustrated in Fig 1. Each separate dc source is connected to a single-phase full-bridge or H-bridge inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0 and $-V_{dc}$, by connecting the dc source to the ac output with different switching combinations of the four semiconductor switches T_1,T_2,T_3 and T_4. To obtain $+V_{dc}$, switches T_1 and T_2 are tuned on, while $-V_{dc}$ can be obtained by tuning on switches T_3 and T_4. By turning on T_1 and T_3 or T_2 and T_4, the output voltage is 0. The ac outputs of each of the full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs [20], [21].

$$m = 2n + 1 \tag{1}$$

$$N = 2(m - 1) \tag{2}$$

Where m is the number of levels, n is the number of DC sources, and N is the number of switching devices in each phase. The most well known SPWM which can be applied to a conventional cascaded multilevel inverter (CCMLI) is the Phase-Shifted SPWM. This modulation technique is almost the same as the conventional SPWM technique which is applied to a conventional single phase full-bridge inverter. The only difference between them is that the Phase-Shifted SPWM utilizes more than one carrier. The number of carriers used per phase is equal to twice the number of dc voltage sources per phase (2n) [20].

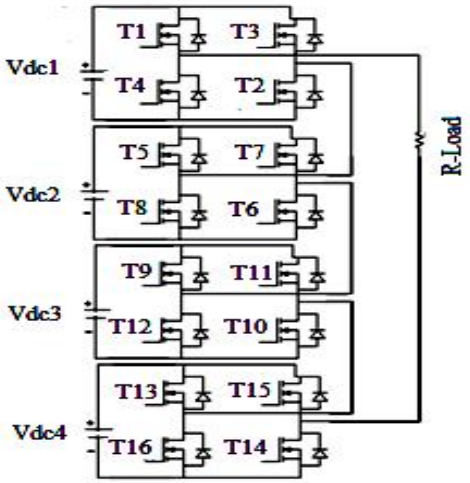


Fig. 1. Single phase structure of the conventional cascaded multilevel inverter.

III. Proposed Reduced Switch Cascaded Multilevel Inverter Topology

In conventional multilevel inverters, the power semiconductor switches are combined to produce a high-frequency waveform in positive and negative polarities. However, there is no need to utilize all of the switches for generating bipolar levels. This idea has been put into practice by the novel topology.

This topology is a hybrid multilevel inverter topology which uses two parts to generate the output voltage. One part is named the level generation part and it is responsible for the generation of different voltage levels. This part requires high-frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability. The other part is called the polarity generation part and it is responsible for generating the polarity of the output voltage. The polarity generation part operates at a low-frequency (line frequency). The proposed topology combines the two parts (high frequency and low frequency parts) to generate the multilevel voltage output. In order to generate a complete multilevel output, the positive levels are generated by the high-frequency part (level generation). Then, this part's output voltage is fed to a full-bridge cascaded inverter (polarity generation), which will generate the required polarity for the output. This eliminates many of the semiconductor switches which were responsible for generating the output voltage levels in positive and negative polarities in conventional cascaded multilevel inverters.

The proposed RSCMLI topology in the single phase structure of nine-levels is shown in Fig. 2. As can be seen, it requires eleven switches and four isolated sources. The principal idea of this topology is that the left circuit in Fig. 2 generates the required output levels (without polarity) and the right circuit cascaded inverter (full-bridge inverter) determines the polarity of the output voltage. This part, which

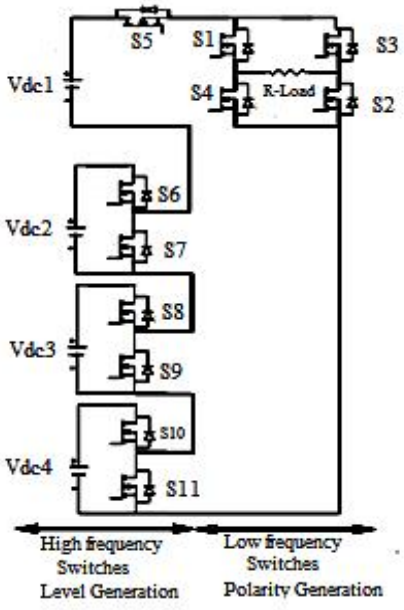


Fig. 2. Single phase structure of the proposed multilevel inverter.

is named the polarity generation part, transfers the required output level to the output with the same direction or the opposite direction according to the required output polarity.

This topology easily extends to higher voltage levels by including an additional end stage in the level generation part in Fig. 2. Therefore, this topology is modular and can be easily increased to higher voltage levels. This topology is also suitable for applications where separate dc voltage sources are available, such as photovoltaic (PV) generators, fuel cells and batteries. The phase output voltage is generated by the sum of the output voltages of each stage, which results in an output phase voltage with nine-levels. In general, if m is the number of levels and N is the number of switching devices in each phase, then the following relation applies:

$$N = m + 2 \tag{3}$$

It can also be applied to three-phase applications with the same principle. This topology uses isolated dc supplies. Therefore, it does not face voltage-balancing problems due to fixed dc voltage values. When compared with a conventional cascaded inverter topology, it requires fewer switching components. Another advantage of the proposed topology is that it requires half the carriers when compared to a conventional SPWM controller. The SPWM for a nine-level CCML inverter consists of eight carriers. However, in this topology, four carriers are sufficient. This is because, according to Fig. 2, the level generation part generates only positive polarity voltage levels and does not generate negative voltage levels. Therefore, it implements the multilevel inverter with a reduced number of carriers, which is a great achievement for inverter control. In the CCMLI topology all of the switches should be selected from fast

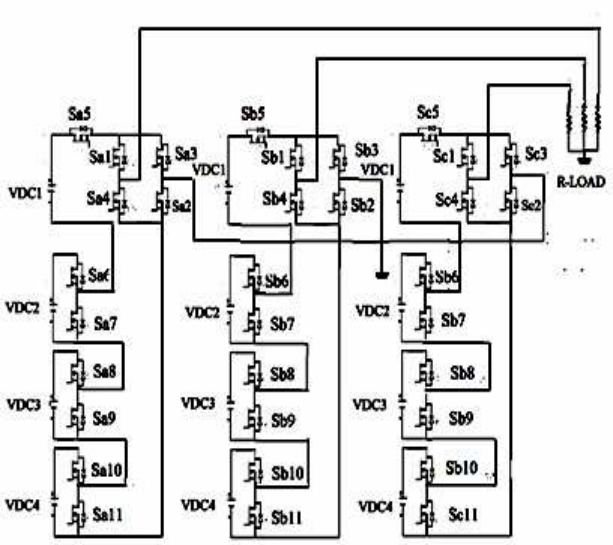


Fig. 3. Three-phase power circuit of the nine-level RSCMLI.

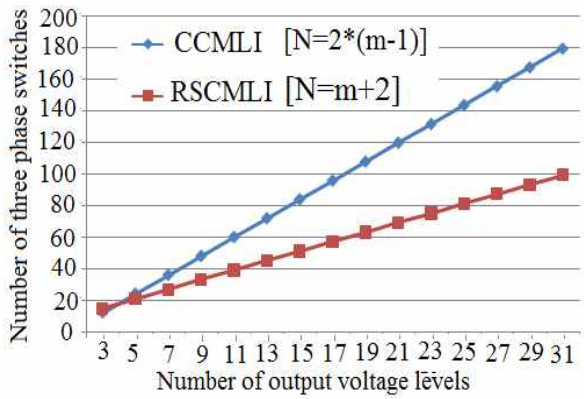


Fig. 4. Comparison of RSCML inverter and CCML inverter.

switches. However, the proposed topology does not require fast switches for the polarity generation part. Fig.3 presents the three-phase power circuit of the nine-level RSCML inverter. MATLAB/SIMULINK simulation results are obtained for the output phase and line voltages of the three phase nine level RSCMLI with 1KW, 3φ, resistive loads for the various PWM techniques.

The Fig. 4 shows a comparison of the proposed RSCML inverter and a CCML inverter based on the required number of switches and the number of levels. From this comparison, it is clear that as the number of voltage levels, m, grows, the number of active switches increases according to m+2 for the RSCML inverter and 2(m-1) for the CCML inverter. The switching sequence in the nine-level RSCMLI is given in Table I to produce the output voltage of the different levels. In general, n-number of isolated dc supply sources are required to produce m-output voltage levels with the cascaded inverter. Based on the various switching sequences given in Table I, switching signals are generated for the switches in the RSCML inverter.

IV. MODULATION TECHNIQUES

Pulse Width Modulation (PWM) control strategy development tries to reduce the total harmonic distortion (THD) of the output voltage. Increasing the switching frequency of the PWM pattern reduces the lower frequency harmonics by moving the switching frequency carrier harmonic and the associated sideband harmonics away from the fundamental frequency component [21]. This increased switching frequency reduces harmonics. This results in a lower THD with high quality output voltage waveforms of the desired fundamental RMS value and frequency, which are as close as possible to the sinusoidal wave shape.

Any deviation from the sinusoidal wave shape will result in harmonic currents in the load and this harmonic current produces electromagnetic interference (EMI), harmonic losses and torque pulsation in the case of motor drives. A higher switching frequency can be employed for low and medium power inverters. Meanwhile, for high power and medium voltage applications the switching frequency should be low. Harmonic reduction can then be strictly related to the performance of an inverter with any switching strategy.

Three phase multilevel inverters require three modulating signals or reference signals which are three-unipolar sine waves with a 120 degree phase shift. In this paper, three new carrier based PWM techniques are developed as follows:

1. Triangular Multicarrier Unipolar Sine PWM (TMC USPWM)
2. Saw Tooth Multicarrier Unipolar Sine PWM (STMC USPWM)
3. Unipolar Sine Multicarrier Unipolar Sine PWM (USMC USPWM)

Each carrier is compared with a corresponding modulating unipolar sine wave. The reference or modulation waveform has peak amplitude A_m and a frequency f_m, and it is centered in the middle of the carrier set. The general principle of the carrier based PWM technique is a comparison of a reference waveform with a carrier waveform, this typically being a triangular carrier waveform. The reference is continuously compared with the carrier signal. If the reference is greater than the carrier signal, then the active device corresponding to that carrier is switched on, and if the reference is less than the carrier signal, then the active device corresponding to that carrier is switched off. The carrier frequency defines the switching frequency of the converter and the high order harmonic components of the output voltage spectrum. and the sidebands occur around the carrier frequency and its multiples. In multilevel inverters, the amplitude modulation index, M_a, and the frequency ratio, M_f, are defined as:

$$M_a = \frac{A_r}{((m-1)/2)A_c} \quad (4)$$

$$M_f = \frac{f_c}{f_r} \quad (5)$$

TABLE I
SWITCHING SEQUENCES FOR SINGLE PHASE NINE-LEVEL RSCML INVERTER

Output voltage level	Switching Sequence										
	Polarity Generation Switches				Level Generation Switches						
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11
4Vdc	1	1	0	0	1	1	0	1	0	1	0
3Vdc	1	1	0	0	1	1	0	1	0	0	1
2Vdc	1	1	0	0	1	1	0	0	1	0	1
Vdc	1	1	0	0	1	0	1	0	1	0	1
0	1	0	1	0	0	0	0	0	0	0	0
-Vdc	0	0	1	1	1	0	1	0	1	0	1
-2Vdc	0	0	1	1	1	1	0	0	1	0	1
-3Vdc	0	0	1	1	1	1	0	1	0	0	1
-4Vdc	0	0	1	1	1	1	0	1	0	1	0

Where A_r and A_c are the amplitude of the reference and the carrier signal, respectively. f_r and f_c are the frequency of the reference and the carrier signal respectively[22].

In this paper, the modulation indexes used are 0.8, 0.9 and 1 for a nine-level RSCML inverter. For multilevel applications, carrier based PWM techniques with multiple carriers are used. Multicarrier Modulation (MCM) techniques, can be divided in to the following categories [23]:

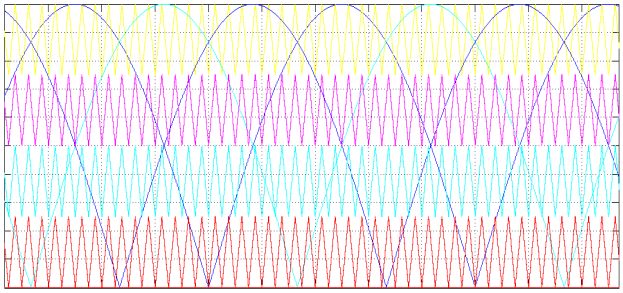
1. Phase Disposition (PD) where all of the carriers are in phase.
2. Inverted Phase Disposition (IPD) where all of the carriers are in phase and inverted.
3. Phase Opposition Disposition (POD) where the carriers above half of the reference are in phase but shifted by 180 degrees from those carriers below half of the reference.
4 Alternative Phase Opposition Disposition (APOD) where each carrier band is shifted by 180 degrees from the adjacent carrier band [24].

The above modulation strategies are implemented for different carriers such as the triangular multicarrier wave, saw tooth multicarrier wave and unipolar sine multicarrier wave. The phase voltage waveform, line voltage waveform and harmonic spectrum of the phase and line voltages are shown for different modulation techniques by doing simulations using MATLAB-SIMULINK for a nine-level RSCMLI and CCMLI. A comparison is done on the obtained results.

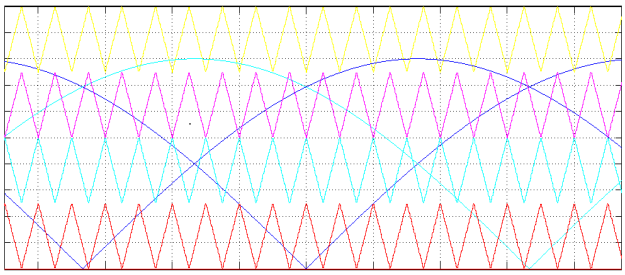
A. Triangular Multicarrier Unipolar Sinusoidal PWM (TMC USPWM)

The performance of a multilevel inverter is based on the multi carrier modulation technique used. Two-level to multilevel inverters are made using several triangular carrier signals and one reference signal per phase. Carrara [25] developed multilevel sub harmonic PWM (SH-PWM), which is as follows:

For m-level inverters, (m-1)/2 carriers with the same frequency f_c and the same amplitude A_c are disposed such that the bands they occupy are contiguous. They are defined as:



(a)



(b)

Fig. 5. (a) PD TMC USPWM with $M_a = 1$ for nine-level RSCMLI. (b) POD TMC USPWM with $M_a = 0.8$ for nine-level RSCMLI.

$$C_i = A_c\left((-1)^{f(i)} y_c(\omega_c, \varphi) + t - \frac{m}{2}\right), \quad i = 1, \ldots\ldots (m-1) \tag{6}$$

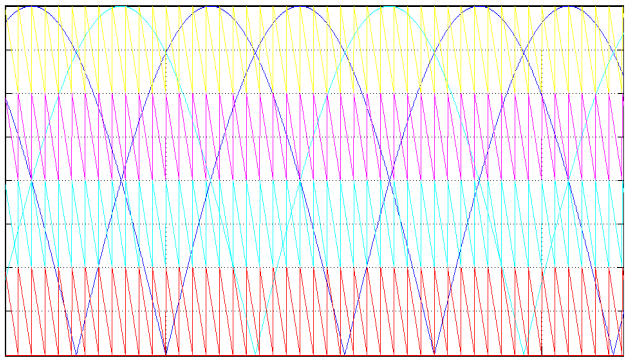
Where y_c is a normalized symmetrical triangular carrier defined as:

$$y_c(\omega_c, \varphi) = (-1)^{\lfloor \alpha \rfloor}((\alpha \bmod 2) - 1) + \frac{1}{2} \tag{7}$$

$$\alpha = \frac{\omega_c t + \varphi}{\pi}, \omega_c = 2\pi f_c \tag{8}$$

where φ represents the phase angle of y_c. y_c is a periodic function with the period $T_c = \frac{2\pi}{\omega_c}$. It is shown that using a symmetrical triangular carrier generates less harmonic distortion at the inverter's output [26], [27].

The multicarrier modulation techniques (PD, IPD, POD, and APOD) are implemented using triangular multicarrier signals for a nine-level RSCMLI with different modulation



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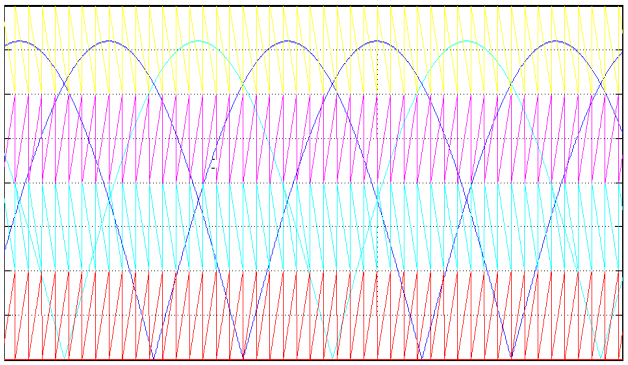


(b)

Fig. 6. (a) IPD STMC USPWM with $M_a = 1$ for nine-level RSCMLI. (b) APOD STMC USPWM with $M_a = 0.9$ for nine-level RSCMLI.

indexes. They are shown in Fig. 5(a) and 5(b), respectively.

B. Saw Tooth Multicarrier Unipolar Sinusoidal PWM (STMC USPWM)

The saw tooth wave is a periodic signal which is generated arbitrarily and can be obtained from the repeated sequence carrier wave by limiting its magnitude to A_c. The simulink block sets the input period as the difference between the first and last value of the time values parameter. The output at any time t is the output at time:

$$t = t - n \times \text{period} \tag{9}$$

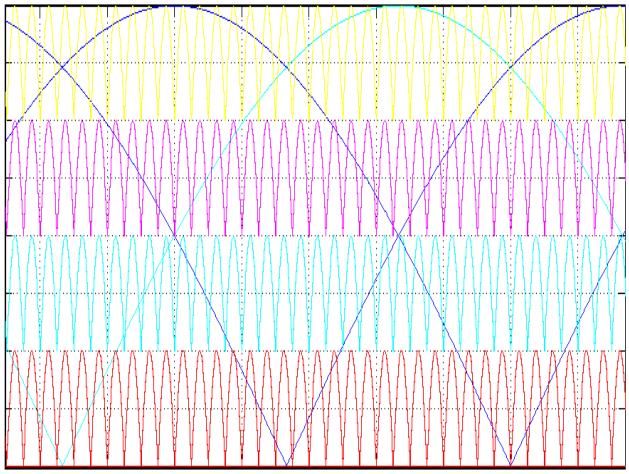
Where n is an integer. The sequence repeats at:

$$t = n \times \text{period} \tag{10}$$

The simulink block uses linear interpolation to compute the value of the waveform between the specified output times. In this technique, the gate signals are generated by comparing the saw tooth multicarrier wave with a unipolar sinusoidal modulating signal.

The multicarrier modulation techniques (PD, IPD, POD, and APOD) are implemented using saw tooth multicarrier signals for a nine level RSCMLI with different modulation indexes. They are shown in Fig. 6(a) and 6(b), respectively.

C. Unipolar Sine Multicarrier Unipolar Sinusoidal PWM (USMC USPWM)



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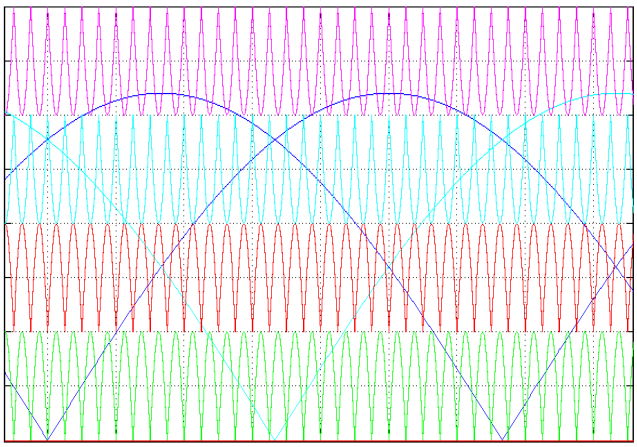


(b)

Fig. 7. (a) PD USMC USPWM with $M_a = 1$ for nine-level RSCMLI. (b) POD USMC USPWM with $M_a = 0.8$ for nine-level RSCMLI.

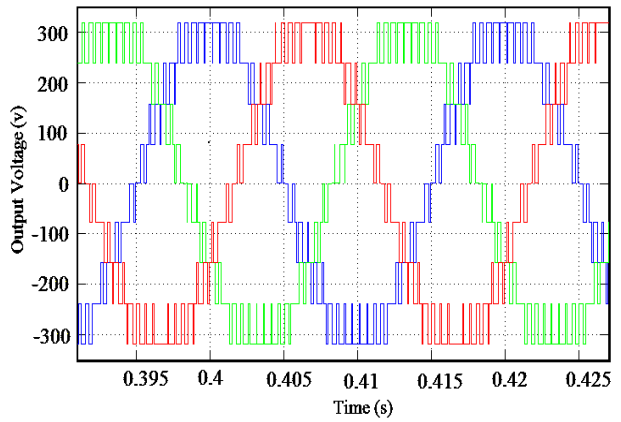
In this PWM technique, the sinusoidal signal is converted into a unipolar sinusoidal signal. The entire negative half cycles in the waveform are converted into positive half cycles with the same amplitude and frequency. This signal is the same as that of the full wave rectifier output. That is the signal has only continuous positive half cycles. This is called the unipolar sine wave.

The control strategy uses the same signal for the reference (synchronized unipolar sinusoidal signal) and carrier signals. The control scheme uses a high frequency unipolar sine carrier that helps maximize the output voltage for a given modulation index.

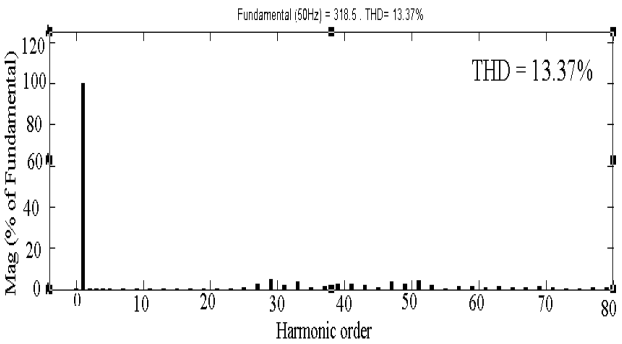
The multicarrier modulation techniques (PD, IPD, POD, and APOD) are implemented using unipolar sine multicarrier signals for a nine level RSCMLI with different modulation indexes. They are shown in Fig 7(a) and 7(b), respectively.

V. SIMULATION RESULTS

The nine level RSCML inverter model with different



(a)



(b)

Fig. 8. (a) Phase Voltage for nine-level APOD USPWM with $M_a = 1$. (b) Percentage phase Voltage THD for nine-level APOD USPWM with $M_a = 1$.

modulation indexes was implemented in MATLAB/SIMULINK software to demonstrate the feasibility of the PWM techniques. The phase disposition, inverted phase disposition, phase opposition disposition and alternative phase opposition disposition techniques are used for the various multicarrier USPWM techniques such as:

1. Triangular Multicarrier Unipolar Sine PWM (TMC USPWM)
2. Saw Tooth Multicarrier Unipolar Sine PWM (STMC USPWM)
3. Unipolar Sine Multicarrier Unipolar Sine PWM (USMC USPWM)

The phase and line voltage waveform with its harmonic spectrum at a fundamental frequency of 50Hz and switching frequencies (SF) of 2 KHz and 10 KHz are obtained for the proposed RSCML inverter. For comparison, the total harmonic distortion (THD) was evaluated for all of the modulation techniques. In order to get the THD level of the waveform, a Fast Fourier Transform (FFT) was applied to obtain the spectrum of the output voltage [28]. The THD was calculated using the following equation:

$$THD = \frac{\sqrt{\sum_{n=2}^{80} v_n^2}}{v_1} \quad (11)$$

Where n is the harmonic order, v_n is the RMS value of the n^{th} harmonic component and v_1 is the RMS value of the fundamental component. Here, the %THD is calculated up to a harmonic order which is twice the switching frequency. For a 2 KHz switching frequency, up to the 80^{th} order harmonics are taken in to account for calculating the THD. For a 10 KHz switching frequency, up to the 400^{th} order harmonics are taken in to account for calculating the THD.

A. Triangular Multicarrier USPWM (TMC USPWM)

Fig 8(a) and 8(b) show the phase voltage waveforms and the percentage THD of the phase voltage for the nine-level APOD USPWM using the alternative phase opposition disposition technique for triangular multicarrier unipolar sinusoidal PWM with $M_a = 1$.

Table II shows the percentage phase voltage THD for a nine-level RSCMLI and CCMLI with triangular multicarrier signals with different multicarrier PWM techniques with switching frequencies of 2 KHz and 10 KHz for different modulation indexes.

From Table II, it can be observed that when the switching frequency of the RSCMLI is increased, the percentage phase voltage THD increases for the PD scheme with all of the modulation indexes. In the IPD scheme, if the switching frequency is increased, the percentage phase voltage THD decreases with modulation indexes of 1 and 0.8. In the POD scheme, when the switching frequency is increased, the percentage phase voltage THD increases with a modulation index of 1. In the APOD scheme, if the switching frequency is increased, the percentage phase voltage THD decreases with a modulation index of 0.8.

The results obtained from the nine-level RSCMLI are also compared with those of the CCMLI when the switching frequencies are 2 KHz and 10 KHz (To limit the number of pages, the comparison is done for only for the switching frequency). It is found that in some of the modulation techniques the percentage phase voltage THD slightly increases in the CCMLI. However, the proposed RSCMLI has a reduced number of switches and increases in the fundamental phase and line voltages.

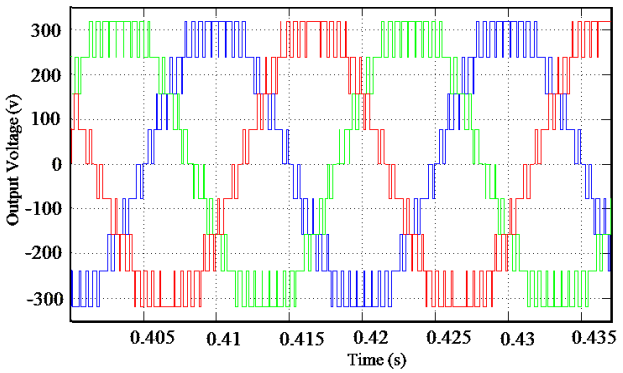
From the simulation results of the triangular multicarrier USPWM technique with the PD and IPD PWM schemes, from the 3^{rd} order harmonics to the 21^{st} order harmonics are less than 1% and all of the even order harmonics are zero. A few of the odd order harmonics from the 23^{rd} harmonics to the 79^{th} harmonics are 1% to 2%. The dominant 39^{th} and 41^{st} harmonic factors are about 5% for the PD and IPD schemes.

In the POD scheme, from the 3^{rd} order harmonics to the 21^{st} order harmonics are less than 1% and all of the even order harmonics are zero. A few of the odd order harmonics from the 23^{rd} harmonics to the 55^{th} harmonics are 1% to 3%. The dominant 35^{th} and 45^{th} harmonic factors are 4.77% and

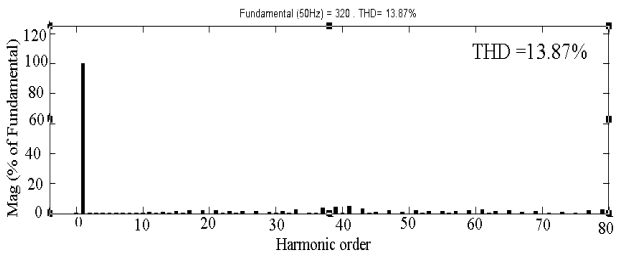
TABLE II

PHASE VOLTAGE % THD FOR NINE-LEVEL RSCMLI AND CCMLI WITH TRIANGULAR MULTI CARRIER USPWM

Modulation Technique	Phase voltage % THD											
	Reduced Switch Cascaded Multilevel Inverter						Conventional Cascaded Multilevel Inverter					
	SF = 2KHz			SF = 10KHz			SF= 2KHz			SF = 10KHz		
	M_a=1	M_a=0.9	M_a=0.8	M_a=1	M_a=0.9	M_a=0.8	M_a=1	M_a=0.9	M_a=0.8	M_a=1	M_a=0.9	M_a=0.8
PD	13.43	16.74	16.95	14.40	17.08	17.11	**13.75**	16.60	17.25	14.32	17.02	17.39
IPD	14.07	16.80	17.43	14.05	16.87	17.31	13.80	16.67	17.28	14.32	17.02	17.39
POD	13.83	16.83	17.49	14.30	16.79	17.31	13.92	16.65	17.37	14.28	17.01	17.35
APOD	**13.37**	16.74	17.26	14.19	16.86	17.24	14.04	16.67	17.21	14.39	17.14	17.39



(a)



(b)

Fig. 9. (a) Phase Voltage for nine-level PD USPWM with $M_a = 1$. (b) Percentage Phase Voltage THD for nine-level PD USPWM with $M_a = 1$.

4.88%, respectively, for the POD scheme.

In the APOD scheme, from the 3rd order harmonics to the 25th order harmonics are less than 1% and all of the even order harmonics are zero. A few of the odd order harmonics from the 27th harmonics to the 69th harmonics are 1% to 3%. The dominant 29th and 51st harmonic factors are 4.67% and 4.61%, respectively, for the APOD scheme.

It is observed that when the switching frequency of the RSCMLI is increased, the percentage line voltage THD increases very slightly and the fundamental phase and line voltage decrease for the all of the PWM schemes.

B. Saw Tooth Multicarrier USPWM (STMC USPWM)

Fig 9(a) and 9(b) show the phase voltage waveforms and the percentage THD of the phase voltage for the nine level PD USPWM using the phase disposition technique for the saw tooth multicarrier unipolar sinusoidal PWM with $M_a = 1$.

Table III shows the percentage of phase voltage THD for the nine-level RSCML inverter and the CCML inverter with the saw tooth multicarrier signal with different multicarrier PWM techniques with a switching frequency of 2 KHz and 10 KHz, respectively, for different modulation indexes.

From Table III, it is observed that when the switching frequency of the RSCMLI is increased, the percentage phase voltage THD decreases for the PD and POD schemes with a modulation index of 1. In the IPD and APOD schemes, if the switching frequency is increased, the percentage phase voltage THD increases for all of the modulation indexes.

From the simulation result in the saw tooth multicarrier USPWM technique with the PD and IPD PWM schemes, from the 3rd order harmonics to the 13th order harmonics are less than 1% and all of the even order harmonics are zero. A few of the odd order harmonics from the 15th harmonics to the 79th harmonics are 1% to 2%. The dominant 39th and 41st harmonic factors are about 4% for the PD and IPD schemes.

In the POD scheme, from the 3rd order harmonics to the 13th order harmonics are less than 1% and all of the even order harmonics are zero. A few of the odd order harmonics from the 15th harmonics to the 79th harmonics are 1% to 3%. The dominant 35th and 45th harmonic factors are 4.10% and 4.75%, respectively, for the POD scheme.

In the APOD scheme, from the 3rd order harmonics to the 13th order harmonics are less than 1% and all of the even order harmonics are zero. A few of the odd order harmonics from the 15th harmonics to the 79th harmonics are 1% to 3%. The dominant 29th and 51st harmonic factors are 4.26% and 4.55%, respectively, for the APOD scheme.

It is observed that when the switching frequency of the RSCML inverter is increased, the percentage line voltage THD decreases and the fundamental phase and line voltage increase for the PD scheme. In the IPD and APOD schemes, if the switching frequency is increased, the percentage line voltage THD increases and the fundamental phase and line voltage decrease. In the POD scheme, when the switching frequency is increased, the percentage line voltage THD and the fundamental phase and line voltage increase. The

TABLE III
PHASE VOLTAGE % THD FOR NINE-LEVEL RSCMLI AND CCMLI WITH SAW TOOTH MULTI CARRIER USPWM

Modulation Technique	Phase voltage % THD											
	Reduced Switch Cascaded Multilevel Inverter						Conventional Cascaded Multilevel Inverter					
	SF = 2KHz			SF = 10KHz			SF= 2KHz			SF = 10KHz		
	M_a=1	M_a=0.9	M_a=0.8	M_a=1	M_a=0.9	M_a=0.8	M_a=1	M_a=0.9	M_a=0.8	M_a=1	M_a=0.9	M_a=0.8
PD	13.87	16.48	16.45	**13.26**	16.57	17.15	13.45	16.80	17.46	13.84	16.77	17.11
IPD	14.16	16.52	16.59	14.43	16.85	17.20	13.45	16.80	17.46	13.79	16.70	17.08
POD	13.91	16.46	16.67	13.48	16.68	17.54	13.37	16.48	17.46	**13.18**	16.46	17.12
APOD	14.09	16.46	16.38	14.32	16.66	16.69	13.22	16.79	17.36	14.31	16.79	16.60

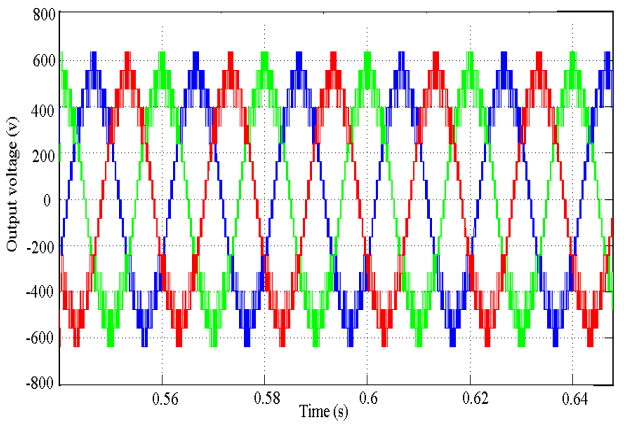


Fig. 10. (a) Line Voltage for nine-level IPD USPWM with $M_a = 1$. (b). Percentage Line Voltage THD for nine-level IPD USPWM with $M_a = 1$.

fundamental line voltage is maximum for the PD and POD schemes and minimum for the IPD and APOD schemes.

C. Unipolar Sine Multicarrier USPWM (USMC USPWM)

Fig 10(a) and 10(b) show the line voltage waveforms and the percentage THD of the line voltage for the nine level IPD USPWM using the inverted phase disposition technique for the unipolar sine multicarrier unipolar sinusoidal PWM with $M_a = 1$.

Table IV shows the percentage phase voltage THD for the nine-level RSCML inverter and the CCML inverter with a unipolar sine multicarrier signal with different multicarrier PWM techniques with switching frequencies of 2 KHz and 10 KHz, respectively, for different modulation indexes.

From Table IV, it is observed that when the switching frequency of the RSCMLI is increased, the percentage line voltage THD increases for the PD, IPD, POD and APOD schemes with all of the modulation indexes.

From the simulation results of the unipolar sine multicarrier USPWM technique PD PWM scheme, from the 3rd order harmonics to the 17th order harmonics are less than 1% and all of the even order harmonics are zero. A few of the odd order harmonics from the 19th harmonics to the 77th harmonics are 1% to 2%. The dominant 79th harmonic factor is 7.03% for the PD scheme.

In the IPD scheme, from the 3rd order harmonics to the 21st order harmonics and from the 25th order harmonics to the 55th order harmonics are less than 1% and all of the even order harmonics are zero. A few of the odd order harmonics from the 57th harmonics to the 77th harmonics are 1% to 2%. The dominant 79th harmonic factor is 5.13% for the IPD scheme.

In the POD scheme, from the 3rd order harmonics to the 15th order harmonics and from the 21st order harmonics to the 55th order harmonics are less than 1% and all of the even order harmonics are zero. A few of the odd order harmonics from the 57th harmonics to the 77th harmonics are 1% to 2%. The dominant 75th and 79th harmonic factors are 5.17% and 3.49%, respectively, for the POD scheme.

In the APOD scheme, from the 3rd order harmonics to the 7th order harmonics and from the 25th order harmonics to the 55th order harmonics are less than 1% and all of the even order harmonics are zero. A few of the odd order harmonics from the 57th harmonics to the 77th harmonics are 1% to 2%. The dominant 69th and 73rd harmonic factors are 5.15% and 3.23%, respectively, for the APOD scheme.

It is observed that, when the switching frequency of the RSCML inverter is increased, the percentage line voltage THD increases and the fundamental phase and line voltage increase for the PD scheme. In the IPD scheme, if the switching frequency is increased, the percentage line voltage THD increases and the fundamental phase and line voltage decrease. In the POD and APOD schemes, when the switching frequency is increased, the percentage line voltage THD increases and the fundamental phase and line voltage

TABLE IV

PHASE VOLTAGE % THD FOR NINE-LEVEL RSCMLI AND CCMLI WITH UNIPOLAR SINE MULTI CARRIER USPWM

Modulation Technique	Phase voltage % THD											
	Reduced Switch Cascaded Multilevel Inverter						Conventional Cascaded Multilevel Inverter					
	SF = 2KHz			SF = 10KHz			SF= 2KHz			SF = 10KHz		
	M_a=1	M_a=0.9	M_a=0.8	M_a=1	M_a=0.9	M_a=0.8	M_a=1	M_a=0.9	M_a=0.8	M_a=1	M_a=0.9	M_a=0.8
PD	15.79	17.46	18.51	16.11	18.53	20.43	14.56	16.99	18.22	15.92	17.66	19.75
IPD	**13.88**	16.34	18.12	15.83	16.69	19.36	14.56	16.99	18.22	10.57	**10.22**	13.24
POD	14.14	16.92	18.99	15.95	17.36	20.09	15.59	17.79	18.95	16.24	18.59	20.51
APOD	14.55	17.52	19.95	16.13	17.75	20.87	14.55	17.83	20.19	16.27	17.87	20.88

TABLE V

PERFORMANCE ANALYSIS OF NINE-LEVEL RSCMLI WITH M_a=1

Modulation Technique		Switching Frequency = 2KHz			
		Line voltage % THD	Voltage per phase (volts)	Line voltage (volts)	Dominant harmonic factor (%)
Triangular Multi carrier	**PD**	**11.36**	228.2	393.5	H_{39}=5.32 H_{41}=5.57
	IPD	11.92	227.1	393.8	H_{39}=5.55 H_{41}=5.66
	POD	12.28	228.0	393.7	H_{35}=4.77 H_{45}=4.88
	APOD	12.20	227.2	393.1	H_{29}=4.67 H_{51}=4.61
Saw Tooth Multi carrier	**PD**	11.66	228.4	395.1	H_{39}=3.89 H_{41}=4.38
	IPD	11.89	227.1	392.7	H_{39}=4.90 H_{41}=4.50
	POD	12.39	228.2	395.4	H_{35}=4.10 H_{45}=4.75
	APOD	12.16	227.4	393.5	H_{29}=4.26 H_{51}=4.55
Unipolar Sine Multi carrier	**PD**	13.89	217.9	376.2	H_{79}=7.03
	IPD	11.40	**235.0**	**405.4**	H_{79}=5.13
	POD	13.37	232.4	402.1	H_{75}=5.17 H_{79}=3.49
	APOD	13.17	230.7	398.3	H_{69}=5.15 H_{73}=3.23
Switching Frequency = 10KHz					
Triangular Multi carrier	**PD**	12.44	226.9	392.4	H_{199}=6.03 H_{201}=6.02
	IPD	12.32	227.3	392.2	H_{199}=5.80 H_{201}=5.93
	POD	12.95	227.0	392.5	H_{195}=4.58 H_{205}=4.58
	APOD	12.60	227.1	392.5	H_{189}=4.80 H_{211}=4.80
Saw Tooth Multi carrier	**PD**	**11.03**	231.2	399.2	H_{199}=4.03 H_{201}=4.05
	IPD	12.60	224.3	387.4	H_{199}=4.61 H_{201}=4.75
	POD	12.44	230.3	397.9	H_{195}=4.20 H_{205}=4.07
	APOD	12.61	226.0	390.2	H_{189}=4.08 H_{211}=4.14
Unipolar Sine Multi carrier	**PD**	14.08	219.3	378.7	H_{19}=2.40
	IPD	13.92	**232.0**	**400.6**	H_{399}=6.54
	POD	14.61	229.8	397.1	H_{395}=4.13 H_{399}=4.74
	APOD	14.31	228.2	393.9	H_{389}=4.79 H_{399}=3.37

decrease. In addition, the fundamental line voltage is maximum for the IPD and POD schemes and is minimum for the PD and APOD schemes. M_a=1

Table V shows the percentage line voltage THD, fundamental phase and line voltage and dominant harmonic factors obtained for the nine-level RSCMLI with different multicarrier PWM techniques with switching frequencies of 2 KHz and 10 KHz with modulation index of unity.

From Table V, it is observed that when the switching frequency is 2 KHz, the unipolar sine (IPD) scheme gives maximum phase and line voltage and the triangular (PD) scheme gives minimum % THD for the line voltage. If the switching frequency is 10 KHz, the unipolar sine (IPD) scheme gives maximum phase and line voltage and the saw tooth (PD) scheme gives minimum % THD for the line voltage.

VI. EXPERIMENTAL RESULTS

In order to experimentally validate the proposed multicarrier PWM techniques, a prototype 100W, 96V, single phase nine-level RSCMLI was constructed using MOSFETs as the switching devices. The MOSFETs, ramp generator, comparator and diodes used are IRF840, UA741, LM324 and IN5408, respectively. The source voltage is 24V for each of the DCMLIs. In total 96V DC is applied across the input side of the nine-level RSCMLI. The RSCMLI output provides power to a 100W resistive load. A picture of the laboratory experimental prototype, built to verify the operation and to obtain the phase voltage of the different multicarrier phase disposition USPWM techniques is shown in Fig.11. The prototype includes a nine-level RSCMLI circuit and measurement equipment. Fig. 12(a) and 12(b) show the phase voltage waveform and the harmonics spectrum of the phase voltage for a nine-level RSCMLI using the phase disposition technique for the triangular multi carrier unipolar sinusoidal

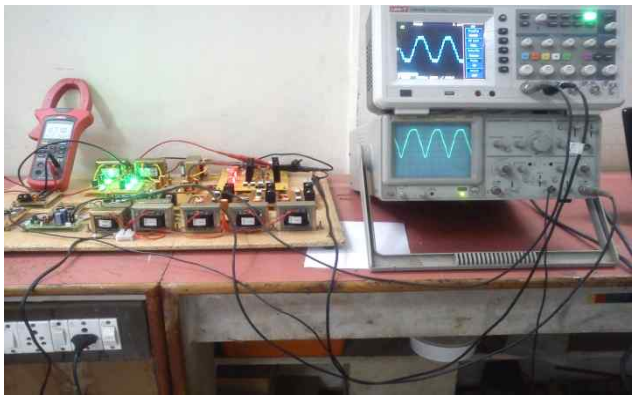
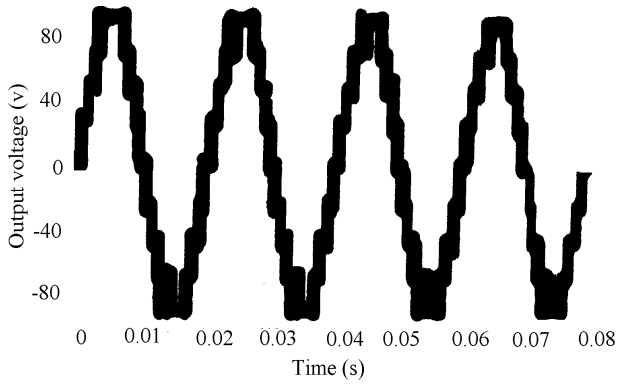
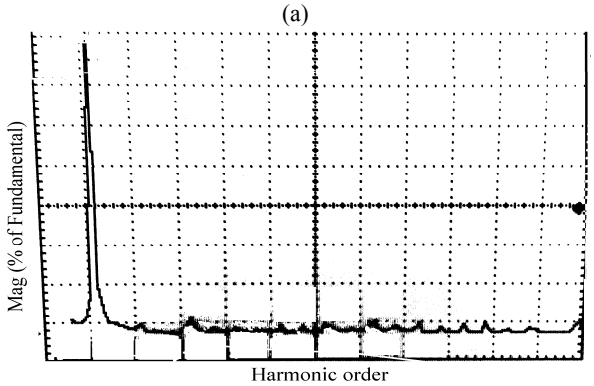


Fig. 11.Nine-level RSCMLI Experimental setup.



(a)



(b)

Fig. 12. (a) Phase Voltage for nine-level TMC PD USPWM with $M_a = 1$. (b) Harmonics spectrum for nine-level TMC PD USPWM with $M_a = 1$.

Fig. 13 shows the phase voltage waveform for a nine-level RSCMLI using the phase disposition technique for the saw tooth multi carrier unipolar sinusoidal PWM with $M_a = 0.9$.

Fig. 14 shows the phase voltage waveform for a nine-level RSCMLI using the phase disposition technique for the unipolar sine multi carrier unipolar sinusoidal PWM with $M_a = 0.8$. Due to the switching and ohmic losses of the converter switches, the peak value of the ac output voltage is found to be 96V. By varying the amplitude of the modulating signal, the RMS output phase voltage can be varied from 0V to 76V.

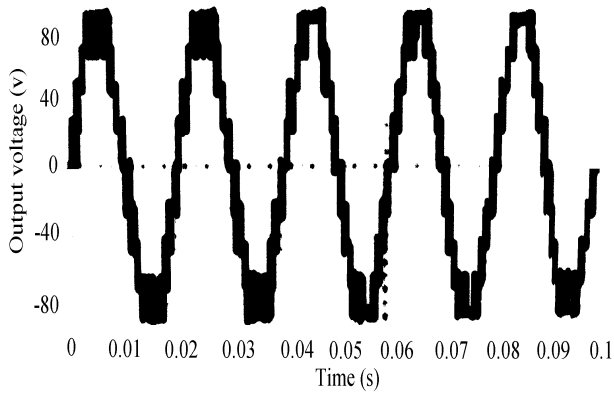


Fig. 13. Phase Voltage for nine-level STMC PD USPWM with $M_a = 0.9$.

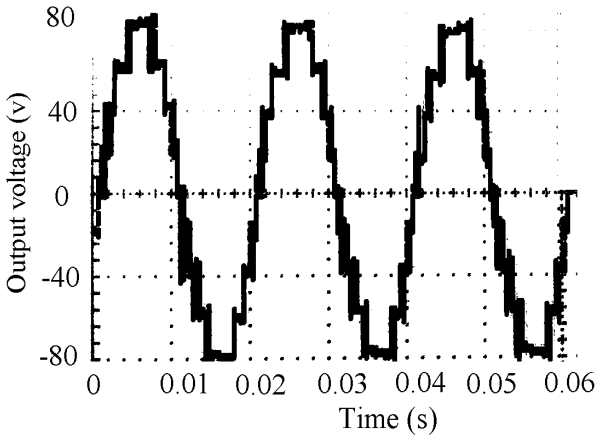


Fig. 14. Phase Voltage for nine-level USMC PD USPWM with $M_a = 0.8$.

TABLE VI

EXPERIMENTAL ANALYSIS OF NINE-LEVEL RSCMLI

Modulation Technique	Phase voltage (volts)		
	M_a=1	M_a=0.9	M_a=0.8
Triangular Multi carrier	72.4	68.6	62.6
Saw Tooth Multi carrier	**75.3**	68.8	62.7
Unipolar Sine Multi carrier	72.6	69.2	65.1
Phase voltage % THD			
Triangular Multi carrier	**5.8**	6.0	6.4
Saw Tooth Multi carrier	6.0	6.3	6.7
Unipolar Sine Multi carrier	8.4	9.5	10.2

Table VI shows the fundamental phase voltage and percentage THD of the phase voltage obtained experimentally for a nine-level RSCMLI with the different multicarrier PWM techniques with a switching frequency of 2

KHz with different modulation indexes. From the above table, it is observed that in all of the multicarrier PWM schemes, if the modulation index is decreased, the phase voltage decreases and the percentage phase voltage THD increases. From the experimental results the saw tooth multicarrier scheme gives the maximum output phase voltage and the triangular multicarrier gives minimum % THD for the phase voltage.

VII. CONCLUSION

In this paper, a novel reduced switch cascaded multilevel inverter (RSCMLI) topology has been proposed which has superior features when compared with the conventional cascaded multilevel inverter (CCMLI) topology in terms of the minimum number of required power switches, control requirements, cost, and reliability. This topology can be a good candidate for the inverters used in power applications such as FACTS, HVDC, PV systems, UPS, etc. In the proposed topology, the switching operation is separated into high-frequency and low-frequency parts. This increases the efficiency of the inverter and reduces the size and cost of the final prototype.

In this paper, the performance of different multicarrier PWM techniques which use the triangular multicarrier waveform, saw tooth multicarrier waveform and unipolar sine multicarrier waveform are determined. In all of the above PWM techniques, different modulation strategies such as the phase disposition (PD), inverted phase disposition (IPD), phase opposition disposition (POD) and alternative phase opposition disposition (APOD) are implemented. The results are verified through simulations for a 1KW, 3φ nine-level RSCMLI in MATLAB/SIMULINK. The output quantities such as the fundamental phase and line voltage, percentage THD of the phase voltage, line voltage and percentage dominant harmonic factor are measured in the all of the above PWM schemes and the results are compared. Experimental results of the developed prototype for a single phase nine-level RSCMLI of the proposed topology are obtained for the different multicarrier PWM techniques. The USPWM control method is used to drive the inverter. The PWM for this topology has fewer complexities since it generates only the positive carriers for PWM control. The results clearly show that the proposed topology can effectively work as a multilevel inverter with a reduced number of switches and carriers for PWM.

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