JPE 14-1-2

http://dx.doi.org/10.6113/JPE.2014.14.1.11
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Novel Switched-Inductor Quasi-Z-source Inverter

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Abstract

A novel switched-inductor quasi-Z-source inverter is proposed in this study. Compared with classic topologies, the boost ability of the proposed topology is strengthened. The voltage stress of the capacitors, diodes, and power devices are reduced, and the current ripple of the DC voltage source is suppressed. Conversion efficiency is also improved. The operation principle of the proposed topology is analyzed in detail and compared with that of similar topologies. The feasibility of the proposed topology is verified by simulations and experiments on a laboratory prototype.

Keywords: Boost ability, Comparison, Switched inductor

I. INTRODUCTION

The Z-source inverter (ZSI) has elicited much interest recently because of its obvious advantages compared with the classic voltage source inverter. First, ZSIs utilize the shoot-through of the inverter bridge to boost voltage and are thus more suitable for applications with low input voltages, such as photovoltaic and fuel cells. Second, no dead time exists between the conduction of the upper switch and that of the lower switch; thus, the distortion of the output waveform is reduced. Third, boost and inversion of the voltage are realized with single-stage power conversion; efficiency is thus increased. Lastly, ZSIs exhibit better immunity against EMI noise [1–5]. However, classic ZSI have obvious disadvantages, such as high voltage stress in the switches and capacitors, huge inrush current, and weak boost ability. The most significant drawback is the discontinuous input current, which limits the use of ZSIs and causes lifetime damage to the DC source. Several pulse width modulation (PWM) methods, such as the maximum boost control method [6] and the constant boost control method [7], have been developed to overcome these drawbacks and obtain reduced voltage stress and increased boost ability. However, these PWM methods have yet to extend the voltage gain without sacrificing the device cost as well as avoid the discontinuous input current. Fortunately, the improvement of circuit topology appears to be an opportunity for ZSIs [8]-[19].

Manuscript received Jul. 6, 2013; revised Oct. 9, 2013
Recommended for publication by Associate Editor Honnyong Cha.
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In [8] and [9], an improved ZSI was proposed to reduce the capacitor voltage stress and startup inrush current; however, boost ability remained unchanged and the input current was still discontinuous. In [10], a novel family of extended-boost ZSIs was developed. Diode or capacitor assistance was applied to increase the boost ability and make the input current continuous. However, these extended-boost ZSIs have obvious shortcomings, such as small boost effect, complicated structure, and large size. In [11] and [12], a class of quasi-Z-source inverters (qZSI) was proposed by Peng et al. Compared with the classic ZSI, qZSI has a lower rating and fewer power devices, continuous input current, and lower current stress for the DC source. A common ground point also exists in qZSI for the DC source and the inverter. Nevertheless, the boost ability of qZSIs remains limited. In [13], a class of trans-Z-source inverters was presented; these inverters employed two coupled magnetic inductors instead of separate ones, and the DC link voltage was boosted according to the changes in turn and shoot-through duty ratios. However, the effect of leak inductance remains inevitable.

Switched capacitor (SC), switched inductor (SL), and hybrid SC/SL techniques are commonly used in DC–DC converters to achieve high boost capability with transformerless cascade structures; thus, size is reduced and power density is increased [14]-[16]. ZSI and SL techniques were successfully combined in [17] to overcome the boost limitation of the classic ZSI; a switched-inductor Z-source inverter (SL-ZSI) was presented. Compared with [17], two isolated DC sources were embedded into the SL-ZSI topology in [18] to make the input current continuous, suppress the voltage stress, and improve reliability. Nevertheless, the circuits in [17] and [18] still entail increased cost, loss, and size because of the large number of components.

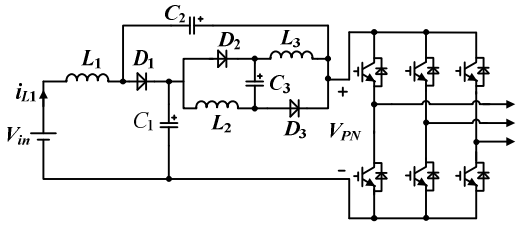


Fig. 1. Proposed SL-qZSI.

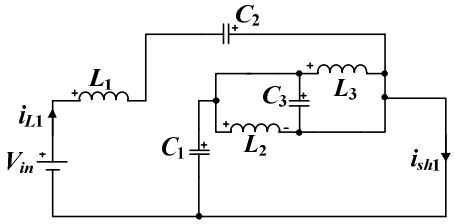


Fig. 2. Equivalent circuit of the proposed SL-qZSI in the shoot-through state.

Compared with the SL-ZSIs mentioned above, the switched-inductor quasi-Z-source inverter (SL-qZSI) in [19] not only has fewer passive components but also produces lower stress on the capacitors, inductors, and diodes. Continuous input current is likewise generated. At startup, SL-qZSIs can avoid inrush current, which could destroy the switching devices. A novel SL-qZSI is proposed in this study to further enhance the performance of SL-qZSIs. The typical switched inductors are replaced by a bootstrap capacitor and boost inductors derived from [20] without increasing the complexity of the circuit. Compared with the classic qZSI and SL-qZSI in [11] and [19], the proposed topology possesses much greater boost ability with the same shoot-through duty ratio. The proposed SL-qZSI achieves low voltage stress for capacitors, diodes, and power devices as well as low current ripple for the input inductor. Furthermore, the conversion efficiency of the proposed topology is improved. The operation principle of the proposed topology is analyzed in detail. Afterward, the topology is compared with similar topologies in literature. Finally, the feasibility of the proposed SL-qZSI is validated by simulations. A laboratory prototype based on a TMS320F28335 digital signal processor is developed.

II. CIRCUIT ANALYSIS OF THE PROPOSED SL-QZSI

Fig. 1 shows the proposed SL-qZSI, which consists of three inductors (L_1, L_2, L_3), three capacitors (C_1, C_2, C_3), and three diodes (D_1, D_2, D_3). A diode inside the switched-inductor cell of the SL-qZSI topology in [11] is replaced by a bootstrap capacitor. The operating principle of the proposed topology is similar to that of the classical SL-qZSI in [19]. The operating state can be simplified into two parts: shoot-through state and non-shoot-through state. Figs. 2 and 3 show the equivalent circuits of the proposed SL-qZSI in the two states.

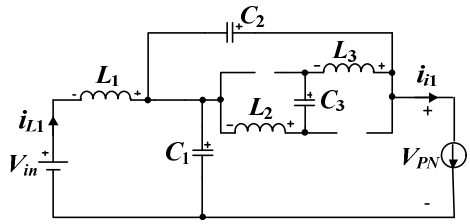


Fig. 3. Equivalent circuit of the proposed SL-qZSI in the non-shoot-through state.

All devices were assumed to be ideal, that is, L_1=L_2=L_3=L, C_1=C_2=C_3=C, to simplify the analysis. During the shoot-through state (Fig. 2), diodes D_2 and D_3 are on, whereas D_1 is off. L_2, L_3, and C_3 are connected in parallel. Capacitors C_1 and C_2 are discharged, whereas C_3 is charged. Inductors L_1, L_2, and L_3 store energy, and the corresponding voltages across L_1, L_2, and L_3 are V_{L1}, V_{L2}, and V_{L3}, respectively. The voltages across C_1, C_2, and C_3 are V_{C1}, V_{C2}, and V_{C3}, respectively, and the currents flowing through C_1, C_2, C_3, L_1, L_2, and L_3 are i_{C1}, i_{C2}, i_{C3}, I_{L1}, i_{L2}, and i_{L3}, respectively. i_{sh1} denotes the shoot-through current. Thus, we obtain

$$\begin{cases} V_{in}+V_{C2}=V_{L1} \\ V_{C1}=V_{C3}=V_{L2}=V_{L3} \\ i_{C1}=i_{L2}+i_{L3}+i_{C3} \\ i_{C2}=i_{L1} \\ i_{L2}=i_{L3} \\ i_{sh1}=i_{L1}+i_{L2}+i_{L3}+i_{C3} \end{cases}. \tag{1}$$

Similarly, in the non-shoot-through state (Fig. 3), diodes D_2 and D_3 are off, whereas D_1 is on. Capacitors C_1 and C_2 are charged, whereas C_3 is discharged. L_2, L_3, and C_3 are connected in series. Inductors L_1, L_2, and L_3 transfer energy from the DC voltage source to the load. i_{i1} denotes the non-shoot-through current. We can then obtain

$$\begin{cases} V_{in}+V_{L1}=V_{C1} \\ V_{C2}=V_{C3}+V_{L2}+V_{L3} \\ V_{PN}=V_{C1}+V_{C2} \\ i_{C1}=i_{L1}-i_{i1} \\ i_{C2}=i_{L2}-i_{i1} \end{cases}. \tag{2}$$

Based on the volt-second balance principle, we can obtain the voltage across inductor L_1 from period (1) to (2). Setting the interval of the shoot-through as DT and non-shoot-through as (1-D)T, we obtain

$$DT(V_{in}+V_{C2})=(1-D)T(V_{C1}-V_{in}). \tag{3}$$

Equation (3) can be revised as

$$V_{C1}=\frac{1}{1-D}V_{in}+\frac{D}{1-D}V_{C2}. \tag{4}$$

The voltages across L_2 and L_3 are equal in a period because of the symmetry of L_2 and L_3; that is, V_{L2}=V_{L3}=V_{C3} in the

shoot-through state and V_{L2}=V_{L3}=(V_{C2}-V_{C3})/2 in the non-shoot-through state. Therefore, by re-applying the volt-second balance principle to L_2 or L_3 from (1) and (2), we acquire

$$DTV_{C3} = \frac{1}{2}(V_{C2} - V_{C3})(1-D)T \,. \tag{5}$$

Equation (5) can be revised as

$$V_{C3} = \frac{1-D}{1+D} V_{C2} \,. \tag{6}$$

In a switching cycle, the voltage across the capacitor remains nearly unchanged, and the capacitor is equivalent to a voltage source. Thus, we obtain

$$V_{C1} = V_{C3} \,. \tag{7}$$

Substituting Equations (4) and (6) into (7) yields

$$\frac{1}{1-D} V_{in} + \frac{D}{1-D} V_{C2} = \frac{1-D}{1+D} V_{C2} \,. \tag{8}$$

Therefore, the voltage across capacitor C_2 can be described as

$$V_{C2} = \frac{1+D}{1-3D} V_{in} \,. \tag{9}$$

Substituting Equations (9) into (6) and (7) yields

$$V_{C1} = V_{C3} = \frac{1-D}{1-3D} V_{in} \,. \tag{10}$$

The peak DC link voltage across the main circuit (V_{PN}) expressed in Equation (2) can be rewritten as

$$V_{PN} = \frac{2}{1-3D} V_{in} \,. \tag{11}$$

Thus, the ratio between DC link voltage V_{PN} and input DC voltage V_{in} of the proposed inverter, called boost factor B, is defined by

$$B = \frac{2}{1-3D} \,. \tag{12}$$

According to Equation (12), the proposed SL-qZSI can obtain high voltage-conversion ratios when shoot-through duty ratio $D \leq 1/3$. Fig. 4 shows the boost factor versus the duty cycle for different topologies when simple boost control method is employed. Fig. 4 shows that the boost ability of the proposed SL-qZSI is significantly higher than that of the other two topologies in [11] and [19] with the same shoot-through interval. Therefore, at the same voltage conversion ratio, the proposed topology employs a high modulation index to improve inverter output performance. In conclusion, the proposed SL-qZSI is suitable for low-voltage power applications.

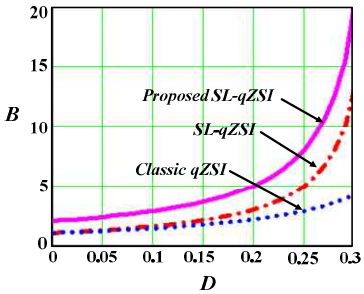


Fig. 4. Comparison of the boost ability of different topologies when simple boost control method is employed.

III. COMPARISON WITH PREVIOUS TOPOLOGIES

A. Voltage Gain

Compared with the simple boost and constant boost control methods, the maximum boost control method converts all zero states into shoot-through states without affecting the active state; thus, the largest possible voltage gain can be obtained for a given modulation index [6]. In the following comparisons, the maximum boost control method was used for the analysis. Simulations and experiments were conducted to verify the merits of the proposed topology. As described in [1], voltage gain G can be expressed as

$$\frac{\hat{V}_o}{V_{in}/2} = MB = G \,, \tag{13}$$

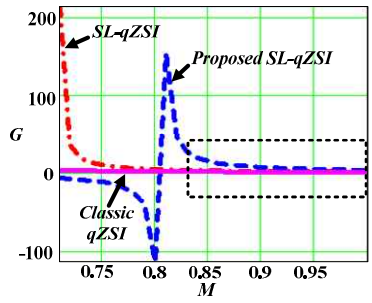
where $\hat{V}_o$ is the output peak phase voltage, V_{in} is the input DC voltage, M is the modulation index, and B is the boost factor. As shown in [6], when the maximum boost control method is used, the average duty cycle of shoot-through state D is described as

$$D = \frac{T_0}{T} = \frac{2\pi - 3\sqrt{3}M}{2\pi} \,, \tag{14}$$

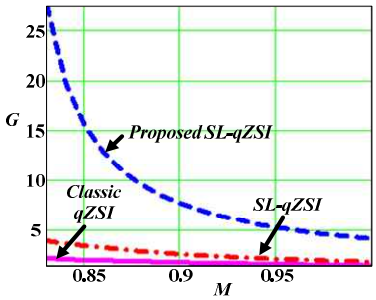
where T_0 is the shoot-through time interval over switching period T. Substituting Equations (12) and (14) into (13) provides voltage gain G of the proposed topology, which can be expressed as

$$G = M * B = \frac{4\pi M}{9\sqrt{3}M - 4\pi} \,. \tag{15}$$

Fig. 5(a) shows the voltage gain of the different topologies under maximum boost control. The dashed box in the figure is expanded and can be seen more clearly in Fig. 5(b). The abscissa in Fig. 5 refers to modulation index M, and the ordinate represents voltage gain G. The proposed SL-qZSI employs a higher modulation index and a shorter shoot-through duty cycle than the other two topologies in [11] and [19] to obtain the same voltage gain G. Thus, inverter output quality is improved.



(a)



(b)

Fig. 5. (a) Comparison of the voltage gain of the different topologies with maximum boost control method. (b) Expanded waveforms (dashed box).

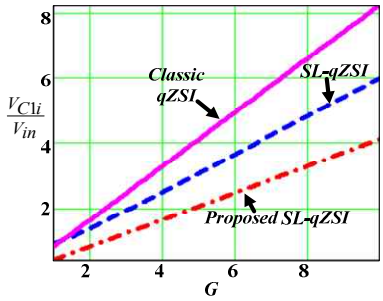


Fig. 6. Comparison of the voltage stress across C_1 in the different topologies with maximum boost control method.

B. Capacitor Voltage Stress

Capacitor voltage stress and inductor current ripple are important factors that affect the performance of qZSIs; they also determine the inverter cost and volume [8]. Therefore, the different qZSI topologies were compared in this study. To ensure a fair and valid comparison, all inverters were assumed to have the same input voltage V_{in} and output voltage V_o under the maximum boost control method; that is, all inverters have the same voltage gain G. From Equations (14) and (15), we can obtain modulation index M and shoot-through duty ratio D of the proposed SL-qZSI, both of which are defined by voltage gain G.

$$\begin{cases} M = \dfrac{4\pi G}{9\sqrt{3}G - 4\pi} \\ D = \dfrac{3\sqrt{3}G - 4\pi}{9\sqrt{3}G - 4\pi} \end{cases} \tag{16}$$

Substituting Equation (16) into (10), we can obtain the voltage stress across capacitor C_1 of the proposed topology shown in Fig. 1. The voltage stress across C_1 is described as

$$V_{C11} = \frac{3\sqrt{3}G}{4\pi} V_{in} . \tag{17}$$

Similarly, the capacitor voltages of the topologies mentioned in [11] and [19] (V_{C12} and V_{C13}, respectively) in the same position can also be replaced by voltage gain G with the same control method as follows:

$$\begin{cases} V_{C12} = \dfrac{6\pi\sqrt{3}M_1}{24\pi\sqrt{3}M_1 - 27{M_1}^2 - 8\pi^2} V_{in} \\ V_{C13} = \dfrac{3\sqrt{3}G}{2\pi} V_{in} \end{cases} . \tag{18}$$

Modulation index M_1 of the SL-qZSI topology in [19] is described as

$$M_1 = \frac{-b + \sqrt{b^2 + 4ac}}{2a} , \tag{19}$$

where the respective coefficients can be rewritten as

$$\begin{cases} a = 6\sqrt{3}\pi - 27G \\ b = 24\sqrt{3}\pi G - 8\pi^2 \\ c = 8\pi^2 G \end{cases} . \tag{20}$$

Fig. 6 shows the voltage stress of capacitor C_1 in the different topologies. The abscissa refers to voltage gain G, and the ordinate denotes the ratio of capacitor voltage stress V_{c1i} (i = 1, 2, 3) and input voltage V_{in}. Compared with that in the other two topologies, the voltage stress across C_1 in the proposed SL-qZSI is lower under the same voltage gain.

Similar to the analysis for capacitor C_1, Equation (16) is substituted into (9) to obtain the capacitor voltage stress across C_2 for the proposed SL-qZSI, SL-qZSI, and classic qZSI as described by Equation (21) below.

$$\begin{cases} V_{C21} = \dfrac{3\sqrt{3}G - 2\pi}{2\pi} V_{in} \\ V_{C22} = \dfrac{8\pi^2 - 12\pi\sqrt{3}M_1}{24\pi\sqrt{3}M_1 - 8\pi^2 - 27{M_1}^2} V_{in} \\ V_{C23} = \dfrac{3\sqrt{3}G - 2\pi}{2\pi} V_{in} \end{cases} \tag{21}$$

Fig. 7 shows the capacitor voltage stress across C_2 in the three topologies. With the same voltage gain, the voltage stress across C_2 in the three topologies is exactly the same.

C. Inductor Current Ripple

Given that the input and output voltages of the different topologies are similar, the input current ripple of the inductor

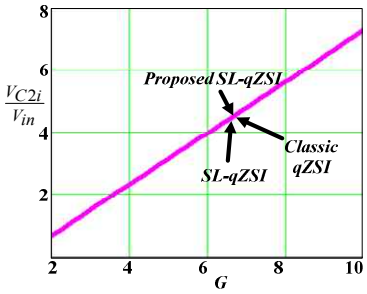


Fig. 7. Comparison of the voltage stress across C_2 in the different topologies with maximum boost control method.

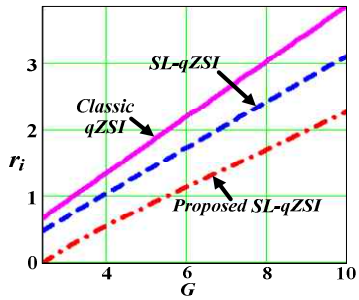


Fig. 8. Comparison of the input current ripples of the different topologies with maximum boost control method.

must be different under the same control method. In the shoot-through state shown in Fig. 2, the voltage across inductor L_1 can be expressed as

$$L\frac{di_{L1}}{dt} = v_{in} + v_{c2}\,. \tag{22}$$

Therefore, the current ripple of L_1 can be described as

$$\left|\Delta I_{11}\right| = \frac{(V_{in} + V_{C2})DT}{L}\,. \tag{23}$$

Substituting Equation (9) into (23), we can obtain the inductor current ripple of the proposed topology as follows:

$$\left|\Delta I_{11}\right| = \frac{(2-2D)D}{(1-3D)}\frac{TV_{in}}{L}\,. \tag{24}$$

Similarly, the inductor current ripple of the other two topologies in [11] and [19] can be described as

$$\begin{cases} \left|\Delta I_{12}\right| = \dfrac{(1-D_1{}^2)D_1}{(1-D_1{}^2-2D_1)}\dfrac{TV_{in}}{L} \\ \left|\Delta I_{13}\right| = \dfrac{(1-D_2)D_2}{(1-2D_2)}\dfrac{TV_{in}}{L} \end{cases}, \tag{25}$$

where

$$\begin{cases} D_1 = \dfrac{2\pi - 3\sqrt{3}M_1}{2\pi} \\ D_2 = \dfrac{3\sqrt{3}G - 2\pi}{6\sqrt{3}G - 2\pi} \end{cases}. \tag{26}$$

Rearranging the inductor current ripple of the three topologies, we obtain

$$\left|\Delta I_{1i}\right| = r_i * \frac{TV_{in}}{L}(i = 1,2,3)\,, \tag{27}$$

where r_i is the inductor current ripple coefficient that can be described as

$$\begin{cases} r_1 = \dfrac{(2-2D)D}{(1-3D)} \\ r_2 = \dfrac{(1-D_1{}^2)D_1}{(1-D_1{}^2-2D_1)} \\ r_3 = \dfrac{(1-D_2)D_2}{(1-2D_2)} \end{cases}. \tag{28}$$

Fig. 8 shows the inductor current ripples of the three topologies. The inductor current ripple of the proposed SL-qZSI is smaller than that of the other two topologies with the same voltage gain G.

D. Switch Voltage Stress and Diode Reverse Voltage

The voltage stress in the switching devices is related to DC bus voltage V_{PN} for qZSI. Therefore, substituting Equation (16) into (11) provides DC link voltage V_{PN1} of the proposed SL-qZSI.

$$V_{PN1} = \frac{9\sqrt{3}G - 4\pi}{4\pi}V_{in} \tag{29}$$

The DC link voltages of SL-qZSI and classic qZSI can also be described as V_{PN2} and V_{PN3}, respectively.

$$\begin{cases} V_{PN2} = \dfrac{8\pi^2 - 6\sqrt{3}\pi M_1}{-8\pi^2 + 24\sqrt{3}\pi M_1 - 27M_1{}^2}V_{in} \\ V_{PN3} = \dfrac{6\sqrt{3}G - 2\pi}{2\pi}V_{in} \end{cases}. \tag{30}$$

The power diode provides uncontrolled rectification in power conversion applications, and its switching phenomenon, which contains forward and reverse recovery, determines the power losses when operating at high frequency. The reverse voltage of a diode is an important factor that affects the reverse recovery; thus, it is worth mentioning as well[21]. In the shoot-through state (Fig. 2), the D_1 reverse voltage of the proposed topology, V_{D11}, can be described as

$$V_{D11} = V_{PN1} = \frac{2}{1-3D}V_{in}\,. \tag{31}$$

In the non-shoot-through state (Fig. 3), the D_2 and D_3 reverse voltages of the proposed topology, V_{D21} and V_{D31}, can be described as

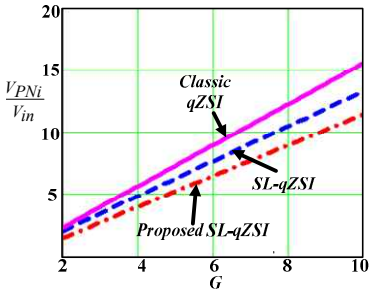


Fig. 9. Comparison of the DC bus voltages of the different topologies with maximum boost control method.

$$V_{D21} = V_{D31} = \frac{D}{1-3D} V_{in} . \tag{32}$$

From Equations (31) and (32), we can conclude that diode D_1 in the proposed topology withstands high reverse voltage that is equal to DC link voltage V_{PN1}. The maximum reverse voltages in the diodes of the other two topologies are V_{D12} and V_{D13}, which are also equal to DC link voltages V_{PN2} and V_{PN3}.

Fig. 9 shows the comparison of the device voltage stress and maximum diode reverse voltage of the three topologies. The abscissa refers to voltage gain G, and the ordinate denotes the ratio of DC bus voltage V_{PNi} (i=1,2,3) and input voltage V_{in}. With the same voltage gain G, the proposed SL-qZSI has lower voltage stress and diode reverse voltage across the switching devices than the other two topologies. This condition is extremely beneficial for high voltage gain applications.

E. Shoot-Through Current and Efficiency

Shoot-through current is an important factor that affects the choice of switching devices and the power loss of the inverter. Therefore, the shoot-through currents of the three topologies were analyzed. To simplify the analysis, we assumed that the inductor current is basically constant in a given period. Applying the volt-second balance principle to the capacitors, from (1) and (2), we can obtain

$$\begin{cases} 2D(i_{L2} + i_{C3}) = (1-D)(i_{L1} - i_{i1}) \\ Di_{L1} = (1-D)(i_{L2} - i_{i1}) \end{cases} . \tag{33}$$

Simplifying Equation (33) and substituting it into (1), we obtain

$$I_{sh1} = \frac{3+D}{1+D} i_{L1} + \frac{1-3D}{1+D} i_{C31} . \tag{34}$$

In the same manner, the shoot-through currents of SL-qZSI and classic qZSI (I_{sh2} and I_{sh3}), which are described by inductor current i_{L12} and i_{L13}, are expressed as

$$\begin{cases} I_{sh2} = \frac{3+D_2}{1+D_2} i_{L12} \\ I_{sh3} = 2i_{L13} \end{cases} . \tag{35}$$

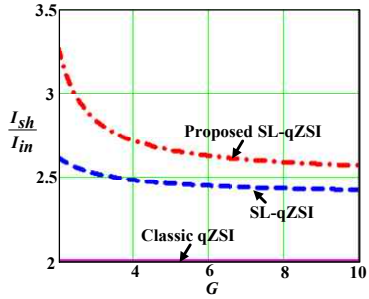


Fig. 10. Comparison of the shoot-through current of the three topologies.

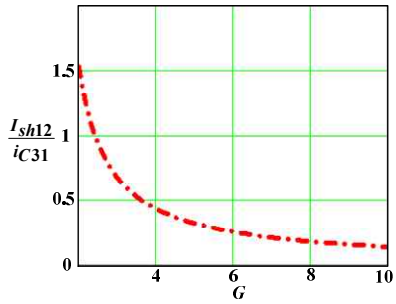


Fig. 11. Polarity judge of I_{sh12}.

To facilitate the analysis, we assumed that no power losses occur in the three topologies. Given that the input and output voltages are similar, the three topologies have the same input and output power. Therefore, the inductor L_1 currents of the three topologies are similar and thus indicates that i_{L1}=i_{L12}=i_{L13}=I_{in}. I_{in} stands for the average value of the input current. Moreover, the first part of I_{sh1} [I_{sh11}=(1-3D)*i_{L1}/(1+D)] was utilized to compare the other two shoot-through currents. D and D_2 were then substituted with Equations (16) and (26), respectively.

Fig. 10 shows the comparison of the shoot-through currents of the three topologies. The abscissa refers to voltage gain G, and the ordinate denotes the ratio of shoot-through current I_{sh} and input current I_{in}. The first part of I_{sh1} is larger than that of I_{sh2} and I_{sh3}.

Fig. 11 shows that the second part of I_{sh1} [I_{sh12}=(3+D)*i_{C1}/(1+D)] is positive. With a given range of voltage gain, the ratios of I_{sh12} and i_{C1} are always greater than zero, which means that the shoot-through current I_{sh1}=I_{sh11}+I_{sh12}>I_{sh2}>I_{sh3}. Therefore, the shoot-through current of the proposed topology is larger than that of the other two topologies.

Fig. 12 shows the relationship between the voltage gain and shoot-through duty ratio of the three topologies. The shoot-through duty ratio of the proposed topology is much smaller than that of the other two topologies and nearly less than half of classic qZSI to obtain the same voltage gain. Thus, the power loss in the proposed topology may be small because of the drop forward of IGBTs and the parasitic impedance of the components and the wire.

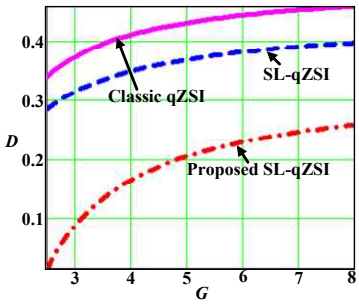


Fig. 12. Relationship between the voltage gain and shoot-through duty ratio of the three topologies.

TABLE I

SIMULATION PARAMETERS FOR qZSI

Input DC voltage		48 *V*
Quasi Z-source network	*L*	1 *mH*
	C	2200 *μF*
Switching frequency		10 *kHz*
Three-phase output filter	L_f	1 *mH*
	C_f	20 *μF*

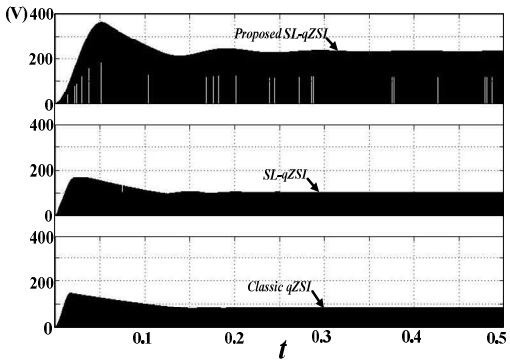


Fig. 13. Simulation results of DC link voltages based on the different topologies with simple boost control method.

IV. SIMULATION RESULTS

The merits of the proposed SL-qZSI shown in Fig. 1 were verified. The simulation results shown in Figs. 13 to 17 compare the performance of the proposed SL-qZSI with that of SL-qZSI and qZSI in [11] and [19]. Table 1 provides the list of the simulation parameters for the three topologies.

Fig. 13 shows the DC bus voltages of the three topologies when simple boost control method is employed. The shoot-through duty ratio is 0.2. The DC bus voltage of the proposed topology is higher than that of the other two topologies and thus indicates that the proposed topology has stronger boost ability. As shown in Fig.14, in the steady state, V_{PN} is boosted to 240 *V* when input DC voltage V_{in} is 48 *V* and the output phase voltage peak value is 90 *V*. V_{C1} and V_{C2} of the proposed SL-qZSI are boosted to 96 and 144 *V*, respectively, similar to the analysis.

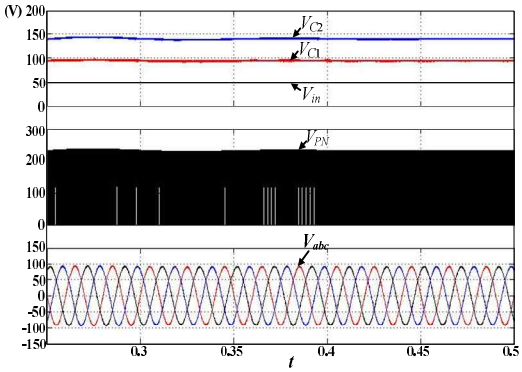


Fig. 14. Simulation results of the proposed topology with simple boost control method.

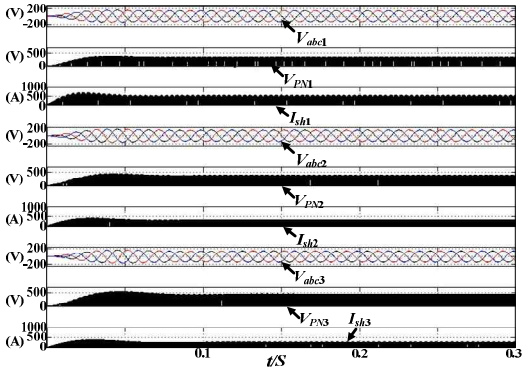


Fig. 15. Simulation results of DC link voltages, output voltages, and shoot-through currents of the different topologies with maximum boost control method.

Figs. 15 to 17 show the simulation results for the three topologies when maximum boost control is used to produce the same input and output voltages. Fig. 15 shows the simulation results for the three phase voltages, shoot-through currents, and DC link voltages for the proposed SL-qZSI, SL-qZSI, and classic qZSI when M_1=0.92, M_2=0.78, and M_3=0.67, respectively. The output phase voltage is 110 *V* (RMS), and the phase resistive load is 5.5 Ω. When the output phase voltages of the three topologies are almost similar, the DC bus voltage of the proposed topology becomes the lowest. This result means that the voltage stress across the IGBTs of the proposed topology is smaller than that of the other two topologies. However, the shoot-through current of the proposed topology is larger than that of the other two topologies.

Fig. 16 shows the input inductor currents and capacitor voltages across C_1 and C_2. In the steady state, the amplitude of the input current ripple and the voltage stress across C_1 of the proposed topology are both less than those of the other two topologies. The voltages across C_2 of the three topologies are similar. The simulation results are in good agreement with the theoretical analysis results.

Fig. 17 shows the input inductor current ripples, diode reverse voltages, and shoot-through currents of the three

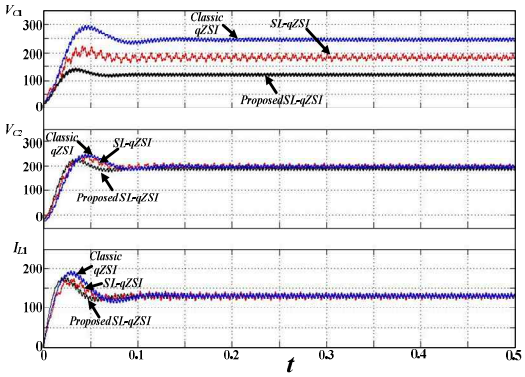


Fig. 16. Simulation results of the different topologies with maximum boost control method.

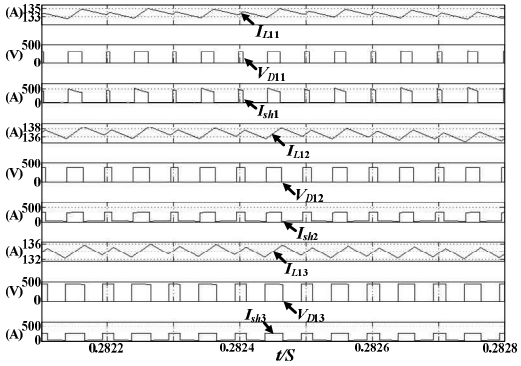


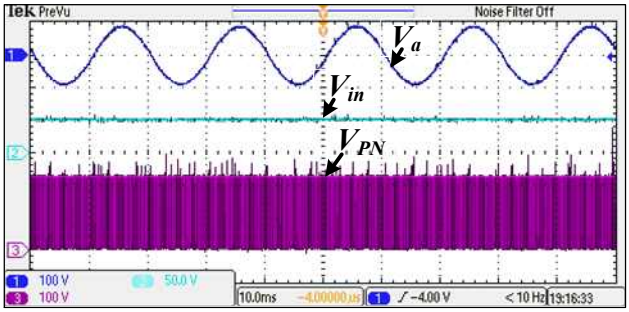
Fig. 17. Simulation results of input current ripples, diode reverse voltages, and shoot-through currents of the three topologies with maximum boost control method.

topologies. The maximum current ripples of the proposed SL-qZSI, SL-qZSI, and classic qZSI are 2.5, 3.0, and 3.5 A, respectively. The input current ripple of the proposed topology is the smallest. The diode reverse voltages are mostly equal to the DC link voltages, and the diode of the proposed topology bears lower reverse voltage. The shoot-through current of the proposed topology is the largest. All simulation results concur with the theoretical analysis.

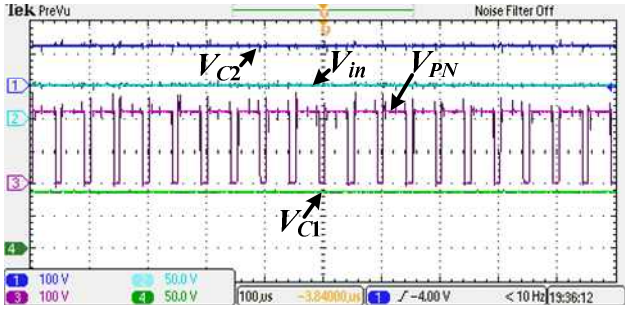
V. Experimental Results

Experiments were conducted on the three topologies with the same parameters (Table 1) to verify the properties of the proposed SL-qZSI. Fig. 18 shows the experimental results for the proposed inverter by using the simple boost control method when the shoot-through duty ratio is 0.2. In Fig. 18(a), V_{PN} is boosted to 221 V when input voltage V_{in} is 48 V and the output phase voltage peak value is 100 V. In Fig. 18(b), V_{C1}, V_{C2}, and V_{PN} are boosted to 89, 125, and 220 V, respectively. These experimental results concur with the theoretical analysis and simulation results.

Figs. 19 to 21 show the experimental results for the three topologies when the maximum boost control method is used. To produce the same phase voltage (100 V/peak value), the



(a)



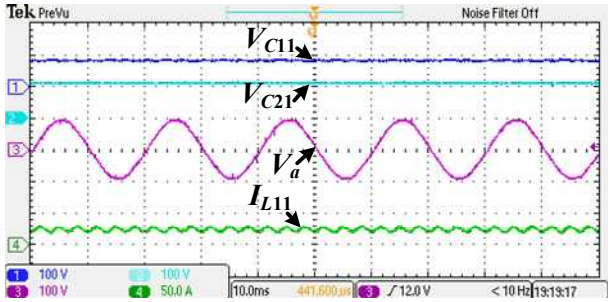
(b)

Fig. 18. Experimental results of the proposed topology with simple boost control method when D=0.2. (a) From top to bottom: output phase voltage, input DC voltage, and DC link voltage. (b) From top to bottom: capacitor C_2 voltage, input DC voltage, DC link voltage, and capacitor C_1 voltage.

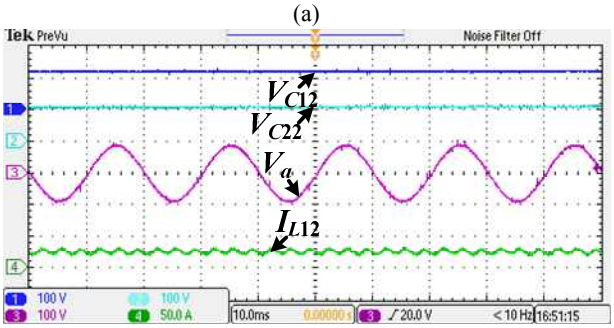
modulation index for the proposed SL-qZSI, SL-qZSI, and classic qZSI is M_1=0.93, M_2=0.723, and M_3=0.63, respectively. A 15Ω/phase resistive load was utilized in the experiment to reduce the current in the power circuit. The voltage across C_1 for the proposed SL-qZSI, SL-qZSI, and classic qZSI is 80, 120, and 160 V, respectively, as shown in Fig. 19. Thus, capacitor C_1 of the proposed topology withstands low voltage. Moreover, the voltages across C_2 for the three topologies are almost 110 V.

The DC link voltage for the proposed SL-qZSI, SL-qZSI, and classic qZSI is 200, 240, and 260 V, respectively, as shown in Fig. 20. The proposed topology achieves low DC link voltage. In the three topologies, the diode reverse voltages are mostly equal to the DC link voltage. Furthermore, the shoot-through current of the proposed topology is larger than that of other two topologies.

Fig. 21 shows that with the same voltage gain, the shoot-though time of the proposed topology is much less than that of the other two topologies although the shoot-through current of the proposed topology is slightly larger. Therefore, the power loss produced by the forward drop of IGBT as well as the parasitic impedance of the components and line is smaller in the proposed topology than in the other two topologies. Fig. 22 shows the comparison of the experimental efficiency of the three topologies under maximum boost control. The proposed SL-qZSI can obtain high conversion efficiency because of its small shoot-through duty ratio.



(a)



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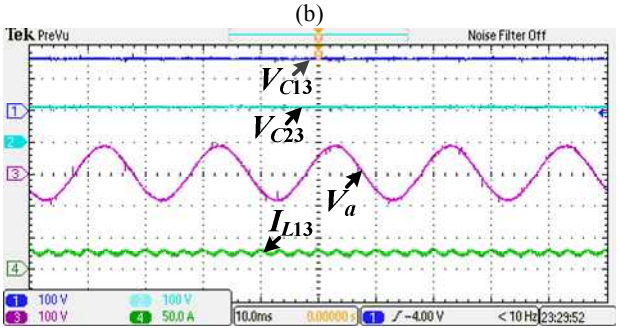
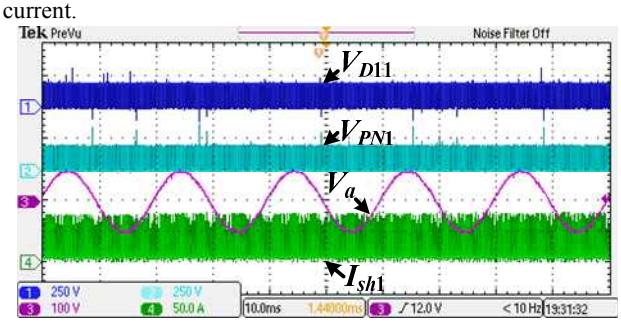
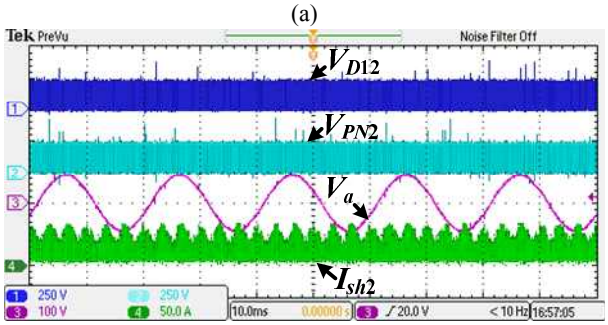


(c)

Fig. 19. Experimental results of the three topologies with maximum boost control method when (a) M_1=0.93, (b) M_2=0.723, and (c) M_3=0.63. From top to bottom: capacitor C_1 voltage, capacitor C_2 voltage, output phase voltage, and input inductor L_1 current.



(a)



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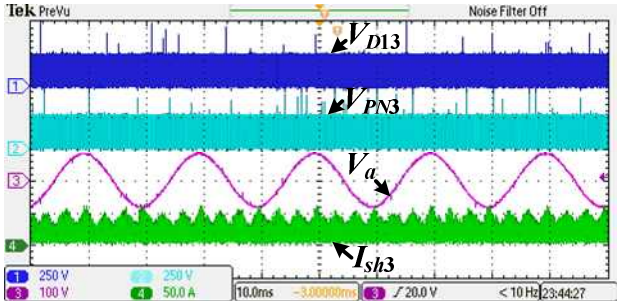
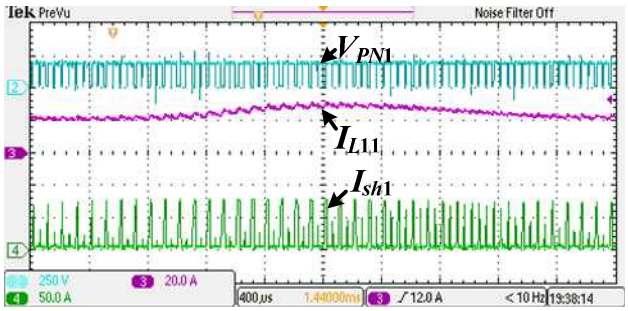
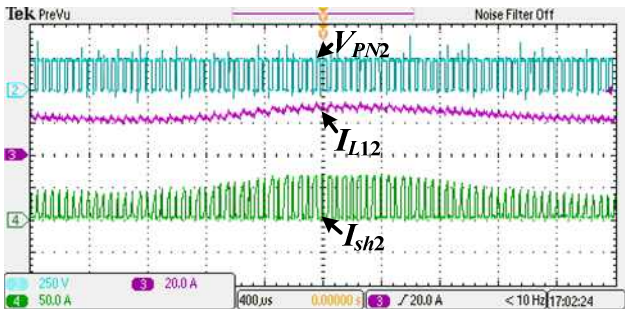


(c)

Fig. 20. Experimental results of the three topologies with maximum boost control method. From top to bottom: diode reverse voltage, DC link voltage, output voltage, and shoot-through current.



(a)



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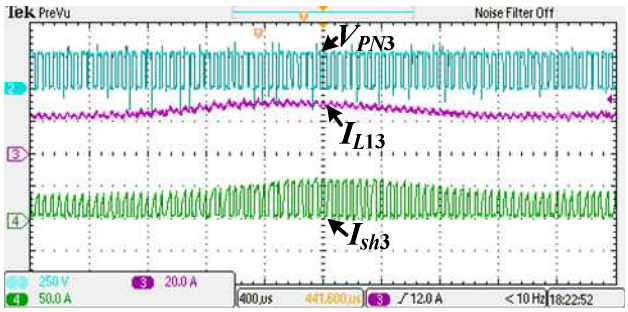

(c)

Fig. 21. Experimental results of the three topologies with maximum boost control method. From top to bottom: DC link voltage, input inductor L_1 current ripple, and shoot-though current.

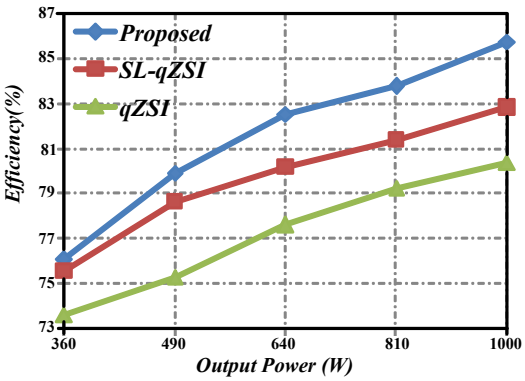

Fig. 22. Comparison of the efficiency of the three topologies under maximum boost control.

VI. CONCLUSIONS

A novel switch-inductor SL-qZSI with strong boost ability was presented in this paper. Compared with the other SL-qZSIs, the proposed topology offers lower capacitor voltage stress, diode reverse voltage, and input current ripple as well as lower voltage stress in the switching devices with the same input and output voltages. To obtain the same voltage gain, the proposed topology uses a modulation index higher than that of the other two topologies. Thus, the quality of the output waveform is improved. The proposed topology can also achieve high conversion efficiency. The effectiveness of the proposed SL-qZSI was verified by simulations and experiments with both the simple boost and maximum boost control methods. According to these methods, the proposed SL-qZSI is a promising candidate in distributed generation applications of low-voltage sources, such as fuel and photovoltaic cells.

ACKNOWLEDGEMENTS

This work was supported by the Science and Technology Support Program of Jiangsu Province, China (Grant No. BE2012036).

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