http://dx.doi.org/10.11142/jicems.2014.3.4.465


# A New Controllable Active Clamp Algorithm for Switching Loss Reduction in a Module Integrated Converter System

**Chang-Seok Park*, and Tae-Uk Jung***

**Abstract – This paper proposes a new switching algorithm for an active clamp snubber to improve the efficiency of a module integrated converter system. This system uses an active clamp method for the snubber circuit for the efficiency and reliability of the system. However, the active clamp snubber circuit has the disadvantage that system efficiency is decreased by switch operating time because of heat loss in resonance between the snubber capacitor and leakage inductance. To address this, this paper proposes a new switching algorithm. The proposed algorithm is a technique to reduce power consumption by reducing the resonance of the snubber switch operation time. Also, the snubber switch is operated at zero voltage switching by turning on the snubber switch before main switch turn-off. Simulation and experimental results are presented to show the validity of the proposed new active clamp control algorithm.**

**Keywords: Controllable active clamp, Module integrated converter (MIC), Snubber, Switching algorithm, Zero voltage switching (ZVS)**

## 1. Introduction

Renewable energy system research has been conducted actively for many years on issues such as depletion of fossil energy and environmental pollution. A module integrated converter (MIC) should be developed with reliability and high efficiency at a size suitable for smaller systems [1, 3]. The single-phase stand-alone type converter (SPSC) is very important for MIC systems, such as photovoltaic (PV), fuel cells, and batteries, especially in developing countries, remote areas, and mountainous regions [4, 5]. The switching control method of the DC-DC boost converter is a key component in SPSC control and will impact the reliability, stability, and power quality of single-phase systems [6].

Previous studies have dealt mostly with performance improvements of SPSC systems under soft switching, such as zero-voltage switching (ZVS) and zero-current switching (ZCS) conditions [7, 9]. Voltage stress is caused by voltage spikes in the switching device and can seriously impact the performance of the SPSC. Due to issues inherent in voltage stress, the efficiency of the SPSC systems may be degraded. Generally, the DC-DC converter of a renewable energy conversion system is designed as a flyback converter because the output voltages of PV, fuel cells, and batteries are low [10, 11]. In the case of a flyback converter, the voltage spike is caused by the stored energy in the leakage inductance of the primary transformer when the primary switching device turns off. This voltage spike generates switching losses and serious noise in the SPSC systems. Thus, a snubber circuit is also required to reduce the voltage spike [12]. This paper is focused on voltage spike reduction.

* Dept. of Electrical Engineering, Kyungnam University, Korea. (chang8793@naver.com)

* Corresponding Author, Dept. of Electrical Engineering, Kyungnam University, Korea. (tujung@kyungnam.ac.kr)

Received 17 October 2014; Accepted 9 November 2014

## 2. Analysis of module integrated converter

### 2.1 Interleaved control method

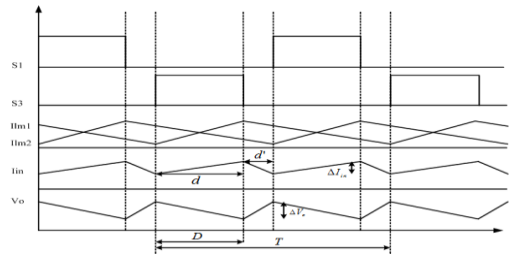


**Fig. 1.** Output voltage and input current ripple waveform of the interleaved control method

The interleaved control is plotted in Fig. 1. The two signals, S1, S2, have a phase delay of 2pi/N following the

number (N) of the single converter stage in parallel, and they have the same switching frequency.

The rated current of a switching device and current stress are reduced by following a single converter stage. Moreover, the ripple frequency is increased by N times because the input current of each single stage converter overlaps, so the ripple is decreased.

Based on the average value of the output current, the output voltage ripple can be calculated as follows:

$$\begin{aligned} \Delta Q &= I_{out} DT \\ \Delta V_{ripple} &= \frac{\Delta Q}{C} = \frac{V_{out} D}{RC} T \\ \Delta V_{ripple} &= \frac{V_{out} D}{RC} \frac{1}{f} \frac{1}{N} \end{aligned} \tag{1}$$

Where $I_{out}$, $D$, $T$, and $f$ are the output current, duty ratio, switching period, and switching frequency, respectively.

### 2.2 Conventional active clamp snubber

The conventional RCD snubber circuit has the disadvantage that thermal losses are caused by the resistor. However, an active clamp snubber circuit using a switch device can remove the voltage spike without thermal losses. Fig. 2 shows a conventional active clamp snubber.

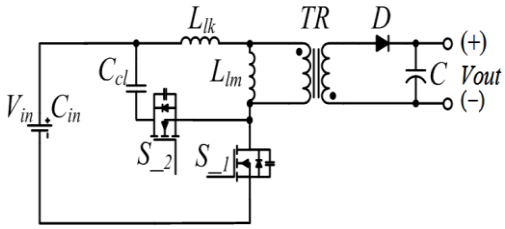


**Fig. 2.** Conventional active clamp snubber

The voltage spike in the conventional active clamp snubber is decreased by charging in the clamp capacitor. Thus, an active clamp will have higher efficiency than a RCD snubber because of smaller losses caused by resistor thermal losses.

The voltage spike in this method is charged automatically through the body diode of the MOSFET when the voltage spike occurs. However, switch losses are generated by the hard switching when turning on the MOSFET to discharge the energy stored in the clamp capacitor. Also, the controller algorithm for turning off the MOSFET is a complex system.

### 2.3 Proposed controllable interleaved active clamp snubber

The proposed controllable interleaved active clamp flyback converter is shown in Fig. 3. Using the interleaved method, connecting the two flyback converters in parallel, increases the input current distribution and switching frequency. The size of the transformer core can be reduced and the output current ripple should decrease.

The leakage inductance current is charged to the clamp capacitor because the clamp capacitor is sufficiently larger than the body capacitor of the MOSFET. Thus, selection of the value of the clamp capacitor is necessary, based on the design of the leakage inductance of the transformer. The clamp capacitor can be calculated as follows (2).

$$C_{cl} = \frac{(1 - D_{\max})^2}{\pi^2 L_{lk} f_{sw}} \tag{2}$$

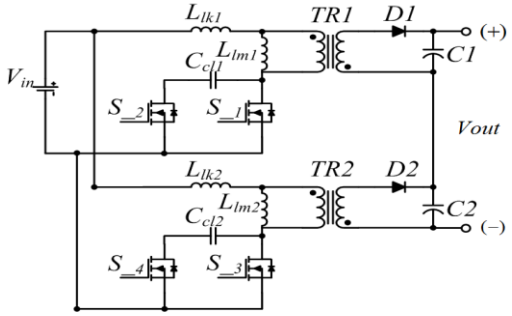


**Fig. 3.** Controllable interleaved active clamp snubber

If the value of the clamp capacitor is higher, it is possible to minimize the voltage spikes. However, the primary side voltage of the transformer will be decreased by the voltage divider. If the clamp capacitor is too large, the performance will not be improved. So, the clamp capacitor is preferably designed to be as small as possible.

The proposed interleaved active clamp snubber has L-C resonance between the clamp capacitor and the leakage inductance when turning on the clamp switch S2. The L-C resonance causes the temperature-rising losses of transformers. At this time, the L-C resonance frequency can be calculated as follows (3).

$$f_o = \frac{1}{2\pi\sqrt{L_{lk} C_{cl}}} \tag{3}$$

To reduce the L-C resonance, the clamp switch is turned off between the second and third quadrant; the voltage is discharged after charging, during the first period of resonance in the snubber capacitor shown Fig. 4. Thus, the optimal turn-on duty period of the clamp switch is calculated by the sum of 1/4 resonance period and the period of the main and clamp switch simultaneously

turning on. This duty period can be written as in equation (4).

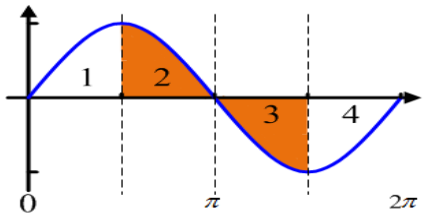


**Fig. 4.** Period of the L-C resonance frequency

$$S_{2,4}on = S_{overlapping} + \frac{\pi}{2}\sqrt{L_{lk}C_{cl}} \tag{4}$$

Figure 5 shows the operation mode of the controllable interleaved active clamp flyback converter[13, 14]. The switching pattern used is the same as in Fig. 6. Mode 1 [*to ~ t1*]: During the interval from $t_0$ through $t_1$, the main switch *S1* is conducting and the clamp switch *S2* is open. Therefore, the currents $I_{S1}$ and $I_{lk1}$ increase linearly. At this time, if the turn-on time of *S1* is $t_{on}$, the primary current $I_{lm}$ of the transformer can be calculated as follows (5).

$$I_{lm1} = \frac{V_{in}}{L_{lm1}} t_{on} \tag{5}$$

The stored energy in the primary winding inductance of the transformer can be stated in the following equation (6).

$$p = \frac{1}{2} L_{lm1} I_{lm1}^{\ 2} = \frac{V_{in}^{\ 2} t_{on}^{\ 2}}{2L_{lm1}} f_{sw} \tag{6}$$

Where $L_{lm1}$, $I_{lm1}$, and $f_{sw}$ are the magnetic inductance of the primary transformer, the leakage inductance of the primary transformer, and the switching frequency of *S1*, respectively. During this time, the output capacitor *C1*, *C2* deliver the required energy to the load. Mode 2 [*t1 ~ t2*]: The main switch *S1* is open and the clamp switch *S2* is conducting with ZVS. The current flowing through the main switch *S1* will be reduced to zero, but a voltage spike is generated due to the change of current flowing through the leakage inductance $I_{lk1}$. Thus, $V_{ds}(s)$ can be written as follows (7).

$$V_{ds1}(t) = V_{in} + L_{lk1}\frac{di_{lk1}(t)}{dt} + \frac{N1_1}{N2_1}V_{out} \tag{7}$$

However, because clamp switch *S2* is conducting, the voltage spike generated by leakage inductance is charged in the clamp capacitor. Thus, $V_{ds}(s)$ is the same as in equation (7). During this time, the output diode *D1* becomes forward-biased as the voltage across the transformer secondary becomes positive.

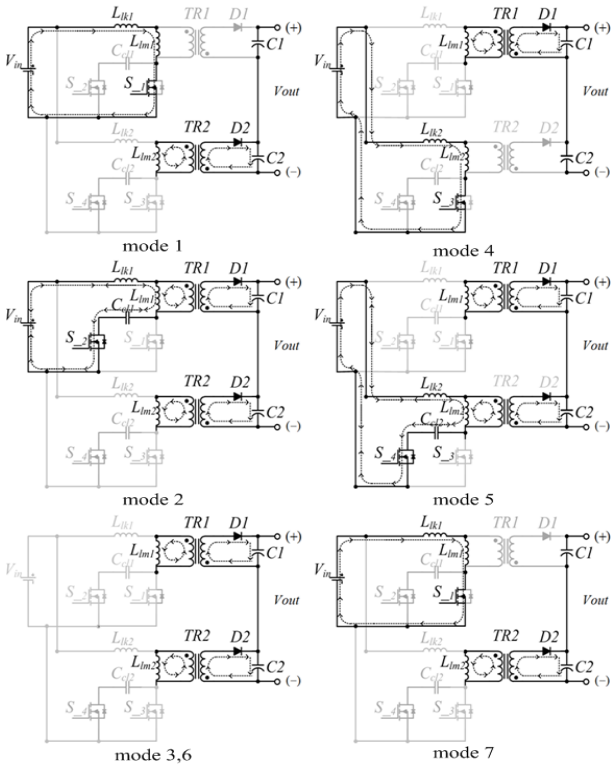


**Fig. 5.** Operation mode of controllable interleaved active clamp flyback converter

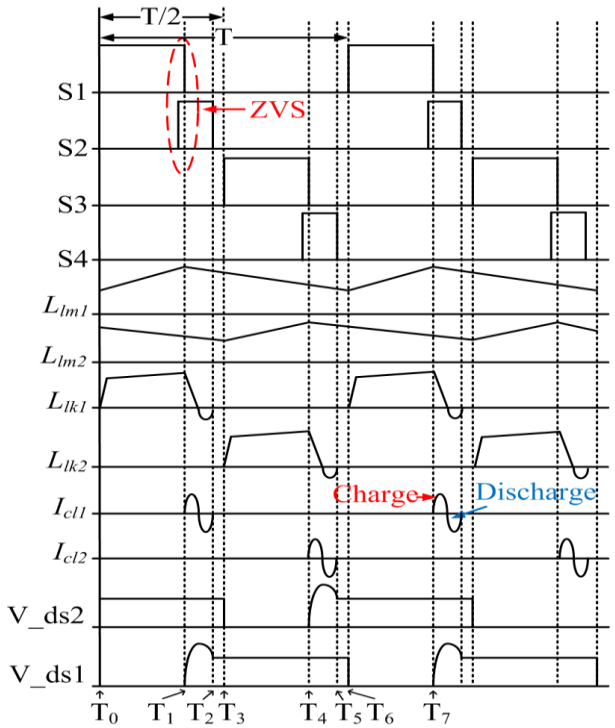


**Fig. 6.** Waveform characteristics of each mode

$$V_{ds1}(t)=\left\{V_{in}+L_{lk1}\frac{di_{lk1}(t)}{dt}+\frac{N1_1}{N2_1}V_{out}\right\}-V_{cl1} \quad (8)$$

Mode 3 [*t2* ~ *t3*]: The energy stored in the core is transferred to the secondary, which charges the output capacitor and provides energy to the load. The transformer secondary current is decreased in the ratio of 1/2 from the maximum value of the secondary current, and can be represented as follows (9).

$$i_{2out}=i_{2\max}-\frac{V_{2out}}{L_{lm2}}t_{off} \quad (9)$$

In this interval, the average value of the load current is calculated according to equation (9) as the average of the current period. Also, the output voltage, according to the duty ratio, is expressed as in equation (10, 11).

$$\begin{aligned} i_{2out}&=\frac{1}{t_{on}+t_{off}}\int_0^{t_{off}} i_2 dt=\frac{1}{T}\int_0^{t_{off}}\left(i_{2\max}-\frac{V_{2out}}{L_{lm2}}t_{off}\right)dt \\ &=\frac{1}{T}\left[i_{2\max}t_{off}-\frac{V_{out}{t_{off}}^2}{2L_{lm2}}\right]=\frac{i_{2\max}t_{off}}{2T} \end{aligned} \quad (10)$$

$$\begin{aligned} V_{in}DT&=\frac{N2}{N1}V_{out}(1-D)T \\ V_{out}&=\frac{D}{1-D}\frac{N1}{N2}V_{in} \end{aligned} \quad (11)$$

Mode 4 [*t3* ~ *t4*]: The under converter stage is operated, as in Mode 1. Mode 5 [*t4* ~ *t5*]: The under converter stage is operated as in Mode 2. Mode 6 [*t5* ~ *t6*]: The under converter stage is operated as in Mode 3.

## 3. Analysis of simulation and experiment

To confirm the theoretical analysis of the proposed control strategy, a simulation circuit under ideal conditions is presented in Fig. 7, using the PSIM software. The key parameters of the simulation are given in Table 1.

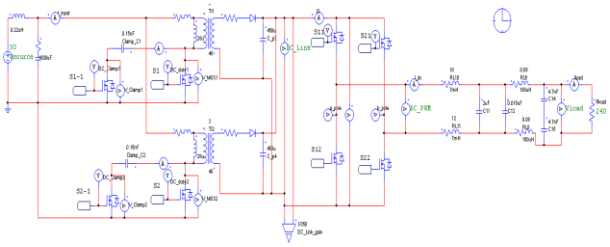

**Fig. 7.** Simulation circuit of controllable interleaved active clamp flyback converter

**Table 1.** Specification of the flyback converter

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{in}$ | Input voltage | 12-30 | $V_{dc}$ |
| $V_{out}$ | Output voltage | 220 | $V_{rms}$ |
| $C_{cl1,2}$ | Clamp capacitor | 0.15 | *uF* |
| $L_{lk1,2}$ | Leakage inductance | 0.1 | *mH* |
| $L_{lm1,2}$ | Magnetic inductance | 28 | *mH* |
| $n$ | Turn ratio of transformer | 3 : 48 | *Turn* |
| $C_{link1,2}$ | DC_Link capacitor | 470 | *uF* |
| $L_{f1,2}$ | Filter inductance | 7 | *mH* |
| $C_{f1,2}$ | Filter capacitor | 2 | *uF* |
| $f_{dc}$ | Converter switching frequency | 60 | *kHz* |
| $f_{inv}$ | Inverter switching frequency | 10 | *kHz* |
| $P_{out}$ | Rated output power | 400 | *W* |

The simulation results considering the leakage inductance were analyzed to demonstrate the theoretical analysis and the effects.

Figure 8 shows the simulation result of a conventional flyback converter. It presents the voltage spike wave form caused by the leakage inductance. The peak voltage values were 150-170[V].

Figure 9 displays the simulation result of the active clamp flyback converter considering L-C resonance. The peak voltage value was decreased markedly, to 70[V]. The ringing phenomenon was also removed.

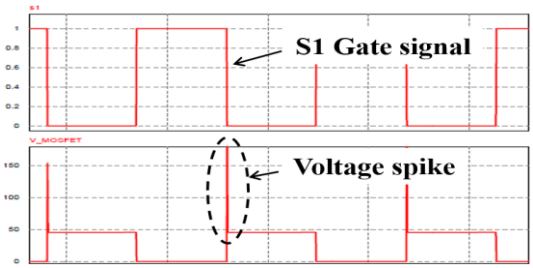


**Fig. 8.** Vds and S1 waveform of the conventional flyback converter

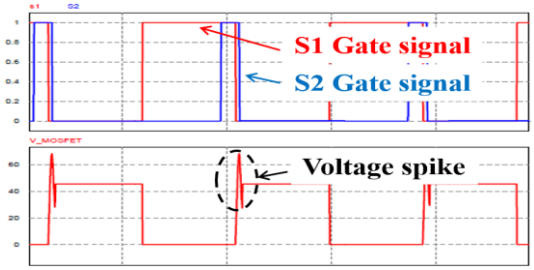


**Fig. 9.** Vds and S1 waveform of the active clamp flyback converter

Figure 10 presents the output voltage waveform. It can be seen that at 220 [V] and 60 [Hz], the output current is in phase with the output voltage.

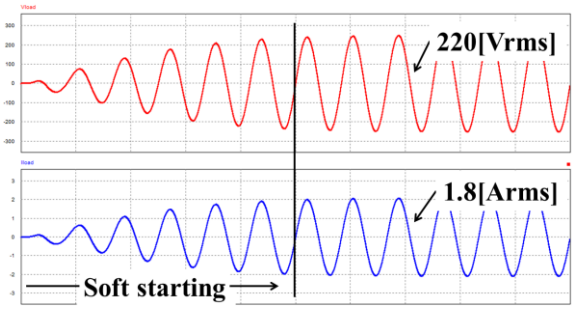


**Fig. 10.** Output waveform of the proposed MIC

Figure 11 presents the control algorithm flow chart of the DC link voltage. For the desired output voltage, the calculation compares $V_{ref}$ and $V_{link}$. The comparison methods are as shown in Fig. 11.

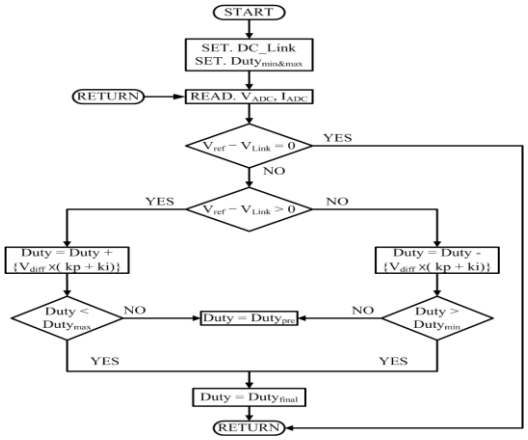


**Fig. 11.** DC link voltage control algorithm flow chart

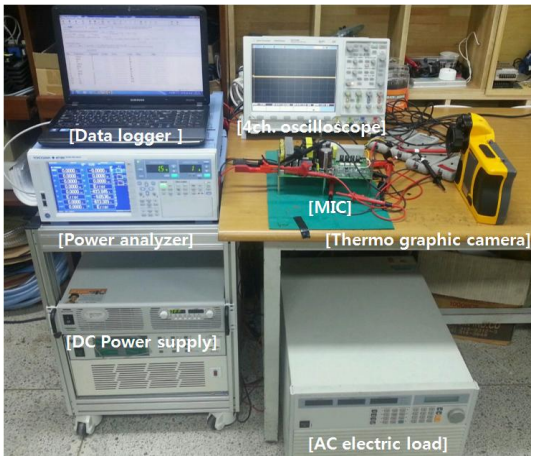


**Fig. 12.** Experimental setup

For the experiment, prototypes were developed that actually produced the simulation parameter values. Fig. 12 shows the experimental setup.

Figure 13 shows the $V_{ds}$ waveform of a conventional flyback converter. As shown, very high voltage spikes are generated. Figure 14 presents the gate signal waveform using the proposed method. *S1* and *S2* are the switch gate signals of the top converter stage and *S3* and *S4* are the switch gate signals of the under converter stage. *S1* and *S3* are controlled by the same duty ratio with a phase difference of 180 °. Additionally, *S2* and *S4* are operated by the ZVS system. Figure 15 shows the $V_{ds}$ waveform from applying the proposed controllable interleaved active clamp switching technique. Figure 16 shows the output waveform of the proposed MIC. The proposed MIC is operated as 200[V], 60[Hz] in working order.

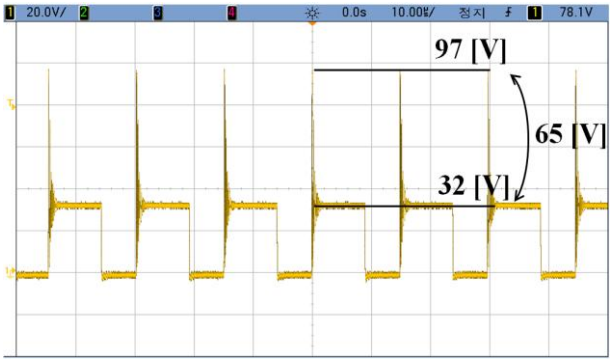


**Fig. 13.** $V_{ds}$ waveform of the conventional flyback converter

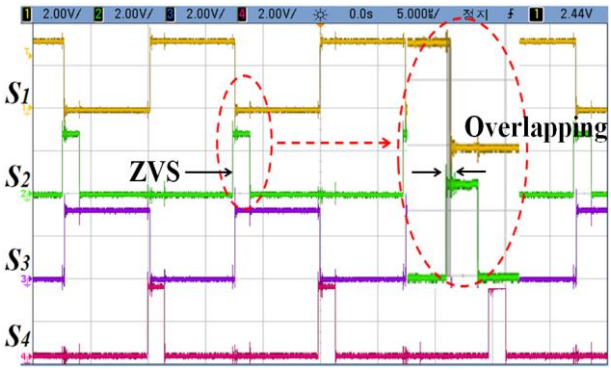


**Fig. 14.** Gate signal waveform using the proposed method

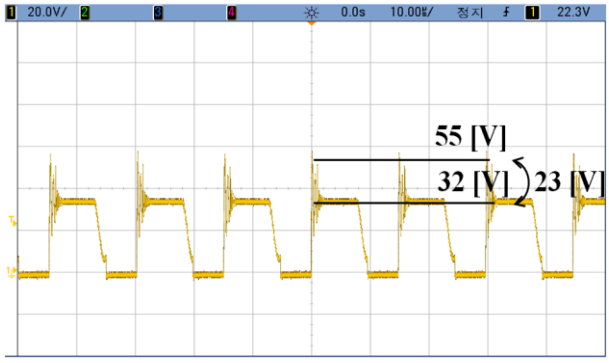


**Fig. 15.** $V_{ds}$ waveform of the proposed active clamp flyback converter

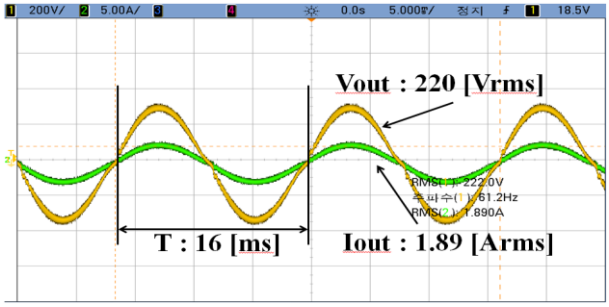


**Fig. 16.** Output waveform of the proposed MIC

Figures 17 and 18 show a temperature test of the MOSFET and transformer using a thermo-graphic camera (Fluke-Ti 55). They compare the temperature of the MOSFET and the transformer before and after applying the controllable interleaved active clamp snubber.

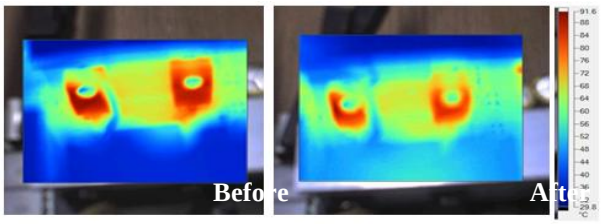

**Fig. 17.** MOSFET temperature measurement

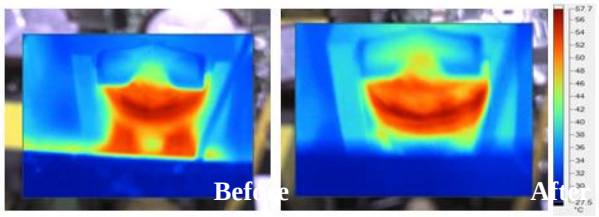

**Fig. 18.** Transformer temperature measurement

The experimental results of the temperature of the MOSFET and the transformer showed reduced temperatures, from 91[℃] to 60[℃] and from 61[℃] to 56[℃].

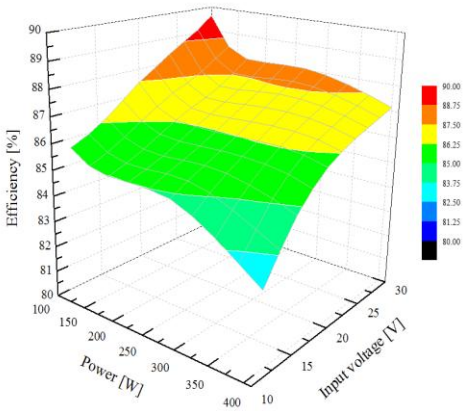


**Fig. 19.** Efficiency surface graph of the proposed MIC

## 4. Conclusions

In this paper, a controllable interleaved active clamp switching method for improving the efficiency of a MIC system is proposed. The suggested method is simple because the voltage spike is removed by charging the clamp capacitor. To confirm the theoretical analysis of the proposed control strategy, a simulation circuit was designed using the PSIM software. Additionally, an actual 400[W] MIC was produced to verify the reliability and validity of this MIC.

The efficiency measurement result showed that the maximum efficiency is ~92[%]. Thus, the proposed method is useful by miniaturizing and reducing the weight for the technical development of a better power conversion device.

## Acknowledgement

This work was partly supported by the Technological innovation R&D program of SMBA [S2089464]] and the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2013R1A1A2010691).

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**Chang-Seok Park** received B.S. and M.S. degree in electrical engineering from Kyungnam University. He is currently a Ph.D. student at Kyungnam University. His research interests are design and motor driver and power conversion

**Tae-Uk Jung** received the B.S., M.S. and Ph.D. degrees in electrical engineering from Pusan National University, Busan, Korea, in 1993, 1995 and 1999, respectively. Between 1996 and 2005, he was a Chief Research Engineer with Laboratory of LG Electronics, Korea. Between 2006 and 2007, he was a Senior Research Engineer of Korea institute of Industrial Technology, Korea. Since 2007, he has been with Kyungnam University as a Professor. His main research topic is concerning about the design and application of small wind turbine PM generator and BLDC motor drive system