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An investigation on dicing 28-nm node Cu/low-k wafer with a Picosecond Pulse Laser

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Abstract: For a nanoscale Cu/low-k wafer, inter-layer dielectric (ILD) and metal layers peelings, cracks, chipping, and delamination are the most common dicing defects by traditional diamond blade saw process. Sidewall void in sawing street is one of the key factors to bring about cracks and chipping. The aim of this research is to evaluate laser grooving & mechanical sawing parameters to eliminate sidewall void and avoid top-side chipping as well as peeling. An ultra-fast pico-second (ps) laser is applied to groove/singulate the 28-nanometer node wafer with Cu/low-k dielectric. A series of comprehensive parametric study on the recipes of input laser power, repetition rate, grooving speed, defocus amount and street index has been conducted to improve the quality of dicing process. The effects of the laser kerf geometry, grooving edge quality and defects are evaluated by using scanning electron microscopy (SEM) and focused ion beam (FIB). Experimental results have shown that the laser grooving technique is capable to improve the quality and yield issues on Cu/low-k wafer dicing process.

Keywords: nanoscale low-k wafer, laser kerf geometry, laser grooving

1. Introduction

As IC scales down into nanometer level, interconnect technologies on back end of the line (BEOL) are forced to move from Al/SiO_2 to Cu/low-k (Copper/low dielectric constant).[1-2] Copper and low-k dielectric layers are implemented as multilevel interconnects to improve the speed of logic devices and reduce cross talk noise, propagation delays and power dissipation from RC delay. Amongst the available low-k materials, black diamond (BD) has been widely used for integration in ULSI (ultra large scale integration) for its better electrical and dielectric properties.[3-4] BD is a trade mark of Applied Materials Inc.[5] and is silica based dielectric material, obtained by doping of silica with -CH3 groups and it has chemical formula SiOC:H. BD thin films are usually fabricated by using the chemical vapor deposition (CVD) method near room temperature. The dielectric constant (k) value of BD films ranges from 2.5 to 2.7, and integrated ILD stack dielectric constant is mostly less than 3. The glass transition temperature of the BD is well above 450°C. The dielectric constant of the BD films can be lowered by introducing porosity into the microstructure in which retains thermo-mechanical properties of silicon oxide. Due to heterogeneous structure of Cu/low-k, interfacial adhesive failure may occur during fabrication processes and delamination or cracking can also be observed during packaging processes. Therefore, micromachining of nanoscale low-k wafer has been one of the crucial issues in IC packaging technology.

Laser technology has been practiced for over four decades and playing an important role in the modern manufacturing industry. Recently, high brightness of fiber/disk lasers and ultra-fast of pico-/femto-second lasers have enabled new developments in micro/nano fabrication that lasers material processing can bring to IC packaging industries. A metallized diamond saw blade has been successfully applied to separate the traditional 300 mm thickness silicon wafer. However, damage to the silicon chips during mechanical dicing has become an extraordinary issue as nanometer node wafers with Cu/low-k dielectrics is implemented.[6-8] Consequently, blade die saw processes confront many serious challenges, such as chipping, die breaking, cracking

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and delamination of the bonded layers due to the diamond-edge mechanical forces. Several new wafer-dicing techniques, such as scribe-and-break, dicing before-grinding and dicing by thinning with dry-etched trenches have been developed to overcome the above-mentioned challenges. Nevertheless, dicing using laser technology is one of the significantly efficient and improving methods.[9-10] Laser technology works as a non-contact tool and offers a mandated micromachining process which is much more competitive than diamond blade saw. Laser process with tight focus results in diminished kerf width and reduces top-/bottom-side chipping and cracking.

Heat energy is concentrated on the laser beamed area to produce debris on the top surface of silicon wafer. Redeposition of melted silicon adheres fast to the top surface of silicon wafer and greatly damages circuits as well as reduces the performance of the IC devices. Up to present, various methods have been developed to accomplish debris-free cutting minimization of debris during wafer dicing. A soluble protective coating on the silicon wafer surface to capture the debris has become an acceptable method in the laser dicing technology. The silicon wafer is dispensed and spin-coated at first, after drying, then laser grooving is performed. A clean debris-free wafer singulation can be achieved after washing. In addition, a smooth kerf internal wall can be obtained if successive chemical wet etching is further applied.[11]

In this paper, grooving on 28-nm node Cu/low-k wafer using 10 ps pulse 512 nm wavelength laser has been conducted to determine the optimized recipes. Material in sawing street (scribe lane) comprises metal (copper), low-k (silica based dielectric materials) and protectively coated silicon. A series of experimental works has been conducted and the results can be directly applied to industrial wafer sawing process.

2. Experimental Works

The micro structure of nanoscale Cu/low-k silicon wafer used in this work includes 5 μm low-k (black diamond) ·500Å TEOS (tetraethyl orthosilicate)·250Å Ta (Tantalum)·1000Å Cu (Copper) seed·2 μm electroplating-Cu, which is shown in Figure 1.[12] The complete wafer sawing process comprises: laser groove and diamond blade saw. Traditional diamond blade saw process on Cu/low-k wafer (heterogeneous materials) will lead to top-/bottom-side chipping, peeling or sidewall overcutting. The void in sidewall is one of the factors to cause sidewall cracks. Therefore, laser grooving technology is introduced to nanoscale wafer dicing to

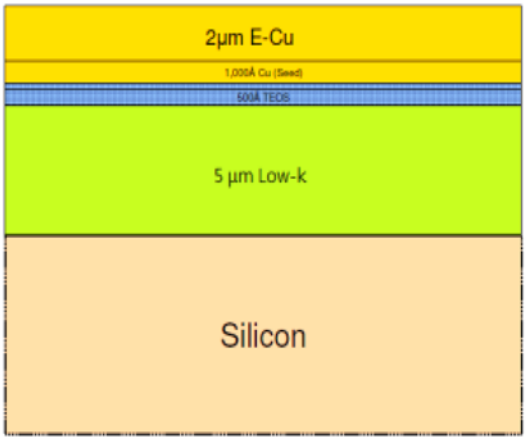

Fig. 1. Cu/low-k wafer micro structure.

Table 1. Specification of Laser machine used in this study.

Wavelength of laser light	512 nm
Maximum average power	30 W
Diffraction factor M^2	<1, 3
Pulse duration	< 10 ps
Base frequency	200, 400, 600, 800 KHz
Maximum pulse energy	150 μJ
Beam diameter at the exit window	5 mm

eliminate sidewall voids and improve the quality of sawing process. Water soluble coating is applied to the surface of the silicon wafer to seize the recast silicon remaining (debris). The thickness of this protective coating film is about 1 um.

The specification of ultra-fast laser machine used in this works is listed in Table 1. Parametric studies are performed based on (1) 3-pass laser grooving (2) DOE (design of experiments) using Taguchi approach (3) sidewall voids elimination in 5-pass. Parameters for standard 3-pass laser grooving, Taguchi orthogonal array and 5-pass sidewall void elimination are listed in Table 2, Table 3 and Table4, respectively.

3. Results and Discussion

Preliminary results demonstrate that parameter of power would directly affect the depth of cut, frequency results in depth of cut/surface debris, defocus relates to beam size, speed influences on surface ripple/surface debris, and index induces the overlap rate. Because the width of sawing street ranges from 65 to 70 μm, the experimental kerf width should be controlled at 45-55 μm and kerf depth is up to 35 μm. For the standard 3-pass laser grooving process, the effects of the laser kerf geometry, grooving edge quality and

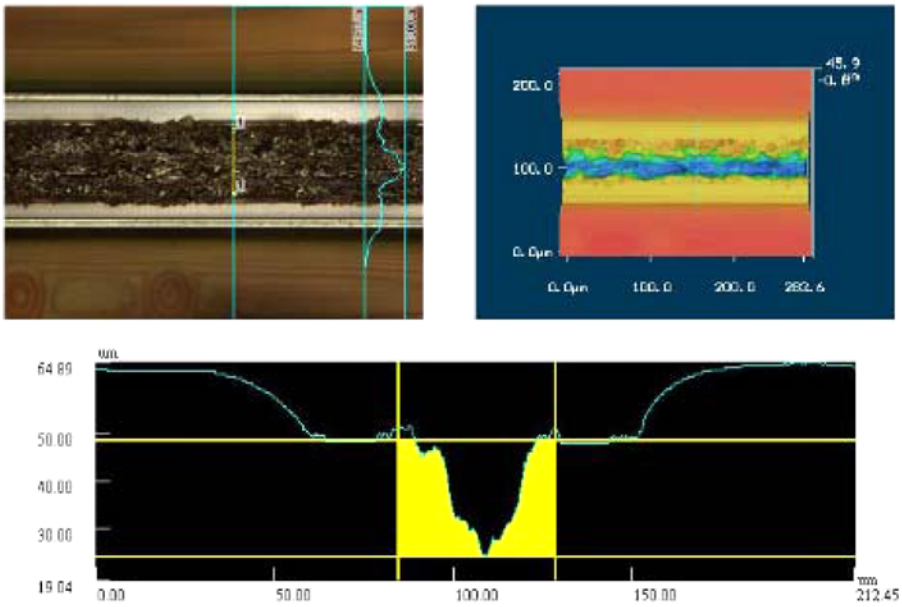

Fig. 2. Kerf geometry for 3-pass laser grooving scanned by Keyence 3D laser scanning microscopes (V-shape cut under scribe lane).

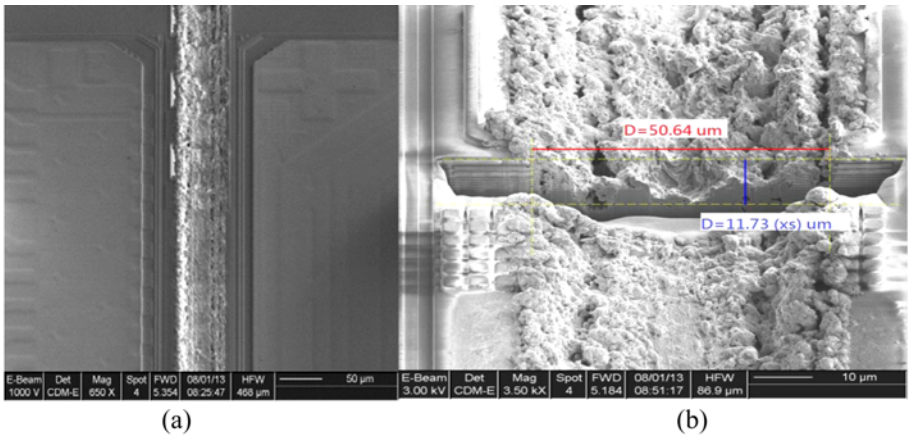

Fig. 3. (a) Top viewed by e-beam (b) Enlarged view of kerf width/kerf depth.

defects are evaluated by 3D laser scanning microscopes and scanning electron microscopy (SEM). Figure 2 illustrates kerf geometry for 3-pass laser grooving standard recipes. The kerf depth can be controlled under 56 μm and the V-shape cut is generated under the sawing street. Figure 3(a) presents the debris on top opening and Figure 3(b) demonstrates the corresponding enlarged view of e-beam photo.

In general, DOE using Taguchi approach can economically satisfy the needs of process design optimization projects. In order to eliminate the top-/bottom side chipping and minimize the debris from heat generation Taguchi method is conducted to evaluate the optimization recipe for laser grooving. DOE parameters matrix is defined in Table 3(a) and Taguchi orthogonal array is listed in Table 3(b). The optimized recipe is found to be A1B3C3D3, i.e. 4 MHz, 15W, 600 mm/s, overlap 100% and the results is determined in Table 4. It should be noted that all experimental data obtained in this work meet the industrial requirements.

Table 2. Recipes for standard 3-pass laser grooving process.

	Pass 1	Pass 2	Pass 3
Power (W)	2.8	3	2
Repetition-Rate (Hz)	160	50	40
Speed (mm/s)	300	120	300
Defocus (mm)	0	0	0
Index (mm)	47	0	0

The main advantage of using laser beam cutting is to reduce top-/bottom-side chipping and cracking. Nevertheless, most of the drawbacks of laser dicing are associated with the heat generation during laser ablation. In order to produce good quality of die sawing process, many issues need to be

Table 3. (a) DOE parameters matrix.

Factor	Level 1	Level 2	Level 3
A (Repetition Rate)	4MHz	6MHz	8MHz
B (Power)	5W	10W	15W
C (Speed)	150 mm/s	300mm/s	600 mm/s
D (Pass & overlap rate)	3-pass (overlap 20%)	3-pass (overlap 50%)	3-pass (overlap 100%)

Table 3. (b) Taguchi orthogonal array.

No.	A	B	C	D
1	L1	L1	L1	L1
2	L1	L2	L2	L2
3	L1	L3	L3	L3
4	L2	L1	L2	L3
5	L2	L2	L3	L1
6	L2	L3	L1	L2
7	L3	L1	L3	L2
8	L3	L2	L1	L3
9	L3	L3	L2	L1

Table 4. Laser grooving results after Taguchi optimized recipes.

Item	Specification	Industry Standard	Experimental work
1	Heat affect analysis (Debris)	< 5 μm	3.57 μm
2	Top side chipping	Not allow	< 0.005 μm
3	Passivation peeling	Not allow	< 0.005 μm
4	Laser groove depth	>10 μm	15.786 μm
5	Wafer scratch	Not allow	<0.005 μm
6	Die crack	Not allow	<0.005 μm
7	Wafer broken	Not allow	None
8	Laser total kerf width	Target ± 3 μm	± 2.73 μm
9	Laser kerf shift	± 2 μm	± 1.96 μm

fully understood. This includes the selection of appropriate processing parameters, analysis of metallurgical effects of the cutting process, minimization of micro-cracks, heat affected zone, debris around the redeposit surface. Hence, an increasing in the number of passes with appropriate processing recipe would be another interesting solution for industrial process. 5-pass laser beam dicing technique then becomes alternative major fabrication process. However, the sidewall voids are sometimes produced during the third pass (pass 3) or the fourth pass (pass 4). Sidewall voids are known to be responsible for top side cracking.

Figure 4(a) schematically illustrates recipes for 5-pass laser grooving process and Figure 4(b) presents the defect of sidewall voids after sawing. The original and optimized recipes for 5-pass laser grooving are listed in Table 5(a) and 5(b), respectively. The differences between original and optimized recipes are defocus amount and controlled kerf width. Figure 5 demonstrates kerf geometry scanned by Keyence 3D microscopes for optimized recipes applied to 5-pass laser grooving process. Please be noted that U-shape cut under scribe lane can be achieved by using special-

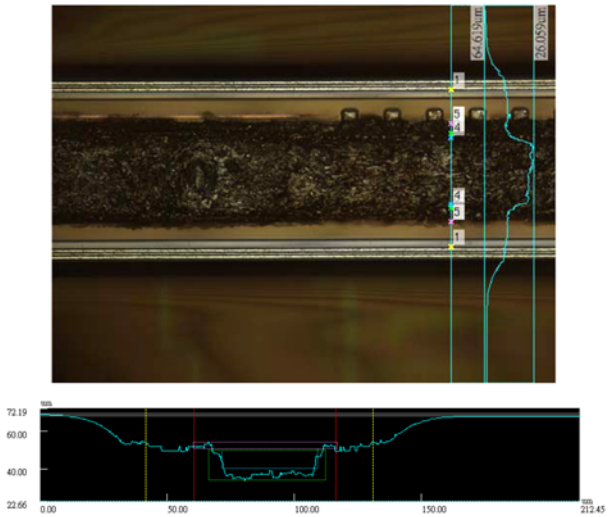

Fig. 5. Kerf geometry for optimized 5-pass laser grooving by Keyence 3D microscopes (U-shape cut under scribe lane).

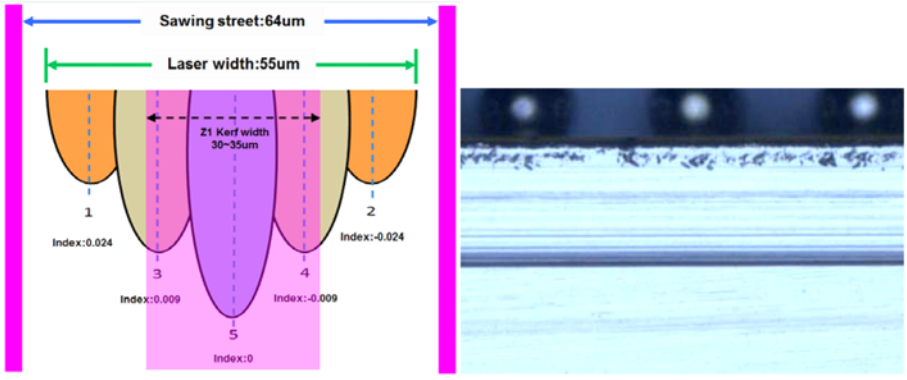

Fig. 4. (a) Schematically illustrated recipes of 5-pass Laser grooving (b) Sidewall voids generated at 3-/4-pass.

Table 5. (a) Original recipes for 5-pass laser grooving.

No	Pass	Power (W)	Repetition Rate (Hz)	Speed (mm/s)	Defocus (mm)	Index (mm)
A1	1	1.4	200	450	0	0.024
A2	2	1.4	200	450	0	-0.024
A3	3	3.5	60	200	0.14	0.009
A4	4	3.5	60	200	0.14	-0.009
A5	5	4.5	40	200	0.2	0

Table 5. (b) Optimized recipes for 5-pass laser grooving.

No	Pass	Power (W)	Repetition Rate (HZ)	Speed (mm/s)	Defocus (mm)	Index (mm)
B1	1	1.4	200	450	0	0.02
B2	2	1.4	200	450	0	-0.02
B3	3	3.5	60	200	0.14	0.005
B4	4	3.5	60	200	0.14	-0.005
B5	5	4.5	40	200	0.2	0

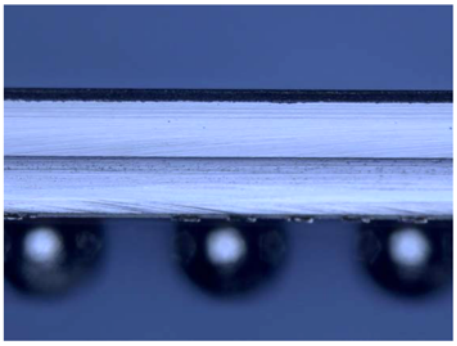

Fig. 6. No sidewall void/no top cracking exists for optimized 5-pass laser grooving.

designed photo mask.

Moreover, Figure 6 shows that sidewall voids has been eliminated as the laser width is constrained from 55 μm to 47 μm, i.e. kerf width for pass 1-2, pass 3-4 and pass 5 has been changed from 55, 36, 22 μm to 47, 28, 22 μm in Figure 4(a). The results also can be found in Table 6(a) and 6(b) for original and optimized recipes, respectively.

Table 6. (a) Kerf geometry for original 5-pass laser grooving.

	Results					
	Ave.	A1	A2	A3	A4	A5
Kerf Width(μm)	58	57	58	58	57	59
Kerf Depth(μm)	20	20	21	20	20	21

Table 6. (b) Kerf geometry for optimized 5-pass laser grooving.

	Results					
	Ave.	B1	B2	B3	B4	B5
Kerf Width(μm)	46	47	48	46	45	47
Kerf Depth(μm)	21	20	21	20	20	21

4. Conclusions

This paper demonstrates an improvement procedure for laser grooving/dicing on a nanoscale low-k wafer to eliminate the sidewall voids and top cracking. Microstructure of nanoscale wafer with Cu/low-k dielectric is presented. Due to heterogeneous materials in Cu/low-k wafer, an ultra-fast pico-second 515 nm green laser is applied to micro machine a 28 nanometer node wafer. DOE using Taguchi method has been conducted and successfully determined the standard 3-pass laser beam void-free recipes. Furthermore, parameters used to eliminate sidewall voids in 5-pass laser grooving technique are obtained. U-shape cut under sawing street has been accomplished by using a self-designed mask. All experimental data in this work satisfy the industrial requirements.

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References

1. D. Shamiryan, T. Abell, F. Lacopi and K. Maex, “Low-k dielectric materials”, Materials Today, 7(1), 34 (2004).
2. H. H. Jiun, I. Ahmada, A. Jalarb and G. Omarc, “Effect of wafer thinning methods towards fracture strength and topography of silicon die”, Microelectronics Reliability, 46, 836 (2006).
3. S. Chen, T. Y. Kuo, H. T. Hu, J. R. Lin and S. P. Yu, “The evaluation of wafer thinning and singulating processes to enhance chip”, Proc. 55th Electronic Components and Technology Conference (ECTC), 1526, IEEE (2005).
4. V. N. Sekhar, “Mechanical characterization of black diamond (low-k) structures for 3D integrated circuit and packaging applications”, Nanoindentation in Materials Science, 10, 229 (2012).
5. http://www.appliedmaterials.com.
6. J. Sillanpaa, J. Kangastupa, A. Salokatve and H. Asonen, “Ultra-short pulse Laser meeting the requirements for high speed and high quality dicing of low-k wafers”, Proc. Advanced Semiconductor Manufacturing Conference and Workshop (ASMC), Munich, 194, IEEE (2005).
7. J. V. Borkulo, P. Dijkstra and R. Hendriks, “Comparison between Single & Multi Beam Laser Grooving of Low-K layers”, Proc. 45th International Symposium on Microelectronics (IMAPS), 433 (2012).
8. C. Paydenkar, A. Poddar, H. Chandra and S. Harada, “Wafer sawing process characterization for thin Die (75micron) applications”, Proc. 29th International Electronics Manufacturing Technology Symposium (IEEE/CPMT/SEMI), 74, IEEE (2004).

9. K. Shimizu, K. Takahashi, H. Morikazu, N. Ogoshi, K. Takeyama, Y. Wakayama and T. Obara, “Laser ablation of silicon wafer with a water microdrop”, J. Laser Applications, 18(2), 127 (2006).
10. L. T. Beng, C. L. W. Yew, K. W. Shi, S. C. Teck and K.Y. Yow, “Laser Grooving Process Development for Low-k Ultra Low-k Devices”, Proc. 33rd International Electronic Manufacturing Technology Symposium (IEMT), Penang, 1, IEEE/CPMT (2008).
11. H. Y. Zheng, X. C. Wang and Z. K. Wang, “Laser dicing of silicon and electronics substrates”, Advances in Laser Materials Processing: Technology, Research and Application, 88 (2010).
12. H. C. Hsu and S. J. Wu, “Laser Drilling and Thermal Stress Analysis on TSV in 3D IC Structure”, Proc. International Conference on Electron Devices and Solid-State Circuits, 112, IEEE (2014).