Small-Signal Analysis of a Differential Two-Stage Folded-Cascode CMOS Op Amp

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Abstract—**Using a simplified high-frequency small-signal equivalent circuit model for BSIM3 MOSFET, the fully differential two-stage folded-cascode CMOS operational amplifier is analyzed to obtain its small-signal voltage transfer function. As a result, the expressions for dc gain, five zero frequencies, five pole frequencies, unity-gain frequency, and phase margin are derived for op amp design using design equations. Then the analysis result is verified through the comparison with Spice simulations of both a high speed op amp and a low power op amp designed for the 0.13 μm CMOS process.**

Index Terms—**Differential two-stage folded-cascode CMOS op amp, equation-based circuit design, high speed, low power, pole and zero frequency, small-signal transfer function, frequency response, BSIM3.**

I. INTRODUCTION

Operational amplifiers have been used in a variety of analog circuits such as instrumentation amplifiers, continuous-time or switched-capacitor filters, analog-to-digital or digital-to-analog converters, voltage regulators, and waveform generators. As a result, these op amps are essential analog circuit cells in many mixed-signal integrated circuits. In particular, the differential two-stage folded-cascode op amp is needed to obtain high dc gain and wide output swing at low supply voltage in deep submicron technology [1]. For example, this op amp is used in high speed pipeline analog-to-digital converters and high frequency switched-capacitor filters [2-4]. Design of such high speed and high frequency complementary metal-oxide-semiconductor (CMOS) op amps becomes more critical in low power and low voltage circuits. In addition, transistor models have become more complex to characterize the physical behavior of submicron devices at high frequencies [5, 6]. Thus analog circuit design consumes a significant portion of total design time for mixed-signal integrated circuits. So this is called analog design bottleneck. In order to enhance design productivity, various computer-aided design (CAD) approaches have been presented for op amp design or analog circuit design [7-14].

The small-signal design equations for dc gain, pole and zero frequencies, unity-gain frequency, and phase margin of op amps are required in manual design as well as equation-based and mixed CAD. So the pole and zero frequencies can be designed to achieve the stable transient response of operational amplifiers. Moreover, pole-zero doublets in the passband should be controlled through the design equations. Otherwise these doublets may seriously deteriorate the settling time. Such pole-zero control is an important advantage of equation-based design compared to simulation-based design. Thus it will be desirable that design equations of all op amps should be available. But in spite of the fact that the differential two-stage folded-cascode CMOS op amp is used in various analog circuits, its small signal design equations have *not* yet been derived analytically. In this paper, the transfer function of such an op amp will be analyzed to obtain its small-signal design equations. Then the analysis result will be verified through the comparison with Spice simulations of both a designed high speed

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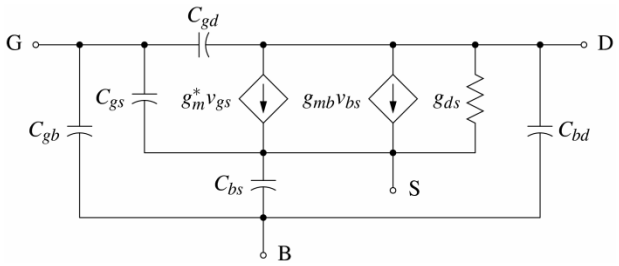

Fig. 1. An MOSFET high-frequency small-signal equivalent circuit model with the complex transconductance g_m^*.

CMOS op amp with a unity-gain frequency of 576 MHz and a designed very low power CMOS op amp with a quiescent power dissipation of 2.5 μW.

II. MOSFET SMALL-SIGNAL MODEL

Spice solves directly for small-signal voltages and currents using the large-signal equations of BSIM3. As a result, BSIM3 guarantees that the results from ac and transient simulation are entirely consistent because the two simulations use the same set of governing transistor equations. Naturally, there is no BSIM3 small-signal equivalent circuit model generated independently from the large-signal equations. But a small-signal circuit model of MOSFETs is needed to obtain the frequency responses of CMOS op amps for their design. A simplified high-frequency small-signal model shown in Fig. 1 has been derived from the large-signal model used by BSIM3 [6]. It will be used in the small-signal analysis of the two-stage folded-cascode op amp circuit.

In this model, the complex transconductance or transadmittance is defined by $g_m^* = g_m - sC_m$ where the transcapacitance C_m is given by $(C_{dg} - C_{gd})$. Also C_{dg} is defined by $-\partial q_d / \partial v_g$ which represents the effect of the gate voltage v_g on the charge q_d associated with drain. On the other hand, C_{gd} is defined by $-\partial q_g / \partial v_d$ which represents the effect of the drain voltage v_d on the gate charge q_g. If the drain and gate are the two terminals of a parallel-plate capacitor, C_{dg} and C_{gd} would have been equal like in the Meyer model. In general, these two transcapacitances are not the same. For example, consider a long-channel transistor in saturation. Because of pinchoff at the drain end, the drain voltage will not affect the gate charge. Thus C_{gd} will be zero. However, the gate voltage will greatly affect the inversion charge associated with the drain charge q_d. Thus C_{dg} will have a large value. As a result, C_{dg} is always greater or equal to C_{gd} under all operating regions, and then C_m will be greatest in the saturation region [5, 6].

Table 1. Typical parameter values of an *n*MOS transistor with width 9 μm and length 0.49 μm for the 0.13 μm CMOS process

Parameter	Strong	Moderate	Parameter	Strong	Moderate
g_m	745μS	13.8μS	g_{mb}	92.6μS	2.1μS
C_m	14.7 fF	1.5 fF	g_{ds}	18.4μS	0.4μS
C_{gs}	40.5 fF	8.5 fF	C_{gd}	5.0 fF	4.6 fF
C_{gb}	2.1 fF	7.2 fF	C_{dg}	19.7 fF	6.1 fF
C_{bs}	10.5 fF	12.3 fF	C_{bd}	9.2 fF	10.1 fF

Finally, the capacitances of five physical capacitors shown in the small-signal model should include extrinsic capacitances like overlap or junction capacitances. In the small-signal analysis, each capacitor is treated as an ordinary circuit element with the given capacitance. Usually Spice reports these total capacitances at a bias point in the operating point printout. For the IBM 0.13 μm CMOS process, typical small-signal parameters of an *n*MOS transistor operating in the strong or moderate inversion region are given in Table 1.

III. SMALL-SIGNAL ANALYSIS

In this section, we analyze and verify the small-signal operation of a fully differential two-stage folded-cascode CMOS op amp to determine its voltage gain in response to the input voltage. Fig. 2 shows this operational amplifier fed by a differential input signal V_i that is applied in a complementary or balanced manner [1-4]. That is, the gate of M_1 is increased by $V_{i+} = +V_i / 2$ and the gate of M_2 is decreased by $V_{i-} = -V_i / 2$. To enhance gain with body effect, the body terminals of M_6 and M_7 are connected to the power supply V_{DD}, whereas those terminals of M_8 and M_9 to the power supply $-V_{SS}$. Because of the circuit symmetry and balanced driving, a signal ground as a sort of virtual

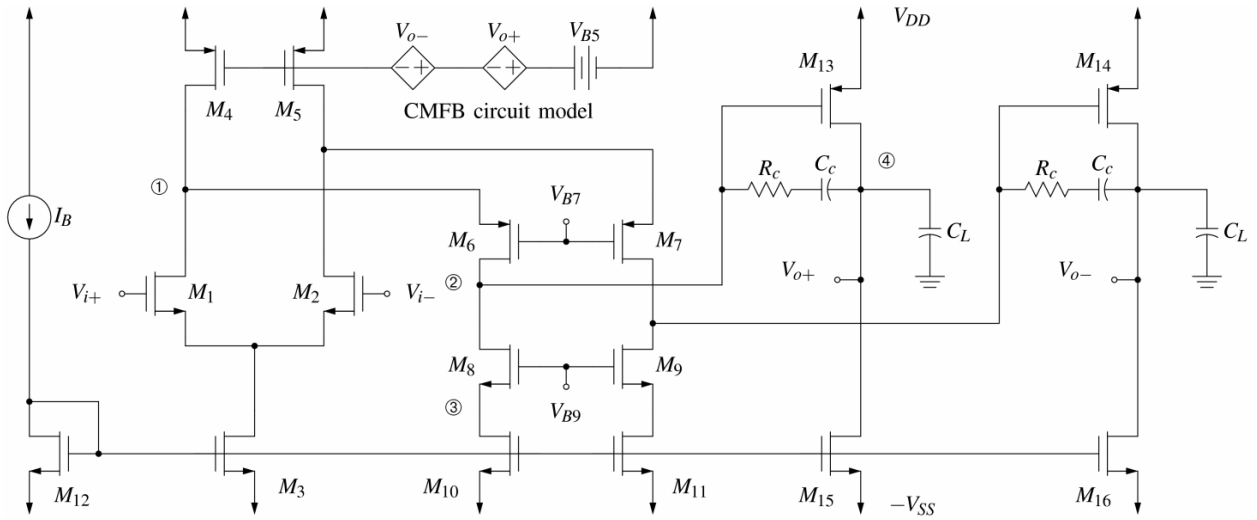

Fig. 2. A fully differential two-stage folded-cascode CMOS op amp with common-mode feedback circuit model and node numbers.

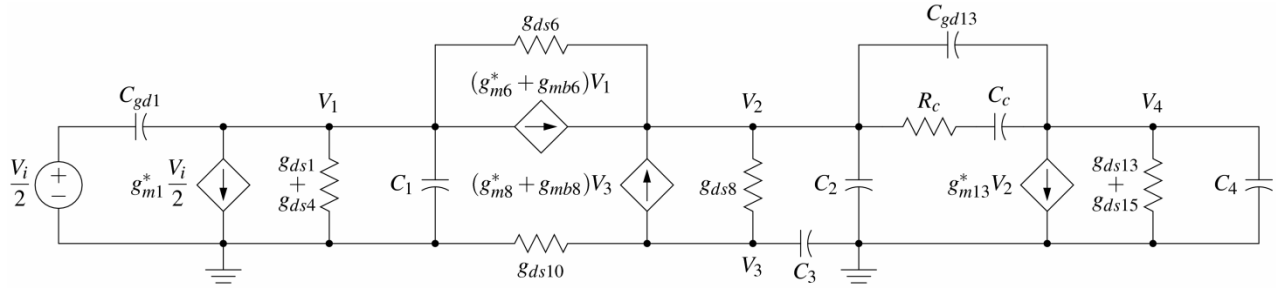

Fig. 3. A high frequency equivalent circuit for the differential half circuit of the two-stage folded-cascode CMOS op amp.

$$\begin{bmatrix} g_{11}+sC_{11} & -g_{ds6} & 0 & 0 \\ -g_{21}+sC_{m6} & g_{22}+s(C_2+C_{24}) & -g_{23}+sC_{m8} & -sC_{24} \\ 0 & -g_{ds8} & g_{33}+s(C_3-C_{m8}) & 0 \\ 0 & g_{m13}-s(C_{m13}+C_{24}) & 0 & g_{44}+s(C_4+C_{24}) \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = -\frac{V_i}{2} \begin{bmatrix} g_{m1}-s(C_{gd1}+C_{m1}) \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{1}$$

$$N(s)=\left(g_{m1}-sC_{dg1}\right)\left(g_{21}-sC_{m6}\right)\left[g_{33}+s\left(C_3-C_{m8}\right)\right]\left\{g_{m13}+s\left[C_c\left(g_{m13}R_c-1\right)-C_{dg13}\right]-s^2C_{dg13}R_cC_c\right\} \tag{2}$$

ground is established at the source terminals of the input differential pair. As a result, the output conductance of the current source M_3 will have no effect on the small signal operation. Thus a differential half circuit of the op amp can be obtained by excluding M_3 for differential signal operation. Fig. 3 shows the equivalent half circuit. Here V_n is the voltage of node *n* and the differential input voltage is given by $V_i \equiv (V_{i+}-V_{i-})$. In addition, the capacitances C_1, C_2, C_3, and C_4 represent the total node capacitances at the drains of M_1, M_6, M_{10}, and M_{13} respectively. From this half circuit, the differential voltage gain of the op amp can be determined directly [15, 16]. The nodal equations for this circuit can be written in a matrix form as (1). The conductances g_{jk} and capacitances C_{jk} used in this equation are defined in Table 2 using the transconductance g_{mi}, body transconductance g_{mbi}, output conductance g_{dsi}, transcapacitance C_{mi}, parasitic capacitances C_{gbi}, C_{gsi}, C_{gdi}, C_{bsi}, and C_{bdi} of each transistor M_i, and the load capacitance C_L at each output node. In order to reduce the number of nodal equations, sC_{24} has been used as an equivalent admittance between node 2 and node 4.

Table 2. Definition of each conductance and capacitance used in the Eq. (1) for the equivalent small-signal half circuit

$$g_{11} \equiv g_{ds1} + g_{ds4} + g_{21}, \quad g_{22} \equiv g_{ds6} + g_{ds8}$$
$$g_{21} \equiv g_{m6} + g_{mb6} + g_{ds6}, \quad g_{23} \equiv g_{m8} + g_{mb8} + g_{ds8}$$
$$g_{33} \equiv g_{ds10} + g_{23}, \quad g_{44} \equiv g_{ds13} + g_{ds15}$$
$$C_{11} \equiv C_1 + C_{gd1} - C_{m6}, \quad C_{24} \equiv C_{gd13} + C_c / (1 + sR_cC_c)$$
$$C_1 = C_{gs6} + C_{bs6} + C_{bd1} + C_{bd4} + C_{gd4}$$
$$C_2 = C_{bd6} + C_{gd6} + C_{bd8} + C_{gd8} + C_{gs13} + C_{gb13}$$
$$C_3 = C_{gs8} + C_{bs8} + C_{gd10} + C_{bd10}$$
$$C_4 = C_L + C_{bd13} + C_{gd15} + C_{bd15}$$

Using the output voltage V_4 of the equivalent half circuit, the differential output voltage of the op amp can be expressed as $V_o \equiv V_{o+} - V_{o-} = 2V_4$. Therefore, the differential voltage gain $A_d \equiv V_o / V_i$ can be written as a rational fraction

$$A_d(s) \equiv \frac{N(s)}{D(s)} = A_0 \frac{\prod_{i=1}^{5}(1 + s/\omega_{zi})}{\prod_{i=1}^{5}(1 + s/\omega_{pi})} \tag{3}$$

where A_0 is the dc gain, ω_{zi} is the frequency of zero z_i, and ω_{pi} is the frequency of pole p_i. From symbolic analysis for the circuit Eq. (1), the numerator can be exactly obtained as a factored form like (2). Assuming that $(1 + b_1 s + b_2 s^2) \simeq (1 + b_1 s)(1 + b_2 s / b_1)$ and $C_c(g_{m13}R_c - 1) \gg C_{dg13}$, the numerator polynomial can be approximately factored as

$$N(s) \simeq g_{m1}g_{21}g_{m13}g_{33} \left(1 - \frac{sC_{dg1}}{g_{m1}}\right)\left(1 - \frac{sC_{m6}}{g_{21}}\right)\left[1 + \frac{s(C_3 - C_{m8})}{g_{33}}\right] \left[1 - \frac{sR_cC_{dg13}}{(g_{m13}R_c - 1)}\right]\left[1 + \frac{sC_c(g_{m13}R_c - 1)}{g_{m13}}\right] \tag{4}$$

The denominator of the differential voltage gain A_d consists of 226 terms and is given by a fifth-order polynomial

$$D(s) = a_0 + a_1 s + a_2 s^2 + a_3 s^3 + a_4 s^4 + a_5 s^5 \tag{5}$$

where the coefficient a_0 can be arranged as

$$a_0 = g_{44}\left[g_{11}g_{ds8}g_{ds10} + g_{33}g_{ds6}(g_{ds1} + g_{ds4})\right] \tag{6}$$

As a result, the dc gain $A_0 \equiv A_d(0)$ can be found as

$$A_0 = \frac{g_{m1}g_{21}g_{m13}g_{33}}{a_0} = \frac{g_{m1}g_{21}g_{m13}}{g_{o1}g_{11}g_{44}} \tag{7}$$

where output conductance of the first stage is given by

$$g_{o1} = \frac{g_{ds8}g_{ds10}}{g_{33}} + \frac{g_{ds6}(g_{ds1} + g_{ds4})}{g_{11}} \tag{8}$$

In general, the coefficient a_1 is related to the open-circuit time constants and the frequencies of poles as follows [17].

$$\frac{a_1}{a_0} \equiv \frac{a_{11} + a_{12} + \cdots + a_{15}}{a_0} = \sum_{i=1}^{5} R_{io}C_i = \sum_{i=1}^{5} \frac{1}{\omega_{pi}} \tag{9}$$

Typically op amps are designed so as to have a dominant pole p_1. Hence its frequency ω_{p1} is much smaller than all other pole frequencies. In the two-stage op amp, this pole is realized by a large compensation capacitance C_c. As a result, the dominant pole will be related to open-circuit time constants (a_{11} / a_0) associated with C_c. The terms a_{11} usually consist of the largest term with C_c and additional terms. Among 25 terms of a_1, the candidates for these terms a_{11} can be arranged as

$$(1 + g_{44}R_c)\left[g_{11}g_{ds8}g_{ds10} + g_{33}(g_{ds1} + g_{ds4})g_{ds6}\right]C_c + g_{11}g_{33}(g_{m13} + g_{44})(C_c + C_{gd13}) \tag{10}$$

where the largest term is $(g_{11}g_{33}g_{m13}C_c)$. The other additional terms for the dominant pole can be found from the terms of (10) by insight for circuit and process of trial and error. As a result, the final major terms a_{11} are found as

$$a_{11} \simeq g_{11}g_{33}(g_{m13} + g_{44})(C_c + C_{gd13}) \tag{11}$$

Thus the dominant pole frequency is approximated as

$$a_5 = C_c C_{11}(C_3 - C_{m8})\left[C_4(C_2 + C_{gd13}) + C_{gd13}(C_2 - C_{m13})\right]R_c \simeq C_c C_{11}\left(C_3 - C_{m8}\right)\left(C_4 + C_{gd13}\right)C_2 R_c \tag{13}$$

$$\omega_{p1} = \frac{a_0}{a_{11}} \simeq \frac{g_{o1}g_{44}}{(g_{m13} + g_{44})(C_c + C_{gd13})} \tag{12}$$

For a two-stage folded-cascode op amp designed for the IBM 0.13 μm CMOS process, the comparison between a transfer function with the dominant pole and Spice simulation is shown in Fig. 4. It can be seen that (12) is an accurate model of the dominant pole and that the nondominant poles are needed to reduce the phase difference at the unity-gain frequency f_t. Because the phase margin is a critical performance in reducing power dissipation, accurate estimation of the phase at f_t is quite important in low power op amp design.

The nondominant poles can be found by factoring the coefficient a_5 with 8 terms that are obtained from the symbolic analysis of (1). Assuming that C_2 is sufficiently greater than C_{gd13} and C_{m13}, the factored form of a_5 can be obtained as (13). Here the factors $(C_4 + C_{gd13})C_2$ have been approximated from the factor $\left[C_4(C_2 + C_{gd13}) + C_{gd13}(C_2 - C_{m13})\right]$. If we compare coefficients between the denominator of (3) and (5), it follows that $\prod_{i=1}^{5}\omega_{pi} = (a_0 / a_5)$. Thus the product of all nondominant pole frequencies can be written as

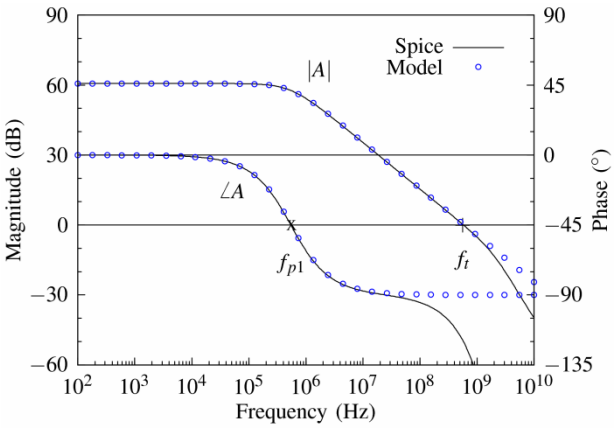

Fig. 4. Comparison between a dominant-pole transfer function model $A = A_0 / (1 + s/\omega_{p1})$ and Spice simulation for a high speed CMOS op amp with a unity-gain frequency of 576 MHz.

$$\omega_{p2}\omega_{p3}\omega_{p4}\omega_{p5} = \frac{a_0}{\omega_{p1}a_5} = \frac{a_{11}}{a_5} \simeq \frac{g_{11}g_{33}(g_{m13} + g_{44})(C_c + C_{gd13})}{C_c C_{11}(C_3 - C_{m8})(C_4 + C_{gd13})C_2 R_c} \tag{14}$$

When C_2 is not sufficiently greater than C_{gd13} and C_{m13}, the above approximation makes slight differences between model and simulation in high frequency region. But such differences can be reduced by using factors $(C_4 + C_{gd13})(C_2 + C_{gd13})$. Therefore, the denominator polynomial of the voltage gain can be expressed as

$$D \simeq a_0\left(1 + \frac{s}{\omega_{p1}}\right)\left[1 + \frac{s(C_4 + C_{gd13})}{(g_{m13} + g_{44})(1 + C_{gd13}/C_c)}\right]\left(1 + \frac{sC_{11}}{g_{11}}\right)(1 + sR_c C_2)\left[1 + \frac{s(C_3 - C_{m8})}{g_{33}}\right] \tag{15}$$

where the last factor is exactly equal to the third factor of the numerator. These factors may give rise to a pole-zero doublet. If this doublet is in the passband, it may cause severe degradation of settling time while only causing minor changes in the frequency response [18]. Besides, the doublet near the unity-gain frequency ω_t may give rise to errors in estimating ω_t and the phase margin. To enhance stability and accuracy, it is desirable to impose a design constraint $\omega_{p5} > \omega_t$.

The unity-gain frequency of the two-stage folded-cascode op amp is an implicit nonposynomial [19]. Using $\left|A_d(j\omega_t)\right| \equiv 1$ and $\omega_t / \omega_{p1} \gg 1$, the unity-gain frequency can be modeled as

$$\omega_t = A_0\omega_{p1}H(\omega_t) \equiv k_t\frac{g_{m1}}{C_c} \tag{16}$$

$$H(\omega_t) \equiv \sqrt{\frac{\prod_{i=1}^{5}\left[1 + (\omega_t/\omega_{zi})^2\right]}{\prod_{i=2}^{5}\left[1 + (\omega_t/\omega_{pi})^2\right]}} \tag{17}$$

where k_t is a modeling parameter. Since this design equation is nonlinear and nonposynomial for ω_t, it

should be solved or designed iteratively. In Fig. 4, f_t was found by iteration. In such an iterative design process, k_t can be considered as an updating parameter. The phase margin of the op amp is also a complicate nonposynomial. Using $\arctan(x) \simeq x$ for $x < 0.5$, the phase margin PM can be approximately obtained from

$$\frac{\mathrm{PM} - 90^\circ}{180^\circ} \simeq \frac{\omega_t}{\pi}\left[\sum_{i=1}^{5}\frac{1}{\omega_{zi}} - \sum_{i=2}^{5}\frac{1}{\omega_{pi}}\right] \tag{18}$$

Here it can be seen that a right-half-plane (RHP) zero with negative frequency ω_{zi} gives rise to decrease in PM like a left-half-plane pole with positive frequency. Small PM leads to excessive gain peaking in the closed-loop frequency response and undesirable ringing in the step response. As a result, the RHP zero will cause degradation of op amp stability. On the contrary, a left-half-plane zero increases the phase margin.

IV. Design and Verification

In this section, the transfer function will be compared with Spice simulations of the two op amps designed by sequential geometric programming. Table 3 shows the design specifications of op amp 1 and 2. To enlarge the performance difference between two op amps, the op amp 1 was designed as a high speed op amp while the op amp 2 was designed as a low power op amp. In general, because op amp design is a nonlinear optimization problem, we have to solve it using an iterative approach. This is naturally compatible with updating parameters. Typically the design equations consist of the transistor parameters. Thus the nonposynomial parameters and equations are updated through modeling parameters from operating point simulation [11]. In this respect, the used design paradigm can be called a mixed approach utilizing both bias simulations and design equations. Finally, it takes 46 and 17 iterations to design the op amp 1 and op amp 2 respectively.

The basic specifications for op amp design are the constraints on dc gain, unity-gain frequency, and phase margin. In addition to these signal constraints, bias constraints should be imposed to ensure that all transistors remain in saturation for the input common-mode voltage v_{CM} and output voltage v_O. These

Table 3. Design constraints and objective of the two-stage folded-cascode CMOS op amp 1 and 2 for the 0.13 μm process

Performance	Specification for op amp 1	Specification for op amp 2
A_0 (dB)	≥ 60	≥ 70
f_t (MHz)	≥ 570	≥ 4.8
PM (°)	≥ 60	≥ 60
CMR (V)	0.1 / 0.7	0.1 / 0.7
OS (V)	–0.3 / 0.3	–0.3 / 0.3
SR (V/ μs)	≥ 500	≥ 1
P_D (mW)	≤ 0.85	$\le 2.5\times10^{-3}$
Area (μm^2)	minimize	minimize
Power supply $= \pm 0.6$ V, $C_c = 0.15$ pF, $C_L = 0.2$ pF		

constraints are expressed by the common-mode range (CMR) and output swing (OS). The lower and upper limits of CMR and OS are given by

$$v_{CM\,\min} = -V_{SS} + V_{ov3} + V_{ov1} + V_{t1} \tag{19}$$

$$v_{CM\,\max} = V_{DD} - |V_{ov5}| + V_{t1} \tag{20}$$

$$v_{O\,\min} = -V_{SS} + V_{ov15} \tag{21}$$

$$v_{O\,\max} = V_{DD} - |V_{ov13}| \tag{22}$$

To operate properly for the circuit connection obtaining the unity-gain amplifier, there must be a substantial overlap between the allowable ranges of v_{CM} and v_O. For maximum output swing, the three bias voltages shown in Fig. 2 can be expressed as

$$V_{B5} = -|V_{ov5}| - |V_{t5}| \tag{23}$$

$$V_{B7} = V_{DD} - |V_{ov5}| - |V_{ov7}| - |V_{t7}| \tag{24}$$

$$V_{B9} = -V_{SS} + V_{ov11} + V_{ov9} + V_{t9} \tag{25}$$

The slew rate taking into account C_L can be obtained as

$$\mathrm{SR} = \min\left(\frac{I_{D3}}{C_c}, \frac{I_{D15} - I_{D3}}{C_L}\right) \tag{26}$$

The active area of the op amp is written as

$$\mathrm{Area} = a_r R_c + a_c C_c + \sum_{i=1}^{16} W_i L_i \tag{27}$$

and the quiescent power dissipation is given by

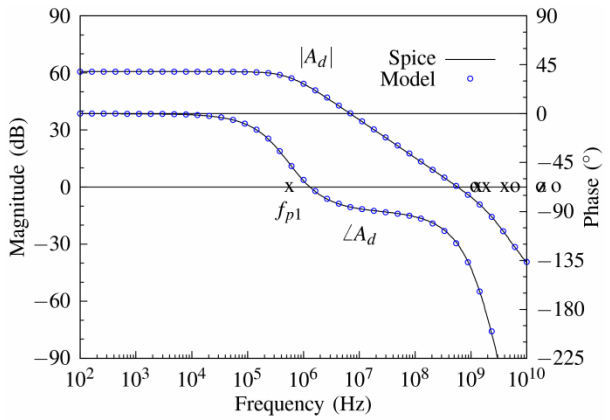

Fig. 5. Comparision of the transfer function model to Spice simulation for high speed op amp 1. Mark 'x' indicates a pole frequency, 'o' a zero frequency, and 'z' a pole-zero doublet.

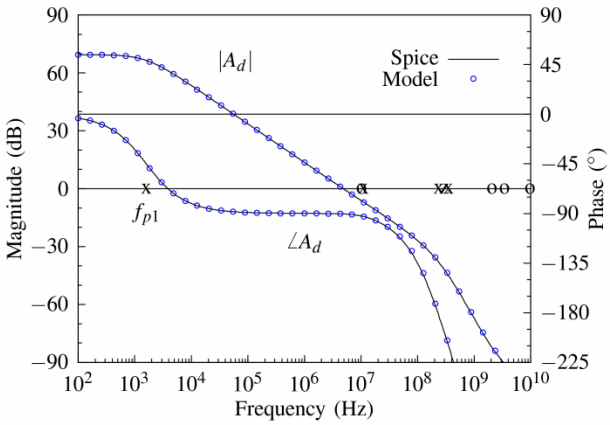

Fig. 6. Comparision of the transfer function model to Spice simulation for low power op amp 2 with dissipation of 2.5 μW.

$$P_D = (V_{DD} + V_{SS})\left[I_B + 2\left(|V_{D5}| + |I_{D13}|\right)\right] \qquad (28)$$

In order to get the op amp operating in strong inversion, a bias constraint for the overdrive voltage $V_{ov} \geq V_{ov\min}$ was imposed on each transistor of the op amp 1. For this high speed op amp, the comparison between the transfer function and Spice simulation is shown in Fig. 5. Because the small-signal model is valid up to about 10 GHz, the frequency is driven to that frequency. Although a pole and three zeros exceed the frequency limit of validity, their marks were indicated to show the relative positions of the pole and zeros. This op amp with C_L of 0.2 pF dissipates a quiescent power of 0.82 mW at supply voltages ±0.6 V and has a unity-gain frequency of 576 MHz. It can be seen that the Eqs. (3), (4), and (15) is an accurate model for the transfer function of the op amp in which all transistors are operating in strong inversion.

Finally, Fig. 6 shows the comparison between the transfer function and Spice simulation for the op amp 2 in which all transistors are operating in moderate inversion. In order to realize this operation, a special constraint for channel width W ≥ 0.65 μm was imposed on two transistors M_4 and M_5. This op amp has a unity-gain frequency of 4.8 MHz but operates with a very low power dissipation of 2.5 μW. It can be also seen that the derived transfer function is a good model even for the op amp operating in moderate inversion. For these two-stage folded-cascode op amps, the values of P_D, f_t, PM, dc gain, pole and zero frequencies are shown in Table 4.

Table 4. Values of power dissipation, unity-gain frequency, phase margin, dc gain, pole frequencies, and zero frequencies for high speed and low power 2-stage folded-cascode op amps

Performances, poles, and zeros	Op amp 1	Op amp 2
Power dissipation P_D	0.82 mW	2.5 μW
Unity-gain frequency f_t	576 MHz	4.8 MHz
Phase margin PM	60.0°	89.6°
$A_0 = \frac{g_{m1}g_{21}g_{m13}}{g_{o1}g_{11}g_{44}}$	60.7 dB	69.5 dB
$\omega_{p1} = \frac{g_{o1}g_{44}}{(g_{m13}+g_{44})(C_c+C_{gd13})}$	556 kHz	1.61 kHz
$\omega_{p2} = \frac{(g_{m13}+g_{44})(1+C_{gd13}/C_c)}{C_4+C_{gd13}}$	1.3 GHz	11 MHz
$\omega_{p3} = \frac{g_{11}}{C_{11}}$	1.9 GHz	236 MHz
$\omega_{p4} = \frac{1}{R_cC_2}$	4.1 GHz	356 MHz
$\omega_{p5} = \frac{g_{33}}{C_3 - C_{m8}}$	19 GHz	295 MHz
$\omega_{z1} = \frac{g_{m13}}{(g_{m13}R_c - 1)C_c}$	1.2 GHz	10.2 MHz
$\omega_{z2} = -\frac{g_{m1}}{C_{dg1}}$	–6.2 GHz	–2.1 GHz
$\omega_{z3} = -\frac{g_{m13}R_c - 1}{R_cC_{dg13}}$	–18 GHz	–3.4 GHz
$\omega_{z4} = \omega_{p5}$	19 GHz	295 MHz
$\omega_{z5} = -\frac{g_{21}}{C_{m6}}$	–34 GHz	–9.8 GHz

V. CONCLUSIONS

Using a high-frequency small-signal equivalent circuit with the complex transconductance, the fully differential two-stage folded-cascode CMOS operational amplifier was analyzed to obtain its small signal transfer function. As a result, the expressions for dc gain, five zero frequencies, five pole frequencies, unity-gain frequency, and phase margin were derived for op amp design using design equations. From comparing with Spice analysis, the good agreement between the transfer function model and simulation result has been observed for two op amps operating in either moderate or strong inversion. Thus the proposed transfer function could be usefully used in accurately designing the differential two-stage folded-cascode CMOS operational amplifiers.

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