Integrate-and-Fire Neuron Circuit and Synaptic Device with Floating Body MOSFETs

Min-Woo Kwon, Hyungjin Kim, Jungjin Park, and Byung-Gook Park*

***Abstract*—We propose an integrate-and-fire neuron circuit and synaptic devices with the floating body MOSFETs. The synaptic devices consist of a floating body MOSFET to imitate biological synaptic characteristics. The synaptic learning is performed by hole accumulation. The synaptic device has short-term and long-term memory in a single silicon device. I&F neuron circuit emulate the biological neuron characteristics such as integration, threshold triggering, output generation, and refractory period, using floating body MOSFET. The neuron circuit sends feedback signal to the synaptic transistor for long-term memory.**

***Index Terms*—Integrate-and-fire neuron circuit, synaptic transistor, long and short-term memory, floating body MOSFET**

I. INTRODUCTION

Until recently, the interest in biological system has increased and many researchers attempt to emulate neural networks that are characterized by parallel processing and low power consumption. Various types of synaptic devices based on resistive switching memory, and neuron circuits using a capacitor have been proposed [1-3]. Integrate-and-fire (I&F) neuron circuit was introduced to emulate biological neuron characteristics. "Axon-Hillock" model shown in Fig. 1 proposed by Mead [4] is the most representative model of the I&F neuron circuit. This circuit uses two capacitors and six transistors and is very simple and compact for integrating and firing. Many I&F neuron circuits are based on this "Axon-Hillock" model, and provide additional neuron characteristics [5-7]. Most of these circuits are constructed with a capacitor for the integration. Using a capacitor increases power consumption and delay time as well as size of the neuron circuits. These will be a critical problem, if many neuron circuits are integrated on a chip.

In this work, we propose a capacitor-less I&F neuron circuit with a floating body MOSFET whose behavior is similar to the 1-transistor DRAM. The capacitor-less 1T-DRAM does not need a storage capacitor, since it uses floating body to store holes made by impact ionization. And we propose silicon-based floating-body synaptic transistor (SFST) [8]. The synaptic device has the transition from short-term to long-term memory in a single silicon device.

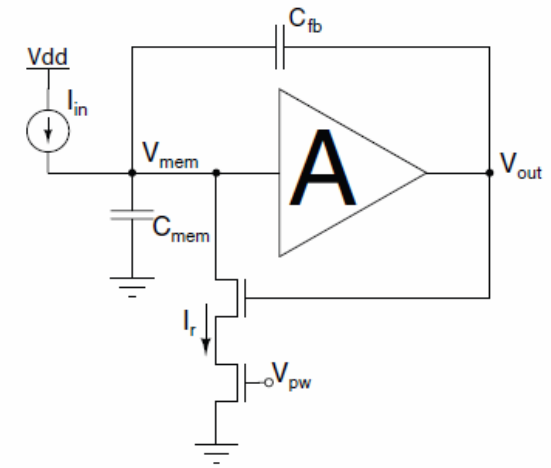

Fig. 1. Schematic of the axon-hillock circuit [4].

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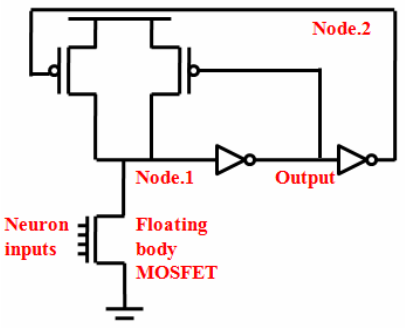

Fig. 2. Circuit diagram of integrated and fire neuron circuit.

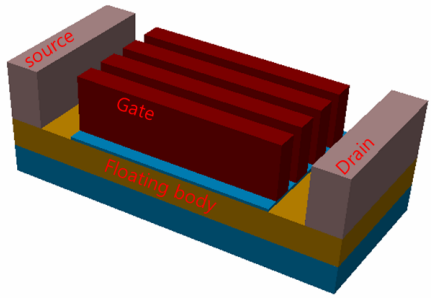

Fig. 3. Device structure of a 4-input floating body MOSFET.

II. I&F Neuron Circuit

1. Circuit Description

The diagram of the proposed I&F neuron circuit is shown in Fig. 2. The circuit comprises a floating body MOSFET, two p-type MOSFETs, and two inverters. P-type MOSFETs in Fig. 2 plays a role of feedback and makes Node 1 voltage high. The input voltage is applied to the gate, the floating body MOSFET turns on, and Node 1 voltage is decreased. Then, the output node voltage is increased by the inverter, which means the neuron circuit fires. Finally the neuron circuit is back to the initial state by feedback [9].

2. Multi-gate Floating Body MOSFET

The essential characteristics of the biological neuron are spatial and temporal integration, threshold triggering, output generation and refractory period. To emulate these properties, we use the multi-gate floating body MOSFET shown in Fig. 3.

The first neuron property is spatial integration. A real

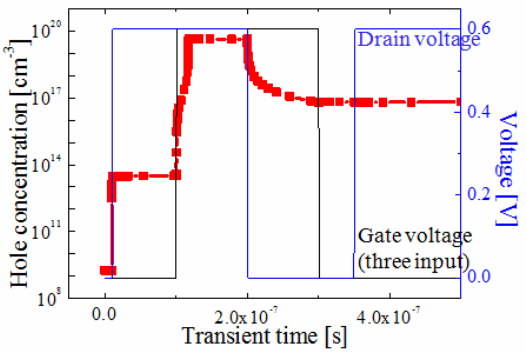

Fig. 4. Simulated hole concentration in the floating body when three-input voltage pulses are applied. When the gate and drain voltages are high, holes are accumulated.

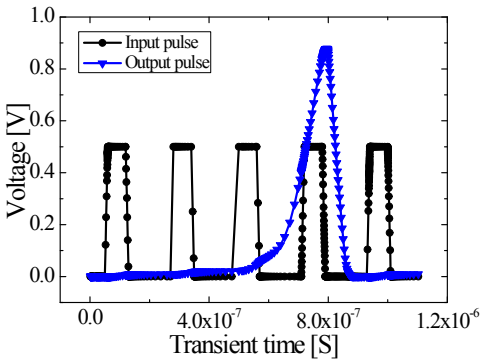

Fig. 5. Repeated low-voltage input pulse simulation result. The holes are accumulated during the first three input pulses, and then the neuron circuit is fired.

neuron has dendrites that connect with many pre-synaptic neurons and receive signals from them. And these signals are integrated. It is spatial integration. To emulate these properties, we use the multi-gate floating body MOSFET for dendrites and integration. When the signals from the many synaptic devices are applied to the gates, the current channel forms below each gate and the holes are made by impact ionization. These holes are integrated in the floating body. Fig. 4 shows the simulation result of the hole concentration in the floating body. The simulation was performed by SILVACO ATLAS. The input voltage is 0.6 V and input pulses are applied to the three gates. Holes are accumulated in the floating body, and the drain current is increased rapidly by the holes. As the drain voltage is 0 V, the holes in the floating body are erased and return to the initial state.

The second property is temporal integration. It is performed by the hole integration. This characteristic is

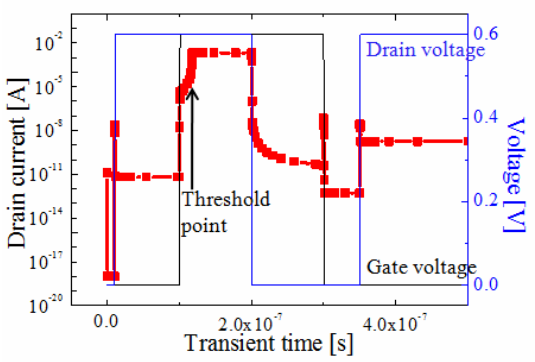

Fig. 6. Simulated drain current of the floating body MOSFET. Drain current increases very rapidly because of the accumulated holes.

shown in Fig. 5. When the pulse trains from one synaptic device are applied to the same gate, the holes are made by impact ionization at every pulse, and these holes are integrated in the floating body. After several input signals are applied, there are enough holes to generate output voltage. It is temporal integration property.

The third property is threshold triggering. The biological neuron has 'all-or-none' characteristics. If the accumulated signal is over the threshold potential, the neuron generates output signal to the other synapses. This property is performed by hole concentration in the floating body. As shown in Fig. 4, the holes are increasing exponentially at first. Because the holes make floating body potential lower, the current increases. And this current makes more holes by impact ionization. Because of this positive feedback, the number of holes is increasing very fast at the threshold point and the hole concentration saturates. The difference of the number of holes and drain current between saturation and non-saturation is about three orders of magnitude as shown in Fig. 6. Therefore, the circuit determines fire-or-not according to the hole concentration.

The final property is refractory period. If the neuron generates an output signal, the neuron returns to the initial state, and is not affected by the input signal. Most of I&F neuron circuits use an additional transistor to discharge the capacitor as shown in Fig. 1. But in this neuron circuit using a floating body MOSFET, the holes that accumulated in the floating body, are erased as shown in Fig. 4, when the neuron circuit generates the output signal.

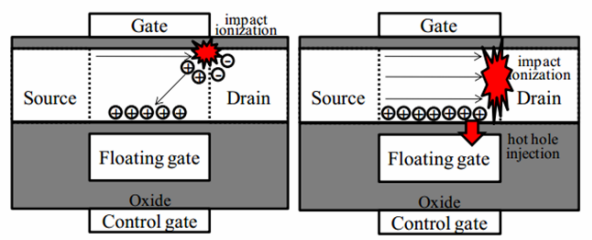

Fig. 7. Schematic view of (a) short term memory, (b) long term memory mechanism [8].

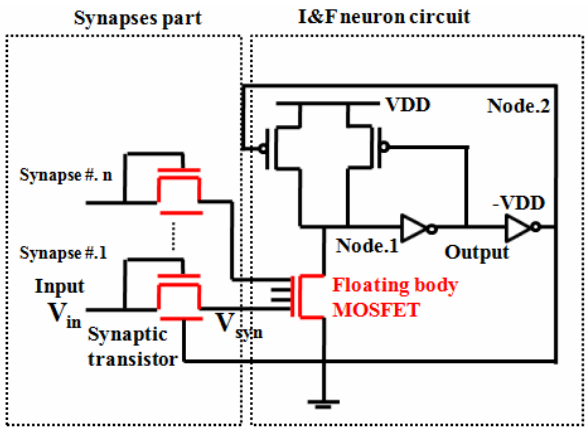

Fig. 8. Circuit description of synapse part and I&F neuron circuit. Each synapse consists of one floating body MOSFET.

III. Synaptic Transistor and I&F Neuron Circuit

1. Silicon-based Floating-body Synaptic Transistor

Fig. 7 shows the synaptic device structure. The structure is based on a floating body transistor for short term memory, and consists of a back floating gate and a back gate for long term memory. When the input pulse is applied to the gate and drain of the device, the conductance is increased and the threshold voltage is decreased temporarily due to the excess holes made by impact ionization in the floating body as shown in Fig. 7(a). When the holes in the floating body are saturated, newly generated holes are injected into floating gate by negative back gate bias from feedback and the hole injection results in long term memory as shown in Fig. 7(b).

2. Synaptic Transistor and I&F Neuron Circuit

The circuit diagram of the synaptic transistor connected with neuron circuit is shown in Fig. 8. The synaptic devices are connected with the neuron circuit.

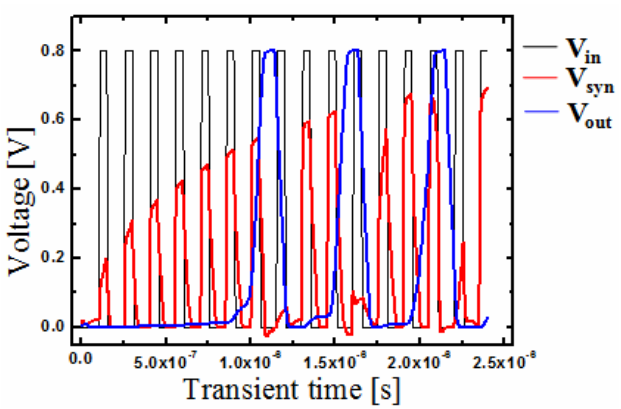

Fig. 9. Simulation result of synaptic device and neuron circuit. V_{syn} is increased at every input pulse due to the decreased threshold voltage of the synaptic device. After the synaptic learning, the required number of input pulses to generate neuron circuit output (V_{out}) is reduced.

The pre-synaptic input is applied to the gate and drain of the synapse and the source of the synapse is connected to the gate of the neuron circuit. And Node 2 of the neuron circuit is connected to the back gate of the synaptic transistor for long term memory. As the input pulse is applied to the gate and drain of the synaptic transistor, the holes are accumulated by impact ionization in the floating body of the synaptic transistor. So current drivability is increased, and the threshold voltage is decreased temporarily. Therefore, the amplitude of the voltage transferred by the synaptic transistor is increased in every input pulse. This result is shown in Fig. 9. The voltage of the source of synaptic device, V_{syn} in Fig. 8, is increased by the input pulse. It means that the synaptic device learns through experience. Before synaptic device learning, the neuron circuit requires many input pulses to generate output voltage. But, after the synaptic device learning, the neuron circuit needs just one or two input pulses for firing.

And the feedback voltage, from Node 2 of the neuron circuit to the back gate of the synaptic transistor, should be negative in order to inject holes into the back floating gate of the synaptic device for long term memory. So the second inverter in Fig. 8 is modified to connect negative V_{DD}. Fig. 10 shows the modified inverter and simulation result.

IV. Conclusions

In this paper, we proposed integrate-and-fire neuron

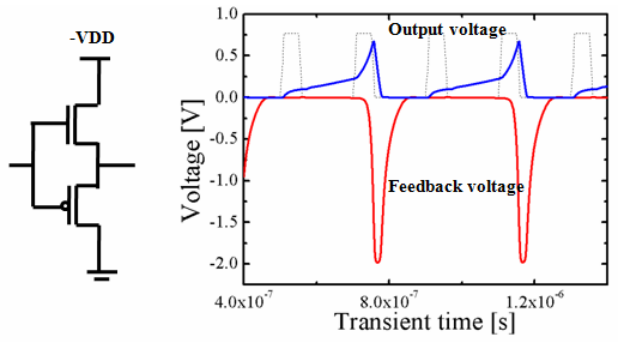

Fig. 10. Structure of the modified inverter and the simulation result. The NMOS has high body doping for negative bias. The negative voltage applied to the back gate in the synaptic device for long term memory.

circuit with a multi-gate floating body MOSFET and synaptic device interconnection. We can reduce the size of neuron circuit by using a floating body MOSFET that acts as an integrator. And we can emulate the characteristics of a neuron. Multiple gates act like dendrites, and performs spatial integration. Temporal integration is performed by the hole accumulation in the floating body. The threshold point is determined by the hole concentration in the floating body. The inverter components generate the output voltage to the other neuron, and the circuit is initialized by the feedback. The synaptic devices consist of a floating body transistor for short term memory, and consist of back floating gate and back gate for long term memory. The synaptic learning is performed by hole accumulation.

Acknowledgments

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