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Charge Controlled Meminductor Emulator

Maheshwar Pd. Sah[1,2], Ram Kaji Budhathoki[1], Changju Yang[1], and Hyongsuk Kim[1,*]

***Abstract*—Emulations of memristor-family elements are very important, since their physical realizations are very difficult to achieve with recent technologies. Although some previous studies succeeded in designing memristor and memcapacitor emulators, no significant contribution towards meminductor emulator has been presented so far. The implementation of a meminductor emulator is very important, since real meminductors are not expected to appear in near future. We designed the first meminductor emulator whose inductance can be varied by an external current source without employing any memrisitve system. The principle of our architecture and its feasibility have been verified using SPICE simulation.**

***Index Terms*—Pinched hysteresis loop, memristor, memcapacitor, meminductor, emulator**

I. INTRODUCTION

Memristors, memcapacitors, and meminductors are the three major elements of the memristor-family. They are passive circuit elements that store information in the form of resistance, capacitance, and inductance, respectively [1]. Although, these three elements are promising for the implementation of memory smaller than conventional silicon memories, they are not expected to be available in the market in near future. Utilizing emulators might be essential for the development of application circuits of memristor-family elements. Though there is active research on memristor and memcapacitor emulators [2, 3], there are not many studies on meminductors. The contributions toward meminductors are only confined to build mathematical models, spice macro models, and the transformation of memristive systems to memcapacitve and meminductive systems using mutator [4-8]. However, the mathematical model and spice macro models are only useful for simulation and cannot be used for physical implementable circuits. Similarly, the meminductor built in an indirect way by employing mutator is complicated and leads to difficulty in employing meminductor application circuits.

In this paper, we propose the first simple and dedicated meminductor emulator that does not require any mutator to transform memristor to meminductor. The features of the proposed meminductor has been verified via PSPICE circuit simulations.

II. PROPOSED MEMIDUCTOR EMULATOR

The relationship between the input current (i_{in}) and flux (φ) in the charge-controlled meminductor is defined as:

$$\varphi(t) = L_M(q)\, i_{in}(t) \qquad (1)$$

where $L_M(q)$ is the meminductance of a meminductor.

The basic idea to build a meminductor emulator is by composing the input inductance as a function of input current. Figs. 1(a) and (b) show the basic concept and its equivalent circuit respectively to design a meminductor emulator.

In Fig. 1(a), the relationship between input current i_{in} and flux φ generated across inductor L_s is given as:

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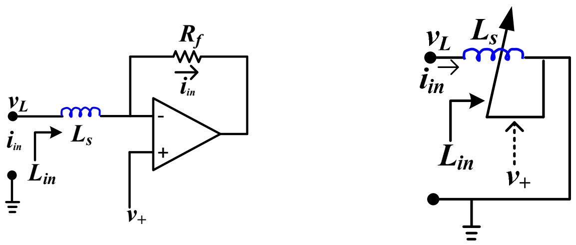
[1] Division of Electronics and Information Engineering and Intelligent Robots Research Center, Chonbuk National University, Jeonju, Jeonbuk, Republic of Korea
[2] Department of Computer Science and Engineering, University of Notre Dame, Indiana, USA
Corresponding Author, Hyongsuk Kim, E-mail : hskim@jbnu.ac.kr



(a) (b)

Fig. 1. Basic concept of proposed meminductor emulator (a) Input inductance as a function of voltage v_+, (b) Equivalent circuit.

$$\varphi(t) = L_s i_{in}(t) + \int v_+ dt \qquad (2)$$

where v_+ is the voltage across the non-inverting terminal of the OPAMP circuit.

If the integration of v_+ in (2) is composed in proportion to the input current i_{in}, then:

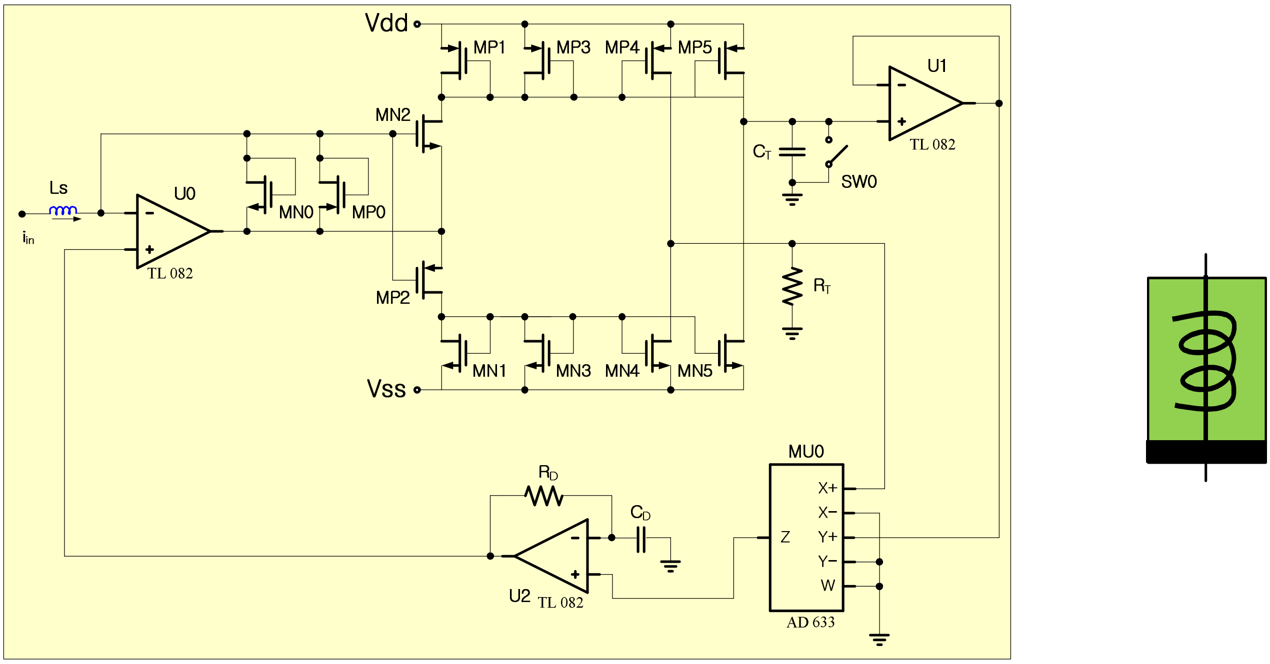
$$\varphi(t) = \left(L_s + m\right) i_{in}(t) \qquad (3)$$

where $\int v_+ dt = m\, i_{in}(t)$. Eq. (3) implies that the meminductance of the charge-dependent meminductor is defined as $(L_s + m)$. If m is controlled by the time integral of i_{in}, then the circuit of Fig. 1 acts as a meminductor whose inductance is variable depending upon the integration of the input current. An analog meminductor to emulate v_+ in (3) is constructed using a capacitor, a resistor, an analog multiplier, and a voltage differentiator, as shown in Fig. 2(a).

In Fig. 2(a), an inductor and feedback voltage v_+ are connected across the input terminal and the non-inverting terminal of OPAMP U_0, respectively. The input current i_{in} can be expressed in terms of the inductor voltage v_L and feedback voltage v_+ as:

$$i_{in}(t) = \frac{1}{L_s}\int \left(v_L(t) - v_+\right)dt \qquad (4)$$

The replicas of positive and negative currents are generated using NMOS and PMOS current mirrors and processed separately at different parts of the circuit [2]. As shown in Fig. 2(a), the positive part of the current, duplicated by a current mirror MN0 and MN2 is fed into a resistor R_T and a capacitor C_T by current mirror MP3 and MP4 with couple of MP1 respectively. On the other hand, MP0 and MP2 acts as the negative part of current mirror that flows out from resistor R_T and capacitor C_T by current mirror MN3 and MN4 with MN1 couple transistor, respectively. The capacitor C_T in our emulator



(a) (b)

Fig. 2 Architecture of proposed meminductor (a) Proposed meminductor emulator circuit, (b) Symbol of the meminductor.

stored programmed information in the form of charge. The buffer U1 avoids the discharging during the period when an input signal does not exist.

The voltage across capacitor C_T is the integration of mirrored current i_{in}, and the voltage across R_T is proportional to the mirrored current i_{in}. Let v_C and v_R be the voltage across C_T and R_T, respectively. Then,

$$v_C = \frac{1}{C_T}\int i_{in}(t)dt = \frac{q(t)}{C_T} \tag{5}$$

$$v_R = i_{in}(t)R_T \tag{6}$$

where $q(t) = \int i_{in}(t)dt$ is the charge across capacitor C_T.

A four-quadrant analog multiplier AD633 performs analog multiplication between voltages v_c and v_R respectively [9]. It includes high impedance, differential X and Y inputs, and high impedance summing input (W). The output and input relation of this multiplier is given by,

$$Z = \frac{(X_+ - X_-)(Y_+ - Y_-)}{10} + W \tag{7}$$

From Fig. 2(a), the output voltage v_{mul} of a voltage multiplier AD633 is given by:

$$v_{mul} = \frac{R_T}{10C_T} q(t) i_{in}(t) \tag{8}$$

The output voltage v_{mul} is fed to a differentiator composed of C_D, R_D, and OPAMP U3. The output voltage v_+ of the differentiator circuit can be expressed as:

$$v_+ = -\frac{R_T R_D C_D}{10C_T}\frac{d}{dt}\left[q(t)i_{in}(t)\right] \tag{9}$$

From (4) and (8), we get:

$$\varphi(t) = \left(L_s - \frac{R_T R_D C_D}{10C_T} q(t)\right) i_{in}(t) \tag{10}$$

Eq. (10) describes the operation of the meminductor circuit, in which the meminductance of the meminductor is:

$$L_M(q) = L_s - \alpha\, q(t) \tag{11}$$

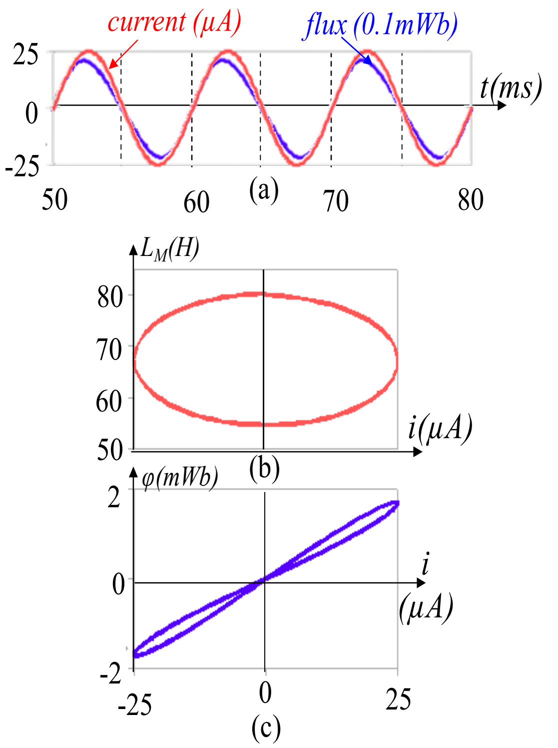


Fig. 3 Various waveforms measured across our meminductor emulator (a) *Input current, flux* with respect to time *t*, (b) *Meminductance (L_M) vs. current (i)*, (c) Pinched hysteresis loop on *φ vs. i* plane.

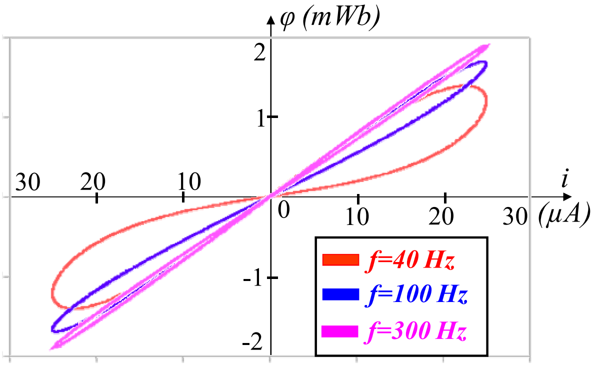


Fig. 4. Pinched hysteresis loops obtained with the proposed meminductor emulator for various frequencies.

where $\alpha = \dfrac{R_T R_D C_D}{10C_T}$.

III. SIMULATION RESULTS

PSPICE simulation was performed to verify the performance of the presented meminductor emulator. The parameters used for the simulations are ±5 V power supply, $C_T=0.1\ \mu F$, $R_T=4\ K\Omega$, $L_s=80\ H$, $C_D=0.8\ \mu F$, and

$R_D = 100\ K\Omega$.

One of the characteristics of a meminductor is a zero crossing pinched hysteresis loop under the φ versus i plane for any bipolar periodic signal. This feature was verified in the proposed meminductor emulator for a sinusoidal input current signal with a frequency of 100 Hz and amplitude of 25 µA. The input current signal and the corresponding waveforms of the flux measured across our meminductor emulator are shown in the Fig. 3(a). Figs. 3(b) and (c) are the corresponding variation of meminductance with respect to the applied input current (i) and the pinched hysteresis loop on the φ *versus* i plane, respectively. Observe that the loci on the φ *versus* i plane for the input signal exhibits zero crossing pinched hysteresis loop as expected.

Another characteristic of meminductors is the frequency dependency of the pinched hysteresis loop. The shape of the pinched hysteresis loop decreases as the frequency of the input signal increases. In our emulator circuit, the variation of flux (φ) and meminductance (L_M) depend on the charge (q) stored in the capacitor. If the frequency of the input signal is low, then the rate of change of q across capacitor is wide and vice versa. Therefore, the flux φ defined in (10) will be wider for low frequency and narrow for high frequency signal. In order to verify the pinched hysteresis fingerprint of a meminductor circuit, we carried out the simulation of the proposed circuit at 40 Hz, 100 Hz, and 300 Hz for a sinusoidal current signal with amplitude of 25 µA. Observe that, all of the φ versus i curves have a zero-crossing, and the shapes of the pinched hysteresis loops are shrunken as the frequency increases. All the pinched hysteresis loops of the proposed meminductor emulator satisfy the required fingerprints of a device to be meminductor.

IV. CONCLUSION

We presented a dedicated meminductor emulator without employing any memrisitve devices. The PSPICE simulations of the proposed architecture confirmed that our emulator satisfies all the criteria for a meminductor circuit. Since solid-state meminductor circuits are not expected to appear in the near future, our proposed meminductor emulator could be an inexpensive and simple solution to develop meminductor application circuits.

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Maheshwar Pd. Sah received the B.E. in Electronics and Communication Engineering from Pokhara University, Nepal in 2005, M.E. and Ph.D in Electronics Engineering from Chonbuk National University, Republic of Korea in 2010 and 2013 respectively, where he worked as a post-doctoral scholar from 2013 to 2014. He is currently working as a Postdoctoral scholar at University of Notre Dame, Indiana, USA. His main research interests include Emerging Transistor Technology, Circuit design, Cellular Neural Network, Analog viterbi decoder, analysis of Memristor and Memristive System.

Ram Kaji Budhathoki received the B.E degree in Electrical and Electronics Engineering from Kathmandu University, Nepal in 2001. He received M.E. degree from Pokhara University, Nepal in 2009. He joined Nepal Engineering College (nec), Nepal, in 2002 and has been an Assistant Professor at nec since 2007. He is curently working toward the Ph.D degree at the Division of Electronics Engineering, Chonbuk National University, South Korea. His current research interests include circuit design and analysis of memristor and memristive systems.

Changju Yang received the B.S and M.S. degree in Electronics and Information Engineering from Chonbuk National Univeristy Korea in 2008 and 2010 respectively, where he is currently studying toward the Ph.D. degree in Electronics and Information Engineering. His main research interests include Circuit design, Analog viterbi decoder, analysis of Memristor and Memristive System

Hyongsuk Kim received the Ph.D. degree in Electrical Engineering from the University of Missouri, Columbia, in 1992. Since 1993, he has been a Professor with the Division of Electronics Engineering, Chonbuk National University, Republic of Korea. From 2000 to 2002 and again from 2009 to 2010, he was with the Nonlinear Electronics Laboratory, EECS Department, University of California, Berkeley, as a Visiting Scholar. His current research interests include memristors and its application to Cellular Neural/ Nonlinear Networks.