

Macro-Model of Magnetic Tunnel Junction for STT-MRAM including Dynamic Behavior

Kyungmin Kim and Changsik Yoo

Abstract—Macro-model of magnetic tunnel junction (MTJ) for spin transfer torque magnetic random access memory (STT-MRAM) has been developed. The macro-model can describe the dynamic behavior such as the state change of MTJ as a function of the pulse width of driving current and voltage. The statistical behavior has been included in the model to represent the variation of the MTJ characteristic due to process variation. The macro-model has been developed in Verilog-A.

Index Terms—Macro model, magnetic tunnel junction (MTJ), spin transfer torque magnetic random access memory (STT MTJ), verilog-A

I. INTRODUCTION

The spin transfer torque magnetic random access memory (STT-MRAM) is considered as a promising technology that can replace the conventional memory because of its fast access time, infinite endurance, low power consumption, good scalability and non-volatility [1-3]. The magnetic tunnel junction (MTJ) for STT-MRAM consists of two ferromagnetic layers and a tunnel barrier between them. One ferromagnetic layer has fixed magnetization direction and is called pinned layer. The magnetization direction of the other ferromagnetic layer (called free layer) can be switched by an external force. The magnetization direction of the free layer is used to represent either '1' or '0' [2]. If the magnetization

directions of the pinned and free layers are parallel with each other, the MTJ has small resistance (R_p). On the contrary, the MTJ has high resistance (R_{AP}) when the magnetization directions of the pinned and free layers are anti-parallel. The ratio of the two resistance values R_p and R_{AP} is represented as tunnel magneto-resistance (TMR) which is defined as $(R_{AP}-R_p)/R_p$. It is desired to have as large a TMR value as possible for better noise margin when MTJ is used as a memory cell. For both read and write operations, a certain amount of current has to flow through MTJ and therefore the stored information on the MTJ may be disturbed during read operation [4]. MTJ may be switched to and from the parallel (R_p) and anti-parallel (R_{AP}) states depending on the amount of current flowing through it [2, 11]. The amount of current required to switch the MTJ state may change by the process variation, temperature, and bias level [5]. As shown in Fig. 1, the macro-model of MTJ has to be capable of modeling all the characteristics explained above in order to simulate the behavior of STT-MRAM.

The MTJ model presented in [1] can describe only the dynamic behavior but does not model the varying characteristic due to the process variation. Therefore it cannot predict the read and write failure due to the process variation. The MTJ model in [10] includes the effect of the process variation but does not consider the effect of the input stimulus waveform. Therefore it cannot fully predict the read disturbance for various environments.

In this paper, a macro-model of MTJ is described which can represent its dynamic behavior. The macro-model is developed in Verilog-A. Section II explains the basics of the switching of MTJ state and Section III describes how the dynamic behavior is modeled. The

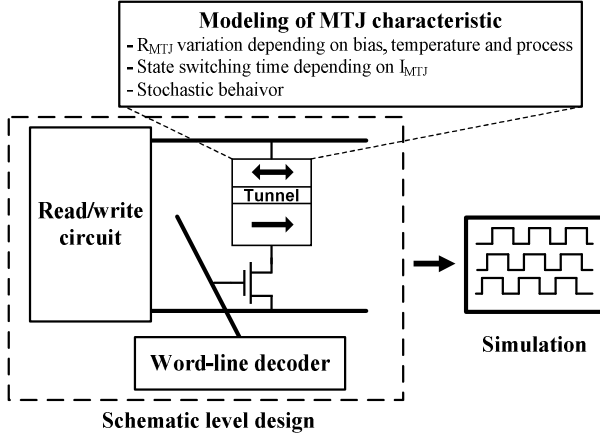


Fig. 1. Simulation of STT-MRAM with MTJ macro-model.

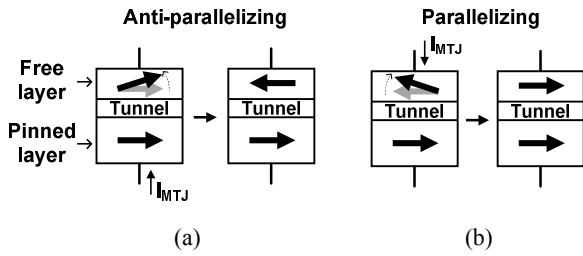


Fig. 2. Required current flow through MTJ for the switching (a) from the parallel state to the anti-parallel state, (b) from the anti-parallel state to the parallel state.

simulation results with the developed macro-model are shown in Section IV and finally the paper is concluded in Section V.

II. SWITCHING TIME OF MTJ

In order to switch the state of MTJ, a certain amount of current I_{MTJ} has to flow through it while the current direction differs for anti-parallelizing and parallelizing as shown in Fig. 2. Another factor that determines the switching of the MTJ state is how long the switching current I_{MTJ} flows through MTJ. Let's define the minimum required duration of the switching current flow for the switching of the MTJ state as the switching time τ_{SW} . The switching time τ_{SW} of MTJ is inversely proportional to the switching current I_{MTJ} [2, 6].

There are two operation regions for MTJ depending on the switching current magnitude I_{MTJ} [7-9]. The threshold current I_{C0} defining the operation region of MTJ is given as [4];

$$I_{C0} = (1/\eta) \cdot \alpha \cdot m \cdot (H + H_K + 2\pi M_S) \cdot (2e/\hbar) \quad (1)$$

where η is the spin polarization factor, α is the magnetic damping constant, m is the magnetization of free layer, H is the applied magnetic field, H_K is the effective anisotropy field, M_S is the saturation magnetization level, e is the charge of an electron, and \hbar is the Planck constant.

The spin polarization factor η and the magnetization of free layer m are given as;

$$\eta = \sqrt{TMR(TMR + 2)} / 2(TMR + 1) \quad (2)$$

$$m = M_S \cdot V_{FREE} \quad (3)$$

where V_{FREE} is the volume of free layer.

When $I_{MTJ} > I_{C0}$, MTJ is in the precession region where the average switching time $\langle \tau_{SW} \rangle$ is expressed as [8];

$$\frac{1}{\langle \tau_{SW} \rangle} = \frac{2}{C + \ln(\pi^2 \xi / 4)} \cdot \frac{\mu_B P_{PIN}}{e \cdot m \cdot (1 + P_{PIN} P_{FREE})} \cdot (I_{MTJ} - I_{C0}) \quad (4)$$

where the Euler's constant C is about 0.577, $\xi = \Delta E / k_B T$ is the thermal stability factor, $\Delta E = \mu_0 M_S V_{FREE} H_K / 2$ is the energy barrier height, k_B is the Boltzmann constant, T is the temperature, μ_B is the Bohr magneton, P_{PIN} and P_{FREE} are the tunneling spin polarization of the pinned layer and free layer, respectively.

When $I_{MTJ} < I_{C0}$, MTJ is in the thermal activation region and the thermal activation switching time is given as [9];

$$\langle \tau_{SW} \rangle = \tau_0 \exp \left[\frac{\Delta E}{k_B T} \cdot \left(1 - \frac{I_{MTJ}}{I_{C0}} \right) \right] \quad (5)$$

where τ_0 is the attempt period of nano-magnet.

III. DYNAMIC BEHAVIOR MODELING OF MTJ

In a conventional MTJ model, the switching time of MTJ state is modeled as a function of the bias current and voltage [10]. The pulse width of driving voltage and current, however, is not considered to model the switching time of MTJ state. Therefore, the read

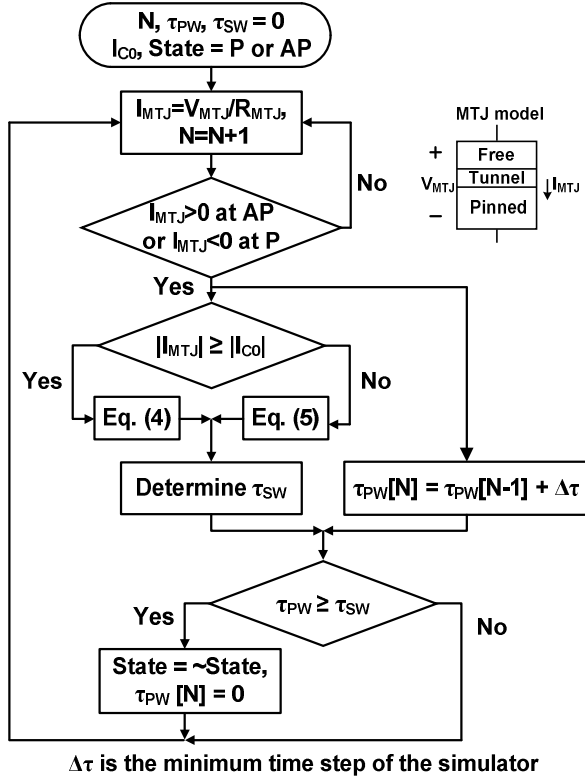


Fig. 3. Proposed algorithm for the modeling of the dynamic behavior of MTJ state switching.

disturbance cannot be modeled, which may be a serious issue in a short pulse reading scheme.

In the proposed MTJ model, the dynamic behavior of the switching of MTJ state is described by the algorithm shown in Fig. 3 which can take the pulse with of driving voltage and current into account. The resistance of MTJ is determined by bias voltage and current and the current state of MTJ.

Initially, the threshold current I_{C0} is calculated with the parameters shown in Table 1 by the equation in (1). Then, the bias current I_{MTJ} of MTJ is judged whether it can switch the state of MTJ considering the current state of MTJ and the direction of the bias current I_{MTJ} . If I_{MTJ} is negative when the MTJ is currently in the anti-parallel state or if I_{MTJ} is positive when the MTJ is currently in the parallel state, the MTJ state cannot be changed. Therefore, the remaining steps are skipped in the algorithm for fast simulation if it is determined that the MTJ state cannot be changed. If the flow of I_{MTJ} is in the correct direction so it can change the MTJ state, the magnitude of I_{MTJ} is compared with I_{C0} . If I_{MTJ} is larger than I_{C0} , the switching time is τ_{SW} is calculated by Eq. (4)

Table 1. Parameters

Parameter	Description	Default Value
H_K	Anisotropy field	1433 Oe
M_S	Saturation magnetization	15800 Oe
α	Magnetic damping constant	0.027
t_{ox}	Oxide barrier height	0.85 nm
TMR(0)	TMR ratio with $0V_{MTJ}$	70%
V_{FREE}	Volume of Free layer	area \times 1.3 nm
area	MTJ surface	40 nm \times 40 nm \times $\pi/4$
$P_{PIN}-P_{FREE}=P$	Tunneling spin polarization	0.52

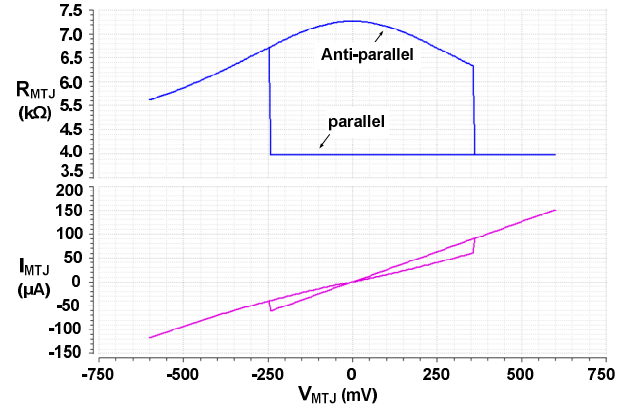


Fig. 4. DC simulation for hysteresis characteristic.

and if I_{MTJ} is smaller than I_{C0} , τ_{SW} is calculated by Eq. (5). The pulse width τ_{PW} of the driving current is increased at every step of simulation as $\tau_{PW}[N] = \tau_{PW}[N-1] + \Delta\tau$ and compared with the switching time τ_{SW} . When τ_{PW} becomes larger than τ_{SW} , the state of MTJ is changed and the variables are all initialized.

In order to model the stochastic behavior of MTJ, the random distribution function of Verilog-A has been utilized. The oxide barrier height t_{ox} , the volume of free layer V_{FREE} , and TMR can be randomly changed by the random distribution function of Verilog-A. As can be seen in the Eqs. (4) and (5), the switching time τ_{SW} varies with those stochastic parameters, especially V_{FREE} [9].

IV. RESULTS

In order to verify the above explained MTJ model, various simulations have been performed with the parameters in Table 1 [10].

The hysteresis characteristic of MTJ is confirmed with the DC simulation. Fig. 4 shows the resistance and current of MTJ as a function of bias voltage V_{MTJ} . The

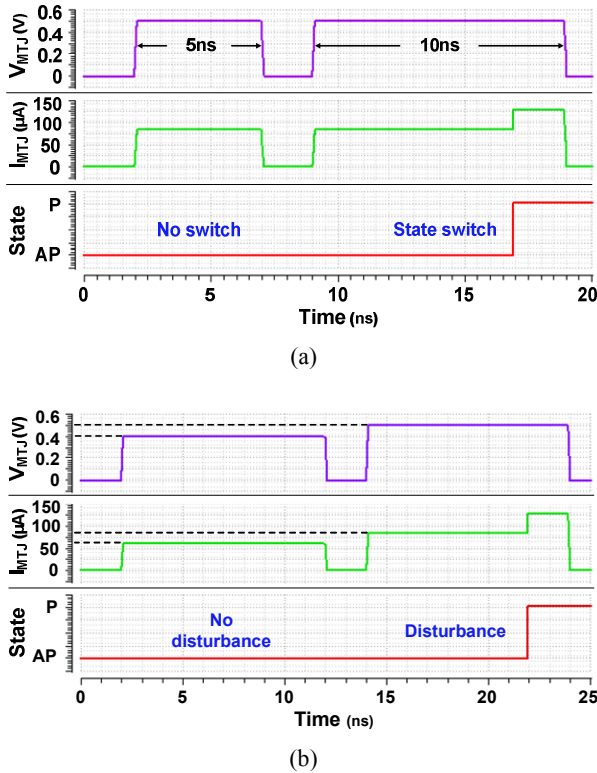


Fig. 5. The dynamic behavior of MTJ model (a) the switching state depending on pulse width of current, (b) read disturbance depending on current magnitude.

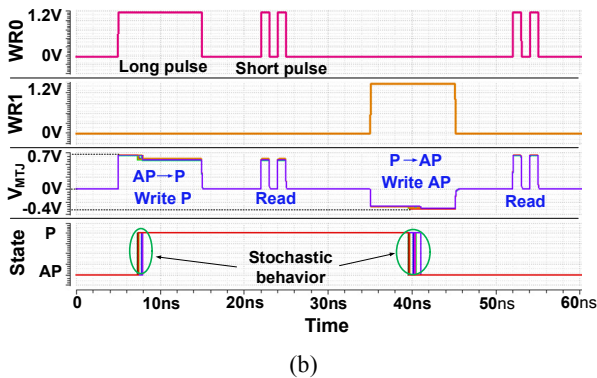
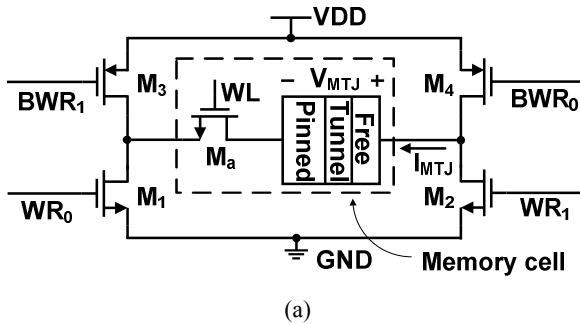


Fig. 6. (a) Test circuit for transient simulation, (b) simulation results.

hysteresis characteristic can be seen in the figure.

The dynamic behavior of MTJ model has been verified by the transient simulation as shown in Fig. 5. Fig. 5(a) shows the change of MTJ state as a function of the pulse width of driving current. In Fig. 5(b), it can be seen that the read disturbance can happen when the read current is unacceptably large.

To see the read and write operation of MTJ considering the dynamic and stochastic behavior, the test circuit shown in Fig. 6(a) has been built. The nMOS transistor M_a is the access transistor of MTJ memory cell while the transistors M_1, M_2, M_3, M_4 are read biasing and write driving transistors. If BWR_0 and WR_1 are LOW and BWR_1 and WR_0 are HIGH, the current I_{MTJ} can switch the MTJ state into the parallel state. When the driving voltage V_{MTJ} and therefore driving current is applied for a long time, the MTJ state is switched while the MTJ state does not change for a short driving pulse. The random variation of the switching time can be seen in the figure.

V. CONCLUSIONS

A macro-model of MTJ has been developed in Verilog-A which can represent its dynamic and stochastic behavior. The variation of the switching time of MTJ state for different driving pulse width can be modeled in the proposed macro-model. The stochastic behavior is also included in the model to see the random variation of the MTJ characteristic.

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