A 32 nm NPN SOI HBT with Programmable Power Gain and 839 GHzV f_tBV_{CEO} Product

Prasanna Kumar Misra and S. Qureshi

Abstract—**The performance of npn SiGe HBT on thin film SOI is investigated at 32 nm technology node by applying body bias. An n-well is created underneath thin BOX to isolate the body biased SOI HBT from SOI CMOS. The results show that the HBT voltage gain and power gain can be programmed by applying body bias to the n-well. This HBT can be used in variable gain amplifiers that are widely used in the receiver chain of RF systems. The HBT is compatible with 32 nm FDSOI technology having 10 nm film thickness and 30 nm BOX thickness. As the breakdown voltage increases by applying the body bias, the SOI HBT with 3 V V_{CE} has very high f_tBV_{CEO} product (839 GHzV). The self heating performance of the proposed SOI HBT is studied. The high voltage gain and power gain (60 dB) of this HBT will be useful in designing analog/RF systems which cannot be achieved using 32 nm SOI CMOS (usually voltage gain is in the range of 10-20 dB).**

Index Terms—**Body bias, sentaurus, SOI HBT**

I. INTRODUCTION

The performance of SOI HBT can be improved by applying body bias [1, 2]. The applied body bias in the HBT is quite large (0 V - 20 V). Using thin BOX the SOI HBT performance can be improved significantly [3] with low range of body bias (0 V - 3 V). However, isolation from SOI CMOS limits this application in SOI BiCMOS technology. In this article an isolation mechanism is proposed by creating an nwell. The nwell can be biased to improve the HBT performance. Circuit techniques have been reported for designing programmable amplifiers [4, 5]. In this paper, a new approach has been proposed for obtaining programmable ac characteristics in SOI HBTs. Using body bias the SOI HBT voltage gain can be programmed over wide range. Also this technique improves the f_tBV_{CEO} product of the HBT.

The paper has been organized as follows. The fabrication procedure, process and device simulation setup of the SOI HBT are discussed in section II. Simulation results of the body biased HBT have been studied in section III. Finally the conclusion is given in section IV.

II. FABRICATION PROCEDURE AND SIMULATION SETUP

An SOI substrate with film thickness of 10 nm and BOX thickness of 30 nm has been used. For ultrathin body, the HBT performance is poor and therefore an epi layer of 30 nm is deposited so that collector thickness would be 40 nm. A 2×10^{12} cm^{-2} dose at 70 KeV is used to create the nwell underneath the thin BOX. Then the collector doping of $5x10^{17}$ cm^{-3} is achieved by applying the same dose at 30 KeV. The depth of the nwell for the structure is 120 nm. The nwell has been created underneath the BOX to isolate the body biased HBT from SOI CMOS. Further, the fabrication procedure of the SOI HBT can be followed from [6] to complete the back gated HBT as shown in Fig. 1. The emitter area of the HBT is 0.04 μm^2 whereas the total device area is 0.6 μm^2. The base, emitter contact area of the device is 0.02 μm^2. For a contact height of 400 nm, the contact resistance is nearly 1 ohm. The reach through

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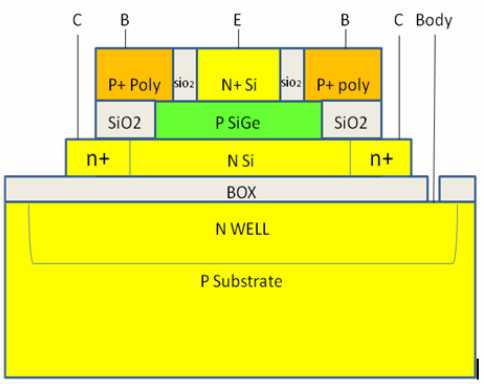

Fig. 1. Schematic of npn SOI HBT (Area=0.04 μm^2) with body bias (Emitter Length =40 nm and Emitter width =1 μm).

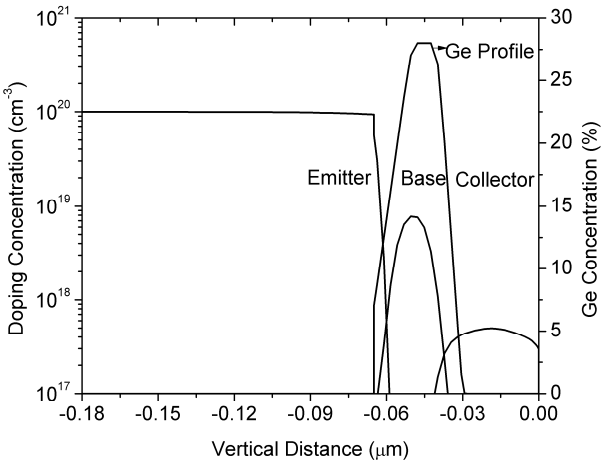

Fig. 2. Doping Concentration and Ge profile of npn SOI HBT.

region has been adjusted so that 250 nm of collector length is achieved.

The emitter, base, collector and reach through doping are 1× 10^{20}, 1×10^{19}, 5×10^{17} and 5×10^{19} cm^{-3} respectively. The emitter and base thickness are 100 nm and 20 nm respectively. The trapezoidal Ge profile (10 % -25 %) has been used in the base layer. The process simulations have been performed [7] by applying the above steps. From the simulation results, the doping and Ge concentration of the SOI HBT are obtained and plotted in Fig. 2.

III. Results and Discussion

After validating the device with the experimental results [6], the collector thickness, collector length, emitter area and BOX thickness values have been scaled to effectively use the body bias. The dc and ac characteristics of HBT are evaluated by using Sentaurus

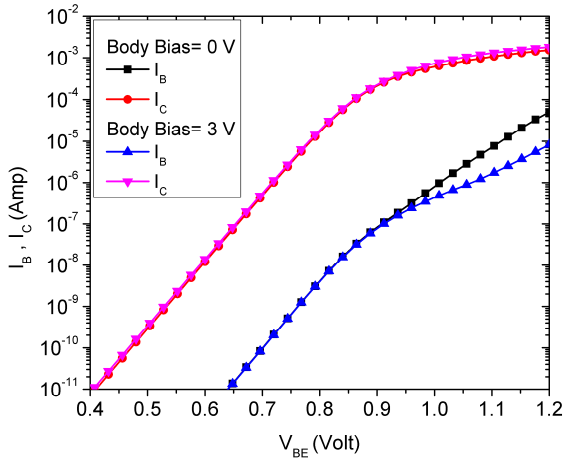

Fig. 3. Input DC characteristics of npn SOI HBT with body bias.

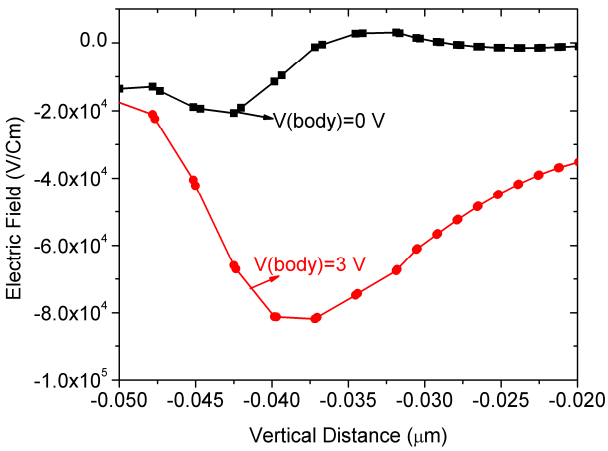

Fig. 4. Electric field of collector-base junction with body bias.

device simulator [8]. The simulation models and model parameters are discussed in [9].

The V_{CE} is 1.2 V and V_{BE} varied from 0 V to 1.2 V. The input DC characteristics have been obtained. The results are shown in Fig. 3 by applying body bias. It has been observed that the base current decreases and the collector current increases by applying the body bias to nwell. On application of body bias, the electrons get accumulated in the collector/BOX interface that reduces the collector resistance. Therefore, I_CR_C drop across the extrinsic part of the transistor (parasitic region) reduces. Hence the available voltage for the intrinsic device is higher. The electric field of reverse biased collector-base junction is plotted by applying the body bias as shown in the Fig. 4. The V_{BE} used for the simulation is 1.0 V. The availability of higher voltage increased the electric field

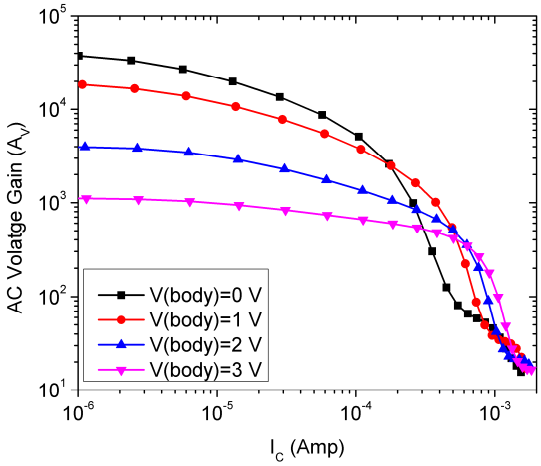

Fig. 5. Programmable voltage gain of npn SOI HBT with body bias.

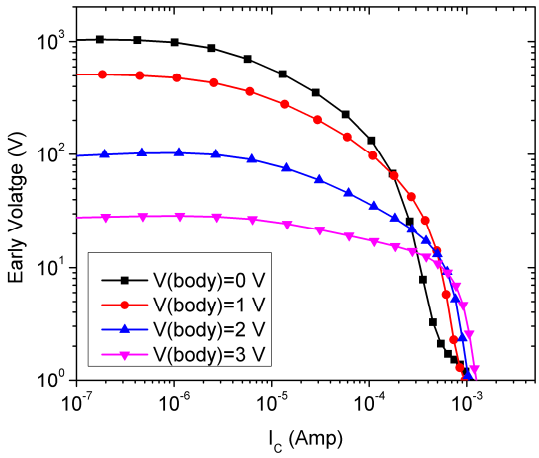

Fig. 6. Early voltage of npn SOI HBT with body bias.

in the base-collector junction for higher value of body bias. Therefore, the recombination of carriers in the neutral base region reduced. The reduction of recombination in base region decreased the value of base current. Hence higher collector current and lower base current can be achieved by applying the body bias.

The small signal analysis of the HBT has been performed at 1MHz frequency and the y-parameters have been obtained. From the results the voltage gain of the SOI HBT is evaluated and plotted in Fig. 5. The voltage gain of the device decreases due to the decrease in the output impedance (from low to moderate injection). From low to moderate injection, the AC voltage gain, A_v of the common emitter amplifier with ideal current load can be shown as given in Eq. (1).

$$A_v = g_m r_0 \tag{1}$$

At high injection, Y_{21}/Y_{22} value improves with body bias. From the plot it can be observed that the voltage gain of the HBT can be programmed by applying the low range of body bias. By applying body bias, the output impedance ($1/Y_{22}$) decreases. The early voltage of the device is plotted by varying the body bias as shown in Fig. 6. By applying body bias, the electron concentration increases in the collector region. To maintain the charge neutrality in the collector-base diode ($qN_AW_p = qN_DW_n$) the W_p value increases. N_A and N_D are the doping values of base and collector. W_p and W_n are the end of depletion regions in base and collector region. q is the unit charge.

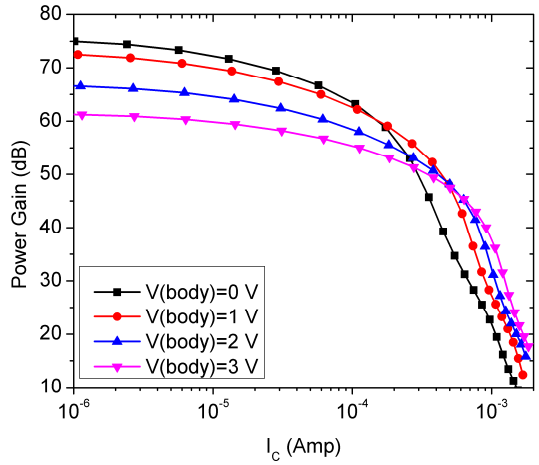

Fig. 7. Programmable power gain of npn SOI HBT with body bias.

The increase in W_p reduces the effective base width resulting in low output impedance when body bias is applied. The power gain, U from [10] that has been used to evaluate the power gain of body biased SOI HBT is given in Eq. (2). The results have been reported in Fig. 7 with different body bias.

$$U = \frac{\left|Y_{12} - Y_{21}\right|^2}{4\left(ReY_{11}ReY_{22} - ReY_{12}ReY_{21}\right)} \tag{2}$$

From the results it has been observed that the power gain of the HBT can be programmed by applying the body bias and therefore it can be used for programmable RF circuits. One major application is the variable gain amplifier in wireless receivers where body bias can be

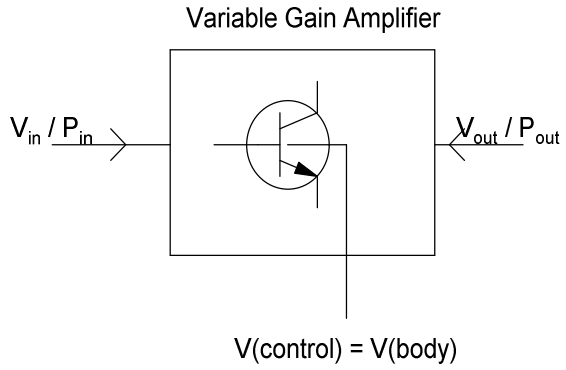

Fig. 8. Variable gain Amplifier with body bias.

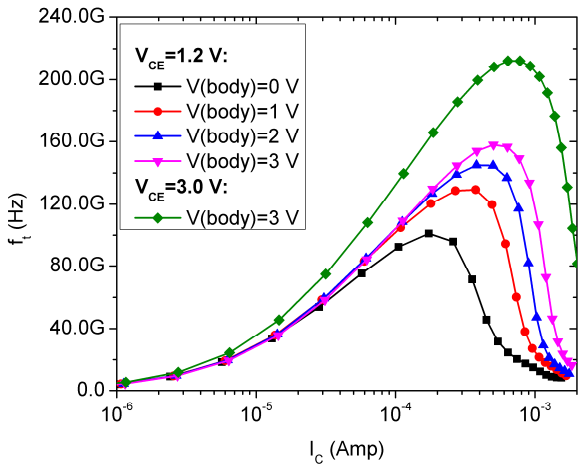

Fig. 9. f_t of npn SiGe HBT with body bias.

used as the control terminal.

When input power is low the control terminal can be grounded. For high input power the control terminal can be activated to avoid the amplifier saturation. The schematic is shown in Fig. 8. The f_t values and breakdown voltages are plotted by applying body bias as shown in Figs. 9 and 10 respectively. By applying the body bias, f_t and BV_{CEO} of SOI HBT improves. The f_t improves due to delayed saturation of the collector current. The Kirk current of the HBT [11] is shown in Eq. (3).

$$I_{C,Kirk} = qA_E v_{sat} N_C \left(1 + \frac{2\varepsilon(V_{CB} + \varnothing_{bi})}{qN_C W_C^2}\right) \quad (3)$$

where N_C is the doping value of the collector and W_C is the thickness of the collector. V_{CB} is the applied reverse bias voltage to the collector-base diode. The applied V_{CE} for the transistor is 1.2 V. By applying body bias, the

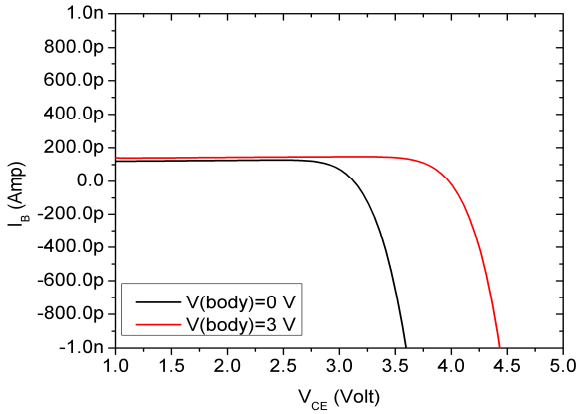

Fig. 10. BV_{CEO} of npn SOI HBT with body bias measured from base current reversal point at V_{BE}=0.7 V.

voltage drop ($I_C R_C$) across the lateral region of the collector reduces. The reduction of voltage drop increases the V_{CEeff} value ($V_{CEeff} = V_{CE} - I_C R_C$). Therefore, the effective voltage (V_{CEeff} and V_{CBeff}) available for the intrinsic transistor is higher when body bias is applied. So the Kirk current increases due to higher V_{CBeff} value available for the intrinsic part of the transistor. In addition to this, by increasing the body bias the n+ buried layer thickness increases (at Si/BOX interface). Therefore, the thickness of collector-base depletion layer decreases because the collector thickness is fixed (40 nm). So, the effective epi layer thickness (W_C) reduces. The improvement of Kirk current by scaling the epi layer thickness is reported in [12]. The onset of Kirk effect gets delayed due to the combined effect of available V_{CB} and W_C value. The increase of Kirk current reduces the charging time of the transistor. By applying 3 V V_{CE} and 3 V body bias, a maximum of 212 GHz f_t value can be obtained. At peak f_t value, the total input capacitance of the device is 4.25 fF. The BV_{CEO} value of HBT is measured from the base current reversal point at V_{BE} =0.7 V. By applying 3 V body bias to SOI HBT, 3.96 V of BV_{CEO} can be obtained. The generated electrons in the collector-base space charge region due to the impact ionization get accumulated at Si/BOX interface by applying body bias. Therefore, the number of generated carriers at the junction reduces by applying body bias. Therefore the maximum $f_t BV_{CEO}$ product of the SOI HBT is 839 GHzV at 3 V of V_{CE}. By applying 1.2 V of V_{CE}, 626 GHzV $f_t BV_{CEO}$ product can be obtained. As the performance of this HBT is very high, this can be used in future SOI BiCMOS technology. The

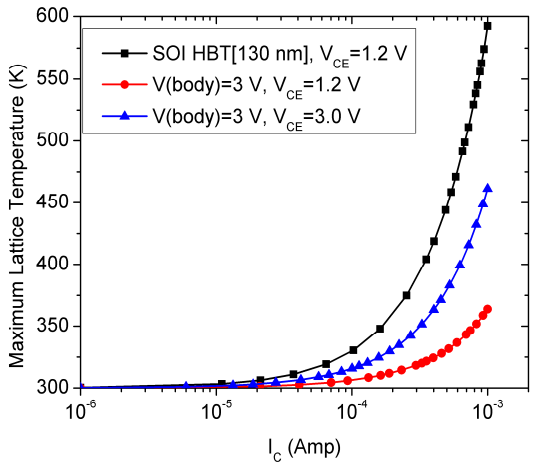

Fig. 11. Comparison of Maximum Lattice Temperature of SOI HBT. The geometry of 130 nm SOI HBT is given in [6].

body biased HBT can be used for designing programmable analog circuits and systems. The simulation setup for studying the self heating effect of the bipolar transistor can be found from [13]. The specific heat model parameters and thermal conductivity model parameters for Si and SiGe that have been used to analyze the self heating performance of the SOI HBT are discussed in [9]. Same values have been used for this simulation. The thermal performance of the experimental SOI HBT is reported in [14]. In our simulation, a thermal electrode is placed with surface resistance of 4000 $K\mu m^2/W$ at the bottom of the SOI HBT. As 2D simulation is used for this study, the width of the device is limited to 1 µm. Heat equation has been solved by coupling the temperature. From the simulation, the maximum lattice temperature of HBT is obtained and plotted in Fig. 11. From the results it has been observed that the self heating performance due to the increased supply voltage has been overcompensated by the thin BOX. At 3 V V_{CE}, the maximum lattice temperature of the HBT is 98 K higher compared to the HBT at 1.2 V at 1 mA of I_C. The thin BOX allows the HBT to be operated at higher supply voltages at comparable self heating performance with the HBT at 130 nm technology node. Further, the lateral collector length of the body biased HBT can be expanded to improve the breakdown voltage that can be used for high voltage applications.

Recently, the performance of lateral bipolar transistor on SOI [15] is investigated. The performance of lateral bipolar transistor benefits by scaling due to the base width reduction. The IBM's lateral bipolar transistor [15] has no base-push out effect. The breakdown voltage and the voltage gain of the vertical bipolar transistor is better compared the lateral bipolar transistor. This is due to reduction in collector-base space charge region in lateral bipolar transistor. The trans-conductance of vertical bipolar transistor is higher compared to the lateral one due to incorporation SiGe epi-layer. The chips based on lateral bipolar transistor will be cheaper due to simple fabrication compared to the vertical one.

IV. Conclusion

An nwell is created underneath thin BOX so that body biased SOI HBT can be isolated from SOI CMOS. The performance of SOI HBT is studied by applying body bias. From the results it is found that the voltage gain of the npn SOI HBT can be programmed by tuning the body bias. Further, the breakdown voltage of SOI HBT improves with body bias. A maximum of 839 GHzV of f_tBV_{CEO} product can be obtained by applying 3 V body bias using 3 V supply voltage. The body biased HBT can be used in analog circuits and its voltage gain and bandwidth can be programmed. One major application is variable gain amplifier in receiver chain of wireless frontend chips. The thin BOX would allow the HBT to operate at high current density as self heating performance is better than 130 nm SOI HBT.

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