

NoC 동기회로 설계를 위한 불안정상태 분석

Jiang Chong* · 김강철**

Analysis of Metastability for the Synchronizer of NoC

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요약

최근에 SoC 버스구조의 대안으로 NoC가 대두되고 있으며, NoC에서 다중클럭이 사용되어 클럭의 주파수는 같지만 clock skew 등으로 인한 위상차이가 발생하므로 데이터 전송 시에 클럭에 대한 동기회로가 사용되고 있다. 본 논문에서는 NoC 클럭의 위상차가 발생하는 경우 데이터의 손실이 발생할 수 있는 불안정상태 (metastability)를 정의하고 분석한다. 180nm CMOS 공정 파라미터를 사용하여 래치와 플립플롭을 설계하고, 1GHz 클럭을 사용하여 모의실험을 수행하였다. 모의실험 결과에서 출력에 로직 1과 0이 아닌 중간 값을 가지는 불안정상태를 래치와 플립플롭에서 확인하였다. 그리고 불안정상태 값이 상당히 긴 시간 동안 존재하여 온도, 공정변수, 전원 크기 등의 주변 환경에 의하여 출력 값이 변할 수 있어 입력값을 손실할 수 있다는 것을 확인하였으며, 이러한 결과는 NoC에서 위상차 동기회로 설계 시에 유용하게 사용될 수 있을 것이다.

ABSTRACT

Bus architecture of SoC has been replaced by NoC in recent years. NoC uses the multi-clock domains to transmit and receive data between neighbor network interfaces and they have same frequency, but a phase difference because of clock skew. So a synchronizer is used for a mesochronous frequency in interconnection between network interfaces. In this paper the metastability is defined and analyzed in a D latch and a D flip-flop to search the possibilities that data can be lost in the process of sending and receiving data between interconnects when a local frequency and a transmitted frequency have a phase difference. 180nm CMOS model parameter and 1GHz are used to simulate them in HSpice. The simulation results show that the metastability happens in a latch and a flip-flop when input data change near the clock edges and there are intermediate states for a longer time as input data change closer at the clock edge. And the next stage can lose input data depending on environmental conditions such as temperature, processing variations, power supply, etc. The simulation results are very useful to design a mesochronous synchronizer for NoC

키워드

Metastability, Mesochronous frequency, Synchronizer, NoC
불안정상태, 위상차주파수, 동조기, NoC

1. Introduction

As new silicon technologies are rapidly advancing in recent years, a number of IP modules and

I/O peripherals are comprised in a single chip called SoC(system on chip) to improve processing performance. And bus-based interconnection architecture does not meet the need for the performance

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접수일자 : 2014. 10. 17

심사(수정)일자 : 2014. 11. 21

게재확정일자 : 2014. 12. 15

required by systems[1]. The key challenge in SoCs design is the distribution of the centralized clock signal throughout the chip with acceptable low skew[2].

GALS(Globally Asynchronous, Locally Synchronous) clocking scheme is introduced since GS(Global synchronization) is no longer suitable for SoC in high frequency[3-4]. In GALS system, local synchronous modules are designed using conventional design techniques and a local clock generator is used for each of them. The modules operate synchronously in their own system but communicate with each other asynchronously due to the different local clock. Therefore benefits of GALS are lower power consumption and more availability of design and synthesis tools compared with asynchronous design. One of solutions for such a communication bottleneck is the use of NoC(network-on-chip) to interconnect the IP modules in SoC.

Metastability is a bloodcurdling disaster in digital circuits as for multi-clock domain systems. Multiple clock domains are connected through GALS. The mesochronous synchronizer(MS) is needed in different clock domains to synchronize the incoming data from transmitter(TX) to a local clock in a receiver(RX) with a phase difference like Fig. 1

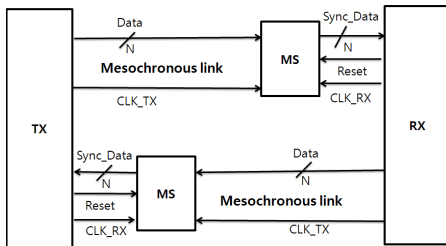


Fig. 1 Mesochronous clocking system

A latch is a bistable device with two stable states (0 and 1). Under the special conditions, the latch can enter a metastable state in which the output is at an indeterminate level between 0 and

1. Metastability is explained as the ball at the middle position as shown in Fig. 2. Any disturbance will cause the ball to roll down to one of the two stable states on the left or right side of the hill[5-6].

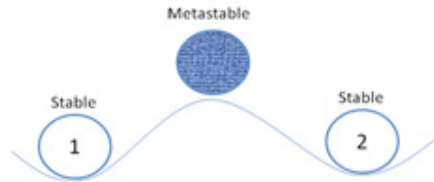


Fig. 2 Metastability model

MW(metastability window) can be defined as sum of setup and hold time as shown in Equation (1).

$$T_{MW} = T_{\text{setup}} + T_{\text{hold}} \tag{1}$$

For a flip flop, we can compute its MTBF(mean time between failures) which is a figure of merit related to metastability. MTBF as the reliability of synchronizer is given by Equation (2). The f_c, f_D , and S denote the frequency of the clock, the rate of the incoming data signal and the settling time allowed for synchronization between the clock domains respectively. Then τ and T_W are the metastability resolution time constant and its window of vulnerability[7].

$$MTBF = \frac{e^{S/\tau}}{T_W \cdot f_C \cdot f_D} \tag{2}$$

In this paper to provide the basic theories of metastability for a synchronizer of NoC with multiple clock domains, metastability event in D latch and DFF(D flip flop) is analyzed and MW is measured by HSpice using 180nm CMOS model parameter. This paper is organized as follows. Related works are presented in section II. In section III, metastability is analyzed in D latch and

DFF. Simulation results are shown in section IV and the conclusion is described in section V.

II. Related Work

For better data transfer between NoC interfaces there is need of synchronizer which synchronizes the different clock domains. The metastability occurs because of setup and hold time violations. This metastability cannot be avoided as input to the synchronizer is asynchronous. The occurrence of metastability can be minimized by synchronizer clock, data rate, setup and hold time window.

A high-throughput metastability-free GALS channel based on pausable clock method is proposed in [2]. The channel can be used as the interconnection of mixed-clock synchronous IP cores without having concerns about their synchronization. The proposed channel is simulated in 90nm CMOS process using predictive technology model(PTM) library. Gate delays and power parameters are extracted from Spice simulations and are back-annotated into its channel HDL code. The throughput, latency and power are analyzed and compared with existing designs.

Degradation of MTBF with technology scaling, calling for measurement and calibration circuits in 65nm and beyond is indicated by synchronizer metastability measurements[8]. Degradation of parameters can be even worse if the system is operated at extreme supply voltages and temperature conditions. The operations of synchronizers in a broad range of supply voltage and temperature corners are presented.

Synchronizer performance is based on MTBF (mean time between failures). Three experiments are done in [9] depending on frequencies of receiver and transmitter. Simulation results show that there is no data loss when the receiver frequency is higher and synchronizer is used.

A detailed study on the metastability behavior

for different high-performance flip-flops, reduced clock-swing flip-flops, and level-converting flip-flops with various circuit styles is conducted, and a novel pre-discharge flip-flop(PDFF) with positive feedback configuration is proposed in [10]. The simulation results show that PDFF achieves better metastability than the other flip-flops at both nominal voltage supply and nominal voltage supply with reduced clock-swing. The metastability window of PDFF is calculated based on two parameters extracted from simulations.

The metastability in shape of undefined output voltage can be converted into a late transition and so analog modeling is not required[11]. A more efficient modeling approach that is also tractable for large circuits is proposed based on modeling the dependence of the output delay on the temporal displacement between the data transition and the disabling of the latch. A mathematical model equation for this dependence is derived from a simplified circuit and shown how the model can be fitted to simulation data. The verified example shows that the model can be fitted to the simulation results very well[12-13].

In the future a mesochronous synchronizer will be used for NoC, but research of metastability and intermediate value are done in few papers. In this paper the metastability is defined and analyzed in a D latch and a D flip-flop to search the possibilities that data can be lost in the process of sending and receiving data between interconnects when a local frequency and a transmitted frequency have a same frequency with a phase difference

III. Metastability Analysis

D latch is transparent when a clock is high and it is opaque when a clock is low. The latch must be placed in each half-cycle and data can arrive at the latch anytime the latch is transparent[5].

When clock and data change simultaneously, the latch might lose the input data. While the clock in a D latch is turning off if the input data is not ready, the output of D latch might get an intermediate value because the input does not hold a final value. And after the clock turns off, we can't predict what value the output gets even though the intermediate value goes to high or low value. The value of output might be decided depending on the environmental conditions. This state is called metastability.

The clock period T_C is given equation (3), where t_{pcq} is a clock-to-Q propagation delay and t_{pd} is a logic propagation delay.

$$T_C \geq t_{pcq} + t_{pd} + t_{setup} \quad (3)$$

$t_{pcq} + t_{setup}$ is called a sequencing overhead. The latch can capture its input properly if the data changes outside a setup time before the clock edge.

The sum of setup and hold time is defined as a metastability, and the delays of rising and falling time in an input and a clock also affect the metastability occurrence, but it is not easy to measure metastability window in HSpice simulation. In this paper, metastability is defined that the output in D latch becomes intermediate when a switch turns off and the output of a master latch has a intermediate value in DFF when a switch turns on. The outputs can have one of three values such as 1, 0, intermediate value.

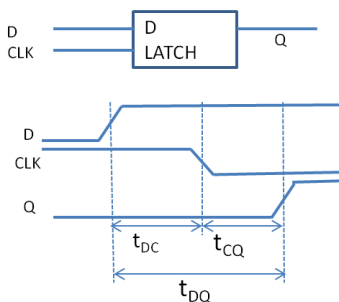


Fig. 3 D latch delay vs. data arrival time

Fig. 3 shows the timing of D latch, where t_{DC} is the time that the input data set up before the clock edge, t_{CQ} is the delay from clock to Q, and t_{DQ} is the sum of t_{CQ} and t_{DC} .

If the data arrive before setup time, t_{CQ} is very short and Q follows input data. As the data move closer to the falling edge of the clock, t_{CQ} begins to rise like Fig. 4. QB1 shows that the period of ambiguous state of Q is not longer than a half clock cycle when input data is not closer to the falling edge of clock inside setup time, but if input data is much closer to the falling edge of clock, the period of ambiguous state of Q is longer than a half clock cycle like the waveform of QB2. The output might be 0, 1, or intermediate state depending on the environments such as supply voltage, threshold voltage, temperature, etc.

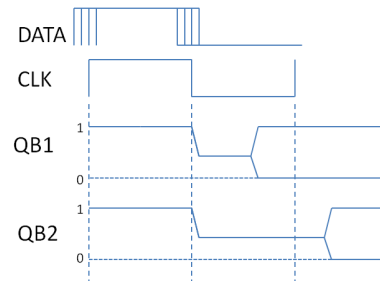


Fig. 4 Metastability in D latch as tDC

Fig. 5 shows the timing of positive edge triggered DFF. When a clock is low, a master latch and a slave latch are disconnected. When the clock goes

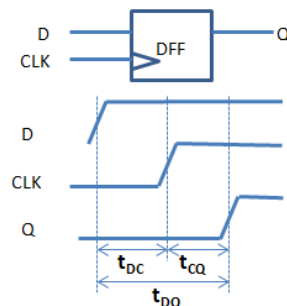


Fig. 5 DFF delay vs. data arrival time

high, input data D is captured. But if t_{DC} is too short or if the D input changes much closer to the rising edge of the clock, output Q might be intermediate.

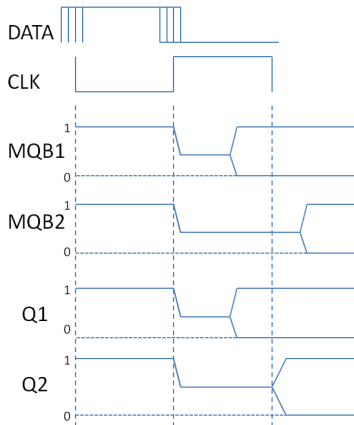


Fig. 6 Metastability in DFF depending on t_{DC}

MQB1 and MQB2 in Fig. 6 show the waveforms of master latch in D-FF. When the input changes longer before and after the clock rising edge in the inside of t_{DC} , output of master latch has a short intermediate level and goes to 1 or 0 like the waveform MQB1. Q1 has one value of 1 or 0. When the input changes in the inside of t_{DC} closer before and after the clock rising edge, output of master latch has a long intermediate level like MQB2. Q2 has one value of 1 or 0. For this period the output of DFF can get one of 1, 0, or intermediate value, but its final value depends on environmental conditions.

IV. Simulation Results

In this paper 180nm CMOS model parameter and 1 GHz are used in HSpice simulation.

To consider the effect of rising and falling time in clocks of a latch, ideal CLK and CLKB without rising and falling time are used in Fig. 7, but there is no a inverter for CLKB.

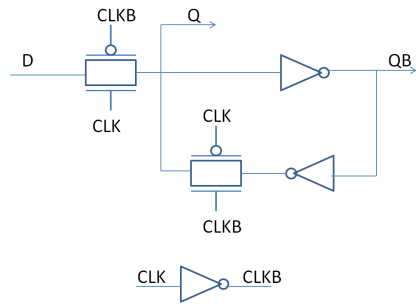
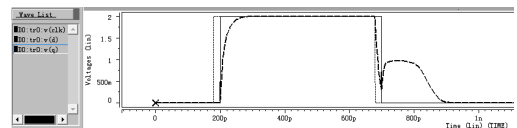


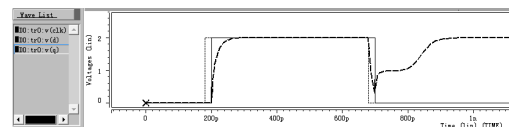
Fig. 7 D latch

Fig. 8 shows the simulation results of D latch with ideal CLK and CLKB. CLK changes to zero at 700ps without any falling time and input data changes to zero at 679.36ps (a), 679.37ps (b) and 680ps (c) respectively. Ideal clocks are used in this simulation, but the results show that the intermediate value appears near 679.36ps and the metastability exists. There is about 20ps time difference between CLK and D because of the delay in a CMOS switch between D and latch. The simulation results also show that the D latch with zero rising and falling time delay in a input and a clock has metastability.

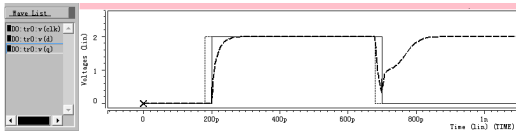
If the intermediate value of the output appears for a little long time after the clock goes low, a latch in next stage can capture an intermediate value and might receive wrong value even though the output of the latch finally goes to correct value.



(a) Falling time of input data : 679.36ps



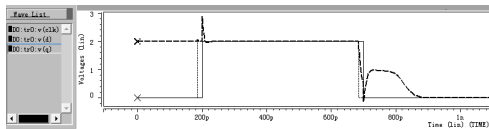
(b) Falling time of input data : 679.37ps



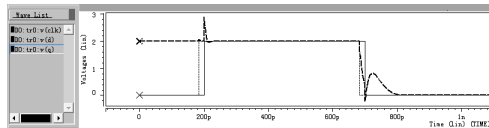
(c) Falling time of input data : 680ps

Fig. 8 Simulation results of D latch with ideal CLK and CLKB

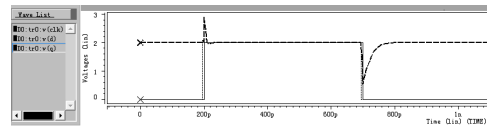
Fig. 9 shows the simulation results of D latch with practical clocks CLK and CLKB that comes from an inverter followed by CLK in Fig. 6. CLK goes to zero at 700ps and input data go to zero at 684.96ps (a), 683ps (b), and 695ps (c) respectively. In Fig. 9 (a) Q output has an intermediate state for more than 100ps and it shows D Latch is in a metastability, but D outputs have 0 at 683ps and 1 at 695ps. So it makes sure that meatstability window is very narrow and the metastability time happens at about 5ps later compared to D latch with ideal clock because of the delay in CLKB.



(a) Falling time of input data : 684.96ps



(b) Falling time of input data : 683ps



(c) Falling time of input data : 695ps

Fig. 9 Simulation results for D latch with practical clocks

Fig. 10 shows a rising edge triggered logic diagram of D-FF. To make practical input and clock,

two inverters are used after D and four inverters are used for CLK and CLKB.

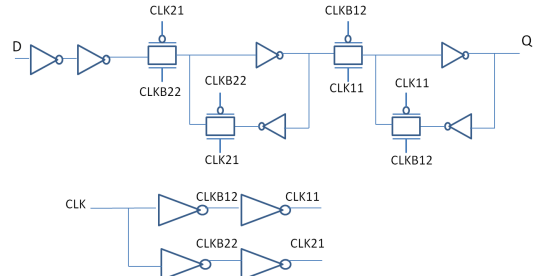
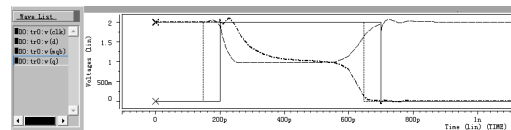
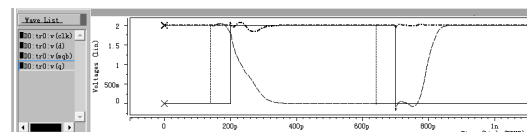


Fig. 10 Logic diagram of DFF

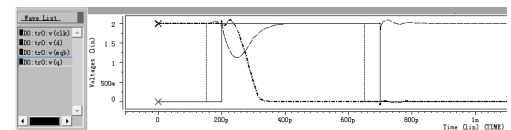
Fig. 11 shows the simulation results of D-FF and CLK goes to 1 at 200ps and input data goes high at 146.211ps (a), 140ps (b), and 150ps (c) respectively. MQB is the waveform of output in master latch. Fig. 11 (a) shows that the output Q keeps an intermediate value for a long time near the metastability point, but in the outside of it the output Q follows the input D without an intermediate value like Fig. 11 (b) and (c). In DFF the metastability window is very narrow.



(a) Rising time of input data : 46.211ps



(b) Rising time of input data : 140ps



(c) Rising time of input data : 150ps

Fig. 11 Simulation results for DFF

The above simulation results show that the network interfaces without a synchronizer can lose input data depending on environmental conditions such as temperature, processing variations, power supply, etc.

V. Conclusion

One of the most important challenges in SoCs is to design the distribution circuit of the centralized clock signal with acceptable low skew.

In this paper metastability event in a latch and a DFF is analyzed by HSpice using 180nm CMOS model parameter. The simulation results show that the metastability happens in a latch and a flip-flop when input data change near the clock edges and there are intermediate states for a long time when the clock edge changes if input data change much closer in the clock edge. So the network interfaces without a synchronizer can lose input data depending on environmental conditions. The simulation results are very useful to design a mesochronous synchronizer for NoC.

Our future work is to design a mesochronous synchronizer based on simulations results of metastability

감사의 글

이 논문은 2013년도 전남대학교 학술연구비 지원에 의하여 연구되었음.

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