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An Analytical Modeling and Simulation of Dual Material Double Gate Tunnel Field Effect Transistor for Low Power Applications

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Abstract – In this paper, a new two dimensional (2D) analytical modeling and simulation for a Dual Material Double Gate tunnel field effect transistor (DMDG TFET) is proposed. The Parabolic approximation technique is used to solve the 2-D Poisson equation with suitable boundary conditions and analytical expressions for surface potential and electric field are derived. This electric field distribution is further used to calculate the tunnelling generation rate and thus we numerically extract the tunnelling current. The results show a significant improvement in on-current characteristics while short channel effects are greatly reduced. Effectiveness of the proposed model has been confirmed by comparing the analytical results with the TCAD simulation results.

Keywords: Tunnel field effect transistor (TFET), Band to band Tunnelling, Poisson equation, Surface potential, Electric field.

1. Introduction

The performance of nanoscale complementary metal-oxide-semiconductor (CMOS) has degraded due to their aggressive scaling [1]. Due to this aggressive scaling the metal oxide semiconductor (MOS) device severely affected by short channel effects (SCEs) such as drain induces barrier lowering and extensive increase in leakage current [2]. Moreover the subthreshold swing of the MOS is limited to 60mV/decade at room temperature [3]. To overcome this, several alternative device structures such as tunnel field-effect transistors (TFETs) [4], impact ionization Metal oxide semiconductor field effect transistors (MOSFETs) [5], MOSFETs with a ferroelectric insulator as a gate oxide [6] and sandwich tunnel barrier FETs [7] have been proposed. TFET is a promising device to replace the conventional MOSFET for low power applications [8]. The applications of TFETs includes implementation on digital circuits like NAND, NOR and in six transistor SRAM memory cell [9].

Due to its built-in tunnel barrier, the TFET device does not suffer from short channel effects, when compared to the conventional planar MOSFET devices [10]. The subthreshold swing of a TFET is less than 60mV/decade at room temperature [11], which is the physical limit of the MOSFET, and in addition, TFETs show a very small leakage current in the range of femto amperes (fA)[12] when the device is turned off. In spite of all these merits, one factor that deters the performance of a TFET is its low ON-current (I_{ON}). Therefore various techniques to improve the I_{ON} of TFETs have been suggested.

In order to enhance the ON current (I_{ON}), various design improvements in terms of band gap engineering [13], hetero junction TFETs [14] strained silicon [15], novel architectures like carbon nanotube TFETs [16] and Double Gate (DG) TFET [17] has been proposed. Boucart et al. [17] proposed a DG TFET structure that shows significant improvements compared with single-gate devices using a SiO_2 gate dielectric. Saurabh et al. [18] proposed the application of Dual Material Gate (DMG) concept in a double gate structure to optimize the I_{ON}, I_{OFF} and SCEs.

The above works on TFET deal only with simulation and only a few analytical models were proposed. Bardon et al. [19] proposed potential and electric field model for a Double Gate TFET using pseudo 2-D solution. 1-D Poisson's equation based modeling of TFET has been proposed by Verhulst et al. [20]. Lee [21] proposed an analytical model of Single Gate (SG) TFET using superposition method, which is highly complex for calculations. Analytical models would be useful to provide fast results, together with further insight on the working principle of the device, and to allow circuit simulations [19].

In this paper, we propose a new analytical model for DMDG TFET structure which enhances the I_{ON} current during device operation. The aim of this work is, to study the potential benefits offered by the DMDG TFET by using parabolic approximation technique for the first time, which is simple and accurate. The analytical model is developed using two dimensional solution of Poisson equation. This model is used to calculate the surface potential and electric field distribution in the device under the two metal gates and the drain current I_{DS} is derived from the electric field using Kane's model. This paper is organized as follows: Section 2 shows model derivation of this work. The result

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and discussions are analyzed in Section 3 and Section 4 contains a summary of the conclusions.

2. Model Derivation

A schematic structure of the DMDG TFET is shown in Fig. 1 with gate metals M_1 and M_2 of lengths L_1 and L_2, respectively. The device parameters are listed in Table .1 The source and drain are made of highly doped p-type and n-type regions with carrier concentration of $10^{20}cm^{-3}$ and $5\times10^{18}cm^{-3}$ respectively. The intermediate channel region is made of a moderately doped p-type layer with a concentration of $10^{17}cm^{-3}$.The work function of the gate material near the source ϕ_{m1} is lower than the one near the drain ϕ_{m2}. This work function variation demonstrates the benefits of high performance proposed DMDG TFET device over their single material gate TFET device [18]. The operation of tunnel field effect transistors is entirely different from conventional MOS devices. The analysis of DMDG TFET operation [18] has been done by considering two separate cases of varying work functions ϕ_{m1} and ϕ_{m2} alternatively to get improved I_{OFF} and I_{ON} current.

Case (i): In the OFF-state, there is no band overlap on the source side, when the metal work function ϕ_{m1} is reduced to 4.0 eV, and hence, the I_{OFF} is expected to be quite low. In the ON-state, with the reduction in ϕ_{m1}, the band overlap increases, and the tunnelling width decreases, leading to a significant increase in the tunnelling probability on the source side. Hence the electrons tunnel from the valence band of the p-doped source to the conduction band in the intrinsic body and then move towards the n-doped drain by drift diffusion.

Case (ii): In the OFF-state, as ϕ_{m2} is increased, the tunnelling width increases, and the band overlap decreases on the source side, leading to a considerable reduction in the OFF-state tunnelling probability. In the ON-state, the increase in ϕ_{m2} does not change the band diagram significantly. In our model, we assume that the device is operated in the subthreshold region. And there is no assumption made in the depletion of the source and drain region has been assumed.

The only limitation of TFET is the presence of an ambipolar state [22] which means conduction in two directions (i.e. both for positive gate voltage and negative gate voltage). It is caused due to the transfer of tunnel junction from source side to the drain side when the gate voltage $V_{GS}<0$ for an n-type TFET operation. The basic requirement for an ideal switch in digital circuits is to work in only one direction, but if it also starts conducting in other direction this can create a problem in complementary logic circuit applications and thus limits the utility of the device for digital circuit design.

Table 1. Process parameters for simulated DMDG TFET

Quantities	Symbol	value
Oxide thickness	t_{OX}	2nm
Silicon body thickness	t_S	10nm
Channel length	L_1	10nm
	L_2	10nm
Gate work function	ϕ_{M1}	4eV
	ϕ_{M2}	4.4eV

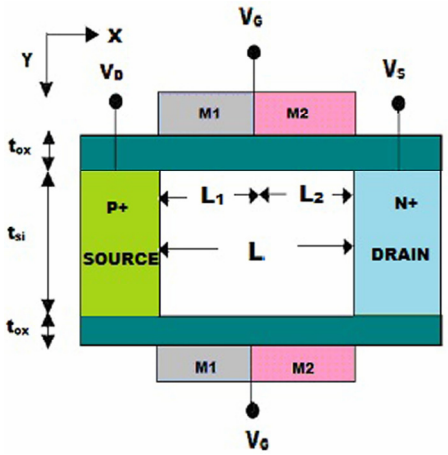

Fig. 1. Schematic diagram of a DMDG TFET

2.1 Surface potential

The potential distribution in the gate oxide region is distinguished by two dimensional Poisson's equation/ Laplace Eq. (21).

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=0 \tag{1}$$

The potential profile in the vertical direction is assumed to be a second-order polynomial [9], i.e.,

$$\phi(x,y)=c_0(x)+c_1(x)y+c_2(x)y^2 \tag{2}$$

The boundary conditions in the channel region are:

(a) Electric flux at the front-oxide gate interface is continuous for DMG TFET, therefore

$$\frac{d\phi_1(x,y)}{dy}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s_1}(x)-\psi_{g_1}}{t_{ox}} \quad \text{Under } M_1 \text{ at } y=0 \tag{3}$$

$$\frac{d\phi_2(x,y)}{dy}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s_2}(x)-\psi_{g_2}}{t_{ox}} \quad \text{Under } M_2 \text{ at } y=0 \tag{4}$$

Where $\psi_{g1}=V_{gs}-\phi_{m1}+\chi+E_g/2$

$\psi_{g2}=V_{gs}-\phi_{m2}+\chi+E_g/2$

(b) Electric flux at the back gate-oxide and the back channel interface is continuous for both the material

$$\frac{d\phi_1(x,y)}{dy}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\ \frac{\psi_{g_1}-\phi_{s_1}(x)}{t_{ox}}\quad \text{Under } M_1 \text{ at } y=t_{si} \tag{5}$$

$$\frac{d\phi_2(x,y)}{dy}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\psi_{g_2}-\phi_{s_2}(x)}{t_{ox}}\quad \text{Under } M_2 \text{ at } y=t_{si} \tag{6}$$

(c) The potential at the source and drain end is

$$\begin{aligned}&\phi_1(x,y)=\phi_{s_1}(0)=V_{bi}\\&\phi_2(L_1+L_2,0)=\phi_{s_2}(L_1+L_2)=V_{bi}+V_{DS}\end{aligned} \tag{7}$$

Where V_{bi} is the built in potential, E_g is Band gap energy, q is elementary charge, V_{GS} is Gate to Source voltage, V_{DS} is Drain to Source voltage, ε_{si} is relative permittivity of silicon and ε_{ox} is relative permittivity of silicon dioxide.

In the present analysis, we have two materials in the gate, the 2D potential under Material1 (M_1) and Material2 (M_2) can be obtained from Eq. (2).

$$\phi_1(x,y)=\phi_{s1}(x)+C_{11}(x)y+C_{12}(x)y^2 \tag{8}$$
$$0 \le x \le L_1$$

$$\phi_2(x,y)=\phi_{s2}(x)+C_{21}(x)y+C_{22}(x)y^2 \tag{9}$$
$$L_1 \le x \le L_1+L_2$$

The values of $C_{11}(x)$, $C_{12}(x)$, $C_{21}(x)$, and $C_{22}(x)$ are arbitrary constants which is obtained from the boundary conditions (3-5) and (6).

$$C_{11}(x)=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s_1}(x)-\psi_{g_1}}{t_{ox}} \tag{10}$$

$$C_{12}(x)=-\frac{1}{2t_{si}}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s_1}(x)-\psi_{g_1}}{t_{ox}} \tag{11}$$

$$C_{21}(x)=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s_2}(x)-\psi_{g_2}}{t_{ox}} \tag{12}$$

$$C_{22}(x)=-\frac{1}{2t_{si}}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s2}(x)-\psi_{g_2}}{t_{ox}} \tag{13}$$

Substituting the Eqs. (10-13) in (8) and (9), we get

$$\phi_1(x,y)=\phi_{s1}(x)+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s_1}(x)-\psi_{g_1}}{t_{ox}}y-\frac{1}{2t_{si}}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s_1}(x)-\psi_{g_1}}{t_{ox}}y^2 \tag{14}$$

$$\phi_2(x,y)=\phi_{s2}(x)+\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s_2}(x)-\psi_{g_2}}{t_{ox}}y-\frac{1}{2t_{si}}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s2}(x)-\psi_{g_2}}{t_{ox}}y^2 \tag{15}$$

Potential $\phi_{s_1}(x)$ and $\phi_{s_2}(x)$ under M_1 and M_2 can be obtained by solving the Poisson's Eq. (1) using (14) and (15).

$$\frac{d^2\phi_{s1}(x)}{dx^2}-\frac{2\varepsilon_{ox}}{\varepsilon_{si}\ t_{ox}t_{si}}\phi_{s1}(x)=-\frac{2\varepsilon_{ox}}{\varepsilon_{si}\ t_{ox}t_{si}}\psi_{g_1} \tag{16}$$

$$\frac{d^2\phi_{s2}(x)}{dx^2}-\frac{2\varepsilon_{ox}}{\varepsilon_{si}\ t_{ox}t_{si}}\phi_{s2}(x)=-\frac{2\varepsilon_{ox}}{\varepsilon_{si}\ t_{ox}t_{si}}\psi_{g_2} \tag{17}$$

By solving the second-order differential Eqs. (16) and (17), we get

$$\phi_{s1}(x)=Ae^{\lambda x}+Be^{-\lambda x}-\psi_{g_1} \tag{18}$$

$$\phi_{s2}(x)=Ce^{\lambda x}+De^{-\lambda x}-\psi_{g_2} \tag{19}$$

Where $\lambda=\sqrt{\frac{2\ \varepsilon_{ox}}{\varepsilon_{si}t_{ox}t_{si}}}$

χ is the electron affinity. λ is the characteristics length. This natural length is an easy guide for choosing device parameters.

The coefficients of A, B, C and D can be expressed as

$$A=\frac{[(V_{bi}-\psi_{g1})e^{\lambda(L_1-L_2)}]-[V_{bi}+V_{DS}-\psi_{g2}]+[(\psi_{g_1}-\psi_{g2})\cosh(\lambda L_2)]}{e^{\lambda(L_1-L_2)}-e^{\lambda(L_1+L_2)}}$$

$$B=\frac{[V_{bi1}+V_{ds}-\psi_{g2}]-[(V_{bi}-\psi_{g1})e^{\lambda(L_1+L_2)}]-[(\psi_{g1}-\psi_{g2})\cosh(\lambda L_2)]}{e^{\lambda(L_1-L_2)}-e^{\lambda(L_1+L_2)}}$$

$$C=Ae^{(\lambda L_1)}+\frac{\psi_{g_1}-\psi_{g_2}}{2} \tag{20}$$

$$D=Be^{-(\lambda L_1)}+\frac{\psi_{g_1}-\psi_{g_2}}{2}$$

2.2 Electric field

The electric-field distribution along the channel length can be obtained by differentiating the surface potential. The lateral electric field can be written as,

$$E_{x1}(x)=-\frac{d\phi_{s1}(x)}{dx}=-(A\lambda e^{\lambda x}-B\lambda e^{-\lambda x}) \tag{21}$$
$$0 \le x \le L_1$$

$$E_{x2}(x)=-\frac{d\phi_{s2}(x)}{dx}=-(C\lambda e^{\lambda x}-D\lambda e^{-\lambda x}) \tag{22}$$
$$L_1 \le x \le L_1+L_2$$

The vertical electric field can be written as

$$E_{y1}(x)=\frac{d\phi_{s1}(x,y)}{dy}=-C_{11}(x)-2yC_{12}(x) \tag{23}$$
$$0 \le x \le L_1$$

$$E_{y2}(x) = \frac{d\phi_{s2}(x,y)}{dy} = -C_{21}(x) - 2yC_{22}(x) \qquad (24)$$

$$L_1 \leq x \leq L_1 + L_2$$

2.3 Drain current

The flow of current I_{DS} in a DMDG TFET is based on Band-to-Band Tunneling (BTBT) of electrons from the valance band of the source to the conduction band of the channel region. The tunnelling generation rate (G) can be calculated using Kane's model. The total drain current is then computed by integrating the band to band generation rate over the volume of the device [19].

$$I_{DS} = q\iint G dx dy \qquad (25)$$

For the calculation of tunnelling Generation rate (G), Kane's Model has been employed [23], [24].

$$G(E) = A\frac{|E|^2}{\sqrt{E_g}} e^{\left[-B\frac{E_g^{3/2}}{|E|}\right]} \qquad (26)$$

Where, $|E|$ is the magnitude of the electric field which is defined as $|E| = \sqrt{E_x^{\,2} + E_y^{\,2}}$ and E_g is the energy band gap. The parameters used for TCAD simulation are A= $8.1\times10^{17} eV^{1/2}/cm.s.V^2$ and B= $3.057\times10^7 V/cm\text{-}(eV)^{3/2}$.

3. Result and Discussion

To verify the accuracy of the analytical model, two-dimensional device simulation has been performed by using TCAD Sentaurus [25]. The models available in TCAD to simulate band-to-band tunnelling are Kane's Band-to-Band model, Hurkx's Band-to-Band model, Schenk's Band-to-Band model and the dynamic Non Local Band-to-Band model. In our work the Kane's model is used to evaluate the band-to-band generation rate [24]. The proposed analytical model, results have been compared with simulation results. Fig. 2 shows the calculated surface potential profile for different gate voltages of the DMG TFET structure along with the simulated potential profile. As the gate voltage increases, the potential in the lightly doped region increases. There is a step-change of potential along the channel at the interface of Metal1 and Metal2. It is clearly seen from the figure that due to the presence of gate bias, there is a momentous change in the potential under the gate metal 1. As a result, the gate bias has high influence on tunnelling current at source side.

Fig. 3 shows the Variation of potential with the Channel position for different combination of gate length L_1 and L_2 of Metal 1 and Metal 2, respectively. The peak electric potential shifts towards the source side, when the gate

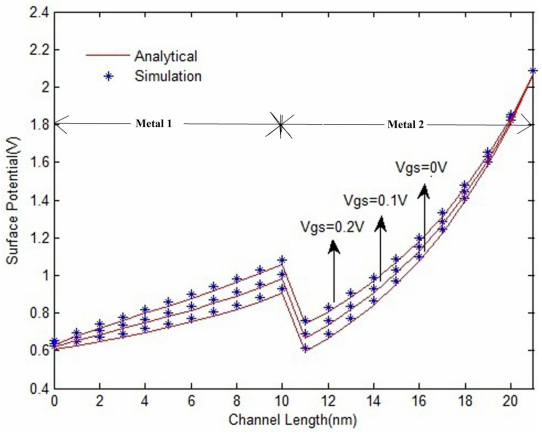

Fig. 2. Surface potential profiles of DMDG-TFET for Channel length L=20nm and V_{DS}=0.1V with different gate biases.

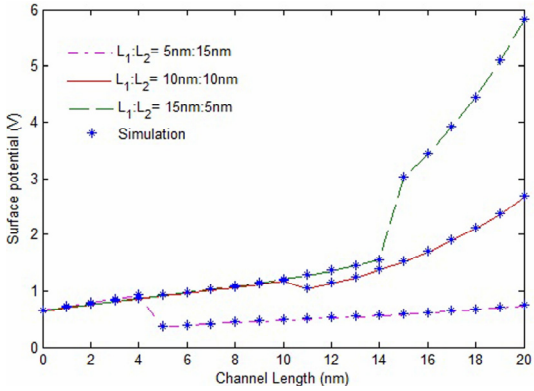

Fig. 3. Variation of surface potential for different combination of gate length L_1 and L_2 of Metal1and Metal 2 respectively.

length L_1 of Metal1is reduced. The electric field in the channel is more uniform due to this peak electric potential, as a result the device operates with higher carrier drift velocity. Analytical results are in excellent agreement with TCAD results.

Fig. 4 shows the calculated surface potential profile for different drain voltages of the DMG TFET structure along with the simulated potential profile. As the drain voltage increases, the potential in the region under metal2 increases. But the simulations show no significant changes in potential under Metal1. Hence we can conclude that Metal1 is screened from the effect of drain voltage. This means that the drain potential has very little effect on the tunnelling region at source side.

Fig. 5 shows the variation of vertical electric field distribution with the channel position for different values of the gate voltage. It is evident from the figure that peak of the vertical electric field appears near the tunnelling junction. ie., region under metal 1, resulting in a increased tunnelling current. The electric field near the drain decreases with the change in the work function. ie., region

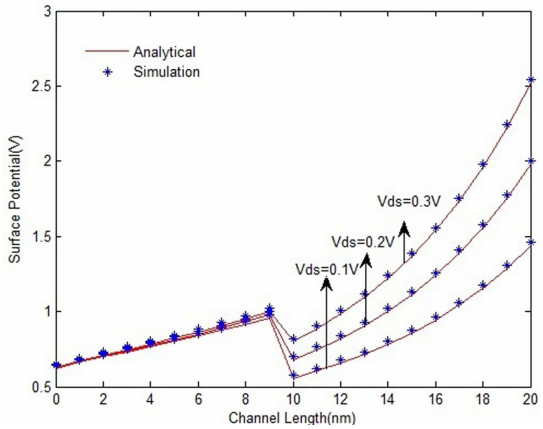

Fig. 4. Surface potential profiles of DMDG-TFET for channel length L=20nm and V_{GS}=0.1V with different drain voltages

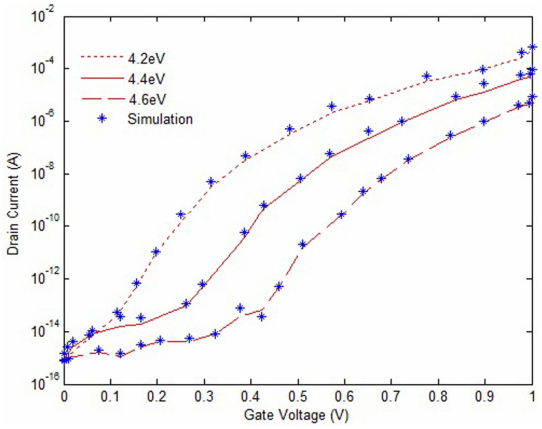

Fig. 6. I_D-V_{GS} characteristics of DMDG-TFET for various gate metal work functions ϕ_{M1} keeping ϕ_{M2} fixed at 4.4eV.

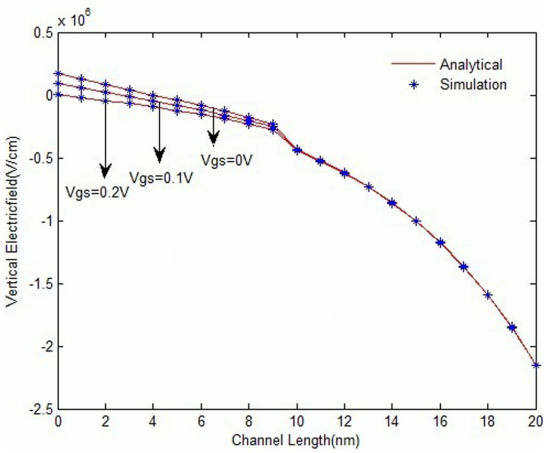

Fig. 5. Vertical electric field of DMDG-TFET for Channel length L=20nm and V_{DS}=0.1V with different gate biases.

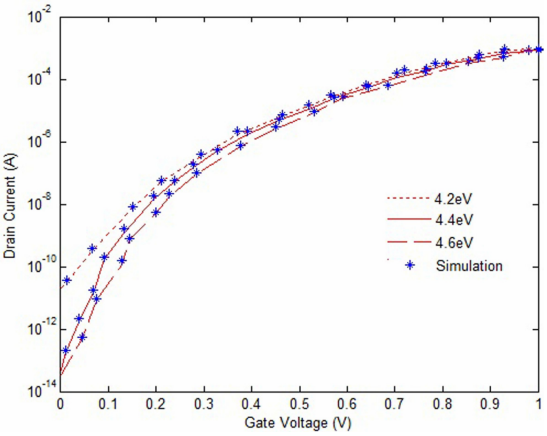

Fig. 7. I_D-V_{GS} characteristics of DMDG-TFET for various gate metal work functions ϕ_{M2} keeping ϕ_{M1} fixed at 4eV.

under metal 2. Thus the simulation results prove the validity of the model proposed.

Fig.6 shows the I_D-V_{GS} characteristics of DMDG-TFET for various gate metal work functions (ϕ_{M1}). The work function of metal M_2 (ϕ_{M2}) is kept fixed at 4.4 eV. As the work function of metal ϕ_{M1} decreases at source side leads to increase in tunnelling current significantly.

Fig.7 shows the I_D-V_{GS} characteristics of DMDG-TFET for various gate metal work functions (ϕ_{M2}) at drain side. The work function of metal M_1 (ϕ_{M1}) at source side is kept fixed at 4 eV. It is evident from the figure that the increase in work function of metal M_2 at drain side does not affected the tunnelling current significantly. Analytical results are in excellent agreement with TCAD results. Also from fig.6 and fig.7, the OFF state current of the DMDG TFET is in the range of 10^{-13}A-10^{-15}A , which shows that the leakage current, one of the Short channel effect is greatly reduced.

The Comparative drain current analyses of Single gate Silicon on insulator (SOI) TFET [9] and DMDG TFET are

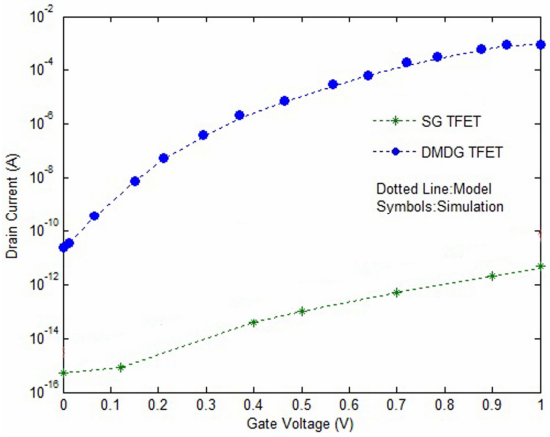

Fig. 8. Comparisons of current-voltage characteristics of DMDG-TFET and SG SOI TFET

shown in Fig. 8. This shows that the DMDG TFET shows better performance by enhancing I_{ON} current than the SG SOI TFET.

4. Conclusion

In this paper the analytical model for DMDG-TFET structure is proposed. The analytical model is based on two-dimensional Poisson's equation solved using parabolic approximation. The analytical expressions of surface potential, lateral electric field and vertical electric field are derived. In this model, components of lateral electric field and vertical electric field can also be used to calculate the distribution of tunnelling generation rate analytically and hence numerical extraction of tunnelling current becomes an easier task. Based on the generation rate and electric fields, the I_{DS}–V_{GS} characteristics of the device are also derived. From the presented results, it can be concluded that the DMDG structure shows better I_{ON} current than the SG SOI TFET.

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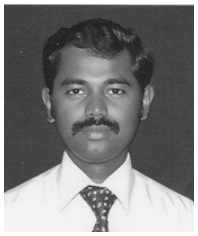

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