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Advanced Cascade Multilevel Converter with Reduction in Number of Components

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Abstract – In this paper a novel converter structure based on cascade converter family is presented. The suggested multilevel advanced cascade converter has benefits such as reduction in number of switches and power losses. Comparison depict that proposed topology has the least number of IGBTs among all multilevel cascade type converters which have been introduced recently. This characteristic causes low cost and small installation area for suggested converter. The number of on state switches in current path is less than conventional topologies and so the output voltage drop and power losses are decreased. Symmetric and asymmetric modes are analyzed and compared with conventional multilevel cascade converter. Simulation and experimental results are presented to illustrate validity, good performance and effectiveness of the proposed configuration. The suggested converter can be applied in medium/high voltage and PV applications.

Keywords: Multilevel converters, Reduced number of components, Cascaded multilevel converter, Symmetric and asymmetric topology

1. Introduction

Multilevel voltage-source converters provide a cost effective solution in the low and medium-voltage energy management market [1]. The term multilevel was introduced with the three level converters [2]. A multilevel converter is a power electronic system that produces a desired output voltage via several levels of dc voltages as inputs. With increasing the number of dc voltage sources, the converter output voltage waveform yields nearly sinusoidal waveform while using a fundamental frequency-switching scheme. As the number of levels increases, these advantages will be enhanced. This characteristic results in high-power-quality waveforms with lower distortion and a low blocking voltage for switching devices. However, it can impose more cost due to increase the circuit complexity and number of components and so the efficiency and reliability of multilevel converter is decreased. These are the main drawbacks of multilevel converters. Three main types of commercial topologies of multilevel voltage-source converters are: neutral point clamped (NPC) or diode clamped [2], cascaded H-bridge (CHB) [3], and flying capacitors (FCs) [4].

Among these converter topologies, the higher output voltage and power rating (13.8 kV, 30 MVA) are related to cascaded multilevel converter and its modular topology causes the higher reliability. The major disadvantages associated with the multilevel configurations are their circuit complexity, requiring the high number of power switches and the great number of auxiliary dc voltages which provided either by independent supplies or, more commonly, by a bulky array of capacitive voltage splitters. In this case, balancing the dc voltages is another factor that makes modulator circuit more complex [5]. A lot of efforts in literatures have been done to reduce the number of power switches and dc sources in several new topologies of multilevel cascade converters. The first introduced topology was the series H-bridge design [6], but several configurations have been obtained for this topology as well [7-8]. Several combinational designs have also been developed by cascading the fundamental topologies [9-10]. These designs can improve power quality for a given number of semiconductor devices than the fundamental topologies alone due to a multiplying effect of the number of levels. In [11-12] new configurations have also been proposed in which the number of separate dc sources have been diminished for high-voltage, high-power applications. A new cascaded multilevel converter called Zigzag converter is presented in [13]. Multiple outputs in this novel converter are produced only by one dc source. The dc voltage of each cascaded cell can be balanced without special control, and independent of load type. In this paper a novel symmetric and asymmetric multilevel modular cascade converter is proposed. Number of switches and on-state IGBTs is reduced in suggested advanced-cascade converter. The proposed configuration is discussed in both symmetric and asymmetric form. Then comparison is done between suggested multilevel converter and conventional one that presents advantages of this topology. Eventually

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simulation results and a prototype implementation of proposed multilevel converter are presented to show affectivity of new topology.

2. Cascade Multilevel Converter

A series connection of multiple single-phase converters creates cascaded multilevel converter. Each converter consists of a dc voltage source and four power switches that can produce three levels of voltage on its terminals. Three voltage steps refer to positive and negative values and zero level in each basic converter. Desired staircase voltage waveform is generated by composing appropriate dc voltage sources. This construction has capability to acquire medium output voltage levels utilizing only standard low-voltage components. This decreases the switching losses and voltage stress on power electronic devices, also the output voltage has small voltage steps, which results in high power quality, low harmonic components and better electromagnetic compatibility. A high modularity capability is main property of these converters because each converter can be seen as a module with similar circuit topology, control structure, and modulation. The cascaded H-bridge (CHB) topologies are suitable solution for high voltage applications due to the modularity and the simplicity of control. But, in these topologies, a great number of separated DC voltage sources are required to supply each conversion cell. Fig. 1 (a) depicts a cascaded H-bridge structure with n DC voltages sources which can produce 2n+1 output voltage levels in symmetric mode. In symmetric position for n dc voltage sources we have $V_1=V_2=\ldots=V_n=V_{dc}$.

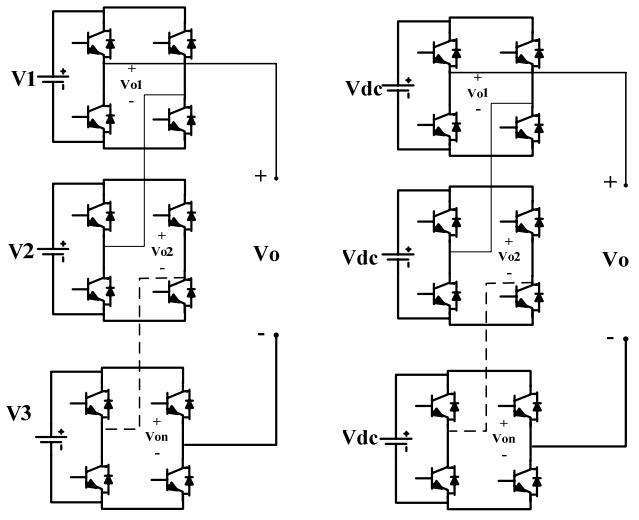


Fig. 1. Multilevel cascade H-Bridge converter: (a) Symmetric converter; (b) Asymmetric converter

3. Proposed Topology

3.1 Fundamental unit of suggested converter

As seen from Fig. 2 basic unit consist of two dc voltage sources and four semiconductor unidirectional switches or IGBTs. When number of dc sources is equal in conventional and proposed converter, it is found out that number of IGBTs here is half of that one in H-Bridge. Therefore each dc source devotes two IGBTs to itself.

In asymmetric CHB converter more output voltage levels are generated compared to the symmetric mode by same number of dc voltage sources.

Each basic unit is able to generate all voltage levels, zero, V and 2V. It is noteworthy that each basic module with two DC voltage sources and 4 switches beside a surrounding H-bridge produces five levels (positive and negative levels and regarding zero level) so the proposed topology with more than three DC voltage sources (two dc sources inside first module and a single voltage source) can generate more output levels with less switches because H-bridge is common for all the modules. Switching states are given in Table 1 for proposed symmetric basic unit. To avoid short circuit across dc voltage sources in the basic unit S_{11} and S_{13} should operate in complementary mode with S_{12} and S_{14} respectively.

Fundamental asymmetric unit of recommended converter is achieved with partial rearrangement in symmetric topology which is presented in Fig. 3. These changes entail adding an IGBT S_{11} at left side of symmetric structure and exchanging of central IGBT with one bidirectional switch as seen in Fig. 3. In this basic module S_{13} is added to avoid turning on diode of S_{14} when S_{11} is on. This prevents short

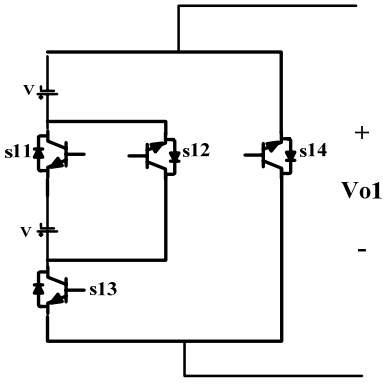


Fig. 2. Basic cell of proposed topology for symmetric mode

Table 1. Switching states of basic symmetric proposed topology

S. No	Switching state				V_o
	S_{11}	S_{12}	S_{13}	S_{14}	
1	1	0	1	0	+2V
2	0	1	1	0	+V
3	0	1	0	1	0

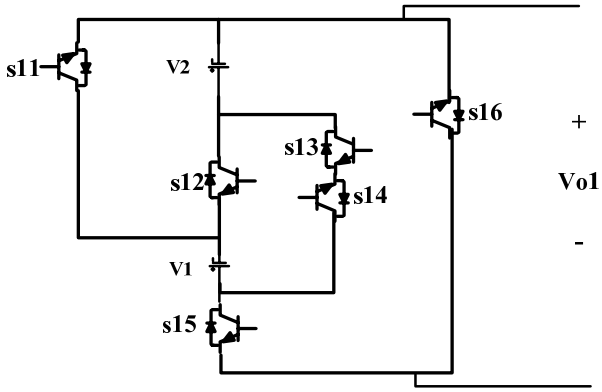


Fig. 3. Basic proposed topology for asymmetric mode

Table 2. Switching states of basic asymmetric proposed topology

S. No	Switching state						V_o
	S_{11}	S_{12}	S_{13}		S_{15}	S_{16}	
1	0	1	1	0	1	0	$+3V$
	0	0	1	1	1	0	$+2V$
3	1	0	0	1	1	0	$+V$
4	1	0	0	1	0	1	0
5	0	1	1	0	0	1	0

circuit across dc voltage sources V_{11} and V_{21} in the Fig. 3.

Switching states have been obtained in Table 2 for asymmetric unit shown in Fig. 3. If dc voltage sources are selected as binary mode, the basic unit will be able to generate four positive levels considering zero level. It is assumed V_1=1V and V_2= 2V in this table.

As seen from Table 2 to avoid short circuit across DC voltage sources in the basic unit S_{11}, S_{12} and S_{15} should operate in complementary mode with S_{13}, S_{14} and S_{16} respectively. Furthermore S_{11} and S_{12} should not be turned on simultaneously. For example if S_{12} and S_{13} are turned on, S_{14} should not turn on; otherwise V_{11} will be shorted circuit. S_{13} and S_{14} operate like a bidirectional switch.

3.2 Suggested configuration

Novel suggested configuration for multilevel cascade converter called advanced cascade (AC) converter in symmetric form is shown in Fig. 4. In this method, all of the dc voltage sources in each unit are identical.

$$V_j = V;\ j = 1, 2, \dots n \tag{1}$$

Where V is amplitude of each dc voltage sources and n is number of dc power supplies. It is noteworthy that n should be odd. In the symmetric case a single DC voltage source is used in the top of all modules to produce more output level without need of two excessive IGBTs. This figure represents connection of n-1 fundamental units and an innovative H-bridge encompassed bulk of novel cascade topology. In this structure, role of H-bridge is to reverse the

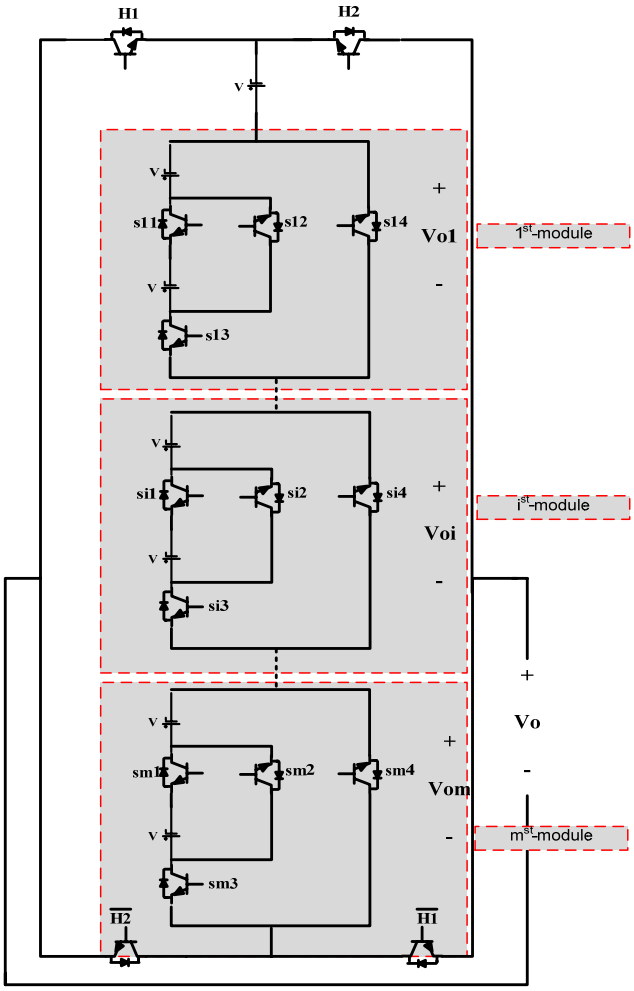


Fig. 4. Proposed symmetric multilevel advanced cascade converter

positive output voltage levels in second half cycle of voltage waveform.

Although several dc sources are required in this configuration, in some applications renewable energy sources could be used, such as photovoltaic panels or fuel cells, or with energy storage devices, such as capacitors or batteries. If ac voltage is already available, multiple dc power supplies can be produced via the isolated transformers and rectifiers. The overall output voltage of the proposed cascaded multilevel converter is the sum of output voltages of the m basic units, as follows:

$$V_O = \pm(v_{o1} + v_{o2} + \cdots + v_{om}) \tag{2}$$

Where for ith basic unit

$$V_{oi} = \begin{cases} 2v & \text{if } S_{i1} = 1 \text{ and } S_{i3} = 1 \\ v & \text{if } S_{i2} = 1 \text{ and } S_{i3} = 1 \\ 0 & \text{if } S_{i4} = 1 \end{cases} \tag{3}$$

For achieving more output voltage steps with the same

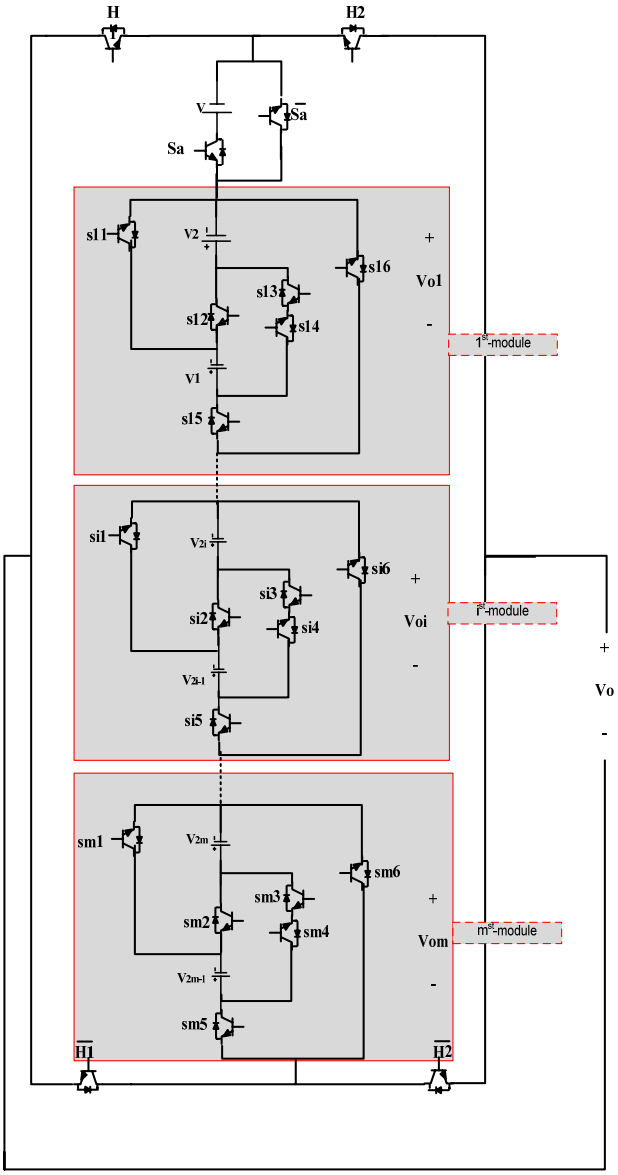


Fig. 5. Proposed asymmetric multilevel advanced cascade converter

number of dc voltages sources that used in symmetric multilevel converter, asymmetric form is introduced. Fig. 5 shows the proposed asymmetric multilevel converter. In asymmetric multilevel converter with n dc power supplies, values of dc voltage sources are defined as bellow:

$$V_k = p^{k-1} \tag{4}$$

Where k=1,2…n, and p is integer number that represents asymmetric factor and V is the smallest dc voltage source in the top of all modules (single DC voltage source). As the matter of the fact DC voltage sources which are used in Fig. 5 are selected by (4) in a sequence.

Here some partial changes have been implied to asymmetric recommended topology. As well as adding two IGBTs in each basic unit which is mentioned before, two IGBTs are joined to alone dc voltage source. To increase the number of output levels in proposed asymmetric topology, one DC source with two IGBTs are added. Two IGBTs is added to the single DC voltage source in the top of all modules (V) to create paths for selecting or eliminating this DC source in order to generate desired step in output voltage. Also in the i-th module (as seen in Fig. 5) Si1 is added to create path for contributing the V2i-1 lonely in the output voltage waveform. Adding this IGBT necessitate adding Si3 beside Si4 to prevent short circuiting the DC sources in this module.

By combinations of switching states of each unit, the various output voltage levels can be obtained. If suitable values for the dc voltage sources are chosen, then the output voltage of the converter can be produced between $-(\sum_{i=1}^{n-1} v_{oi} + v)$ and $+(\sum_{i=1}^{n-1} v_{oi} + v)$, where v_{oi} is determined as bellow:

$$v_{oi(max)} = v_{2i-1} + v_{2i} \tag{5}$$

4. Comparison Study

4.1 Number and rating of devices

The purpose of this section is comparison of imperative quantities between suggested multilevel converter and traditional multilevel converter with the same dc power supplies in the both magnitudes and number. Table 3 and 4 show comparison results between proposed advanced multilevel cascade converter and conventional multilevel cascade converter. It should be noticed in Tables 3 and 4 number of output levels includes positive and negative as well as zero levels. Number of dc voltage sources is equal to n and each unit is consisted of two dc voltage source. It is noteworthy that n should be odd.

In the asymmetric form of basic unit shown in Fig. 3 the PIV is calculated as follows:

$$PIV_1 = 2V_1 + 4V_2 \tag{6}$$

In same way for asymmetric form of ith basic unit PIV

Table 3. Comparison of proposed advanced cascade multilevel converter in symmetric and asymmetric modes

Proposed	Symmetric	Asymmetric
No. of DC sources	n	n
No. of switches	2n+2	3n+3
No. of output levels	2n+1	$2 * \left(\frac{1-p^n}{1-p}\right) + 1$
Maximum voltage	n Vdc	$(\frac{1-p^n}{1-p}) * Vdc$
PIV	$(\frac{13}{2}n - \frac{5}{2}) * V_{dc}$	$\sum_{i=1}^{m} (2V_{2i-1} + 4V_{2i})$
No. of On-state switches	n-1	$(\frac{3}{2}n - \frac{1}{2})$

Table 4. Comparison of conventional multilevel cascade converter in symmetric and asymmetric modes

Traditional cascade	Symmetric	A Symmetric
No. of DC sources	n	N
No. of switches	4n	4n
No. of output levels	2n+1	$2*\left(\frac{1-p^n}{1-p}\right)+1$
Maximum voltage	n Vdc	$(\frac{1-p^n}{1-p})*$ Vdc
PIV	$4n*V_{dc}$	$4*(\frac{1-p^n}{1-p})*$ Vdc
No. of On-state switches	2n	2n

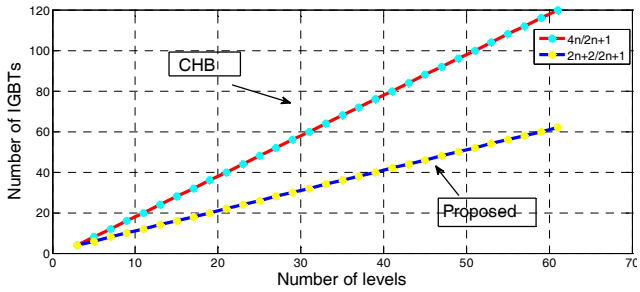


Fig. 6. Number of IGBTs versus number of levels for the symmetric topology

would be equal to:

$$\mathrm{PIV_i} = 2\mathrm{V_{2i-1}} + 4\mathrm{V_{2i}} \tag{7}$$

Therefore total PIV of asymmetric converter shown in Fig. 5 can be obtained as follows:

$$\mathrm{Tottal\ PIV} = \mathrm{PIV_1} + \cdots . \mathrm{PIV_i} + \cdots \mathrm{PIV_m} \tag{8}$$

Where, m is number of basic units.

It is noteworthy that n should be odd. Table 4 shows traditional multilevel cascade circuit information in both symmetric and asymmetric modes. It should be pointed out that in the comparison of proposed and conventional topology the number of DC voltage sources should be considered as equal. So for the single DC voltage source (V) used in the asymmetric proposed topology with two IGBTs, it is assumed an H-bridge is used in the conventional one includes a DC source.

Comparison between two tables illustrates number of IGBTs and on-state switches are almost half of that one in conventional configuration. Number of output voltage levels of multilevel cascade converter in symmetric and asymmetric mode is exactly same to that of suggested converter. This comparison approves advantages of the suggested configuration in this paper. As a matter of fact with less number of IGBTs, same output voltage steps could be generated in introduced topology compared to H-Bridge cascade multilevel converter.

Fig. 6 shows the number of IGBTs versus the number of voltage levels in proposed symmetric topology. As the figure shows, for any specific value of level, the proposed topology uses lower number of IGBTs in comparison with CHB. The figure clearly shows that the proposed topology uses less number of IGBTs.

4.2 Power losses calculation

Generally power electronic converters have two kinds of losses. The conduction losses are produced by equivalent resistance and the on-state voltage drop of the semiconductor devices. Non-ideal operation of switches creates the switching losses. Calculation of the losses of the proposed multilevel converter is discussed below.

A. Conduction losses

In order to calculate the conduction losses, firstly conduction losses of a typical power transistor and diode is calculated then they are extended to the multilevel converter. The instantaneous conduction losses of a transistor (p c, T (t)) and diode (p c, D (t)) can be expressed as follows:

$$P_{C,T}(t) = [V_T + {}_{RT} i^{\beta}(t)] i(t) \tag{9}$$

$$P_{C,D}(t) = [V_D + R_D\, i(t)] i(t) \tag{10}$$

Where, VT and VD are the on-state voltage of the transistor and diode, respectively. RT and RD are the equivalent resistance of the transistor and diode, respectively and β is a constant related to the characteristic of the transistor. Therefore, using (9) and (10), the average conduction power loss of the proposed sub-multilevel converter can be calculated as follows [14]:

$$P_C(t) = \frac{1}{\pi}\int_0^{\pi}\left[\begin{pmatrix} x(t)V_T + y(t)V_D + \\ x(t)R_T\, i^{\beta}(t) + y(t)R_D i(t) \end{pmatrix} i(t)\right] d\omega t \tag{11}$$

where, x(t) and y(t) are number of transistors and diodes in the current path in any instant of time respectively.

B. Switching losses

The switching losses are calculated for a typical switch and then the results are developed for the proposed multilevel converter. The total switching power losses consist of two components:

1. IGBT switching power loss
2. Anti-parallel diodes power losses

The following equations can be written:

$$P_{sw,T} = (E_{on,T} + E_{off,T}) f_{sw} \tag{12}$$

$$P_{sw,Anti-D} = (E_{on,Anti-D} + E_{off,Anti-D}) f_{sw} \approx E_{on,Anti-D} f_{sw}$$

Where,

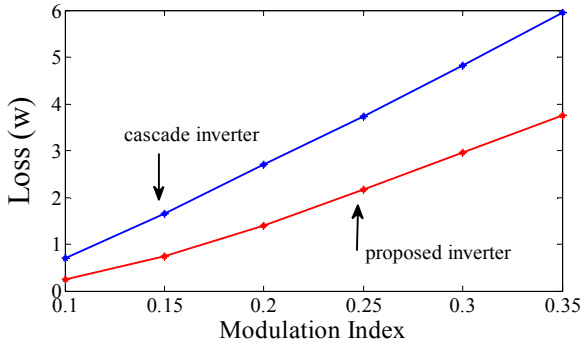


Fig. 7. Comparison of the power losses for the proposed and conventional structures

$P_{sw,T}$ is switching power losses of IGBT, $E_{on,T}$ is turn on energy losses in IGBT

$E_{off,T}$ is Turn off energy losses in IGBT and f_{sw} is switching frequency.

The index $Anti-D$ indicates the parameter related to the anti-parallel diodes. The switching losses depend on the number of switching transitions. Therefore, it depends on the modulation method. Finally total switching power losses of a fundamental block can be calculated as below:

$$P_{sw} = \sum_{1}^{i} P_{sw,T_i} + P_{sw,Anti-D_i} \tag{14}$$

Where i are depended on switching pattern that define the number of turned on IGBTs.

Using (11) and (14), the total losses of the fundamental multilevel converter will be as follows:

$$P_{loss} = P_{sw} + P_C \tag{15}$$

Comparison of the power losses for the 7-level symmetric proposed and conventional structures is depicted in Fig. 7. Calculation of losses is analyzed based on SPWM modulation approach. In this case the proposed configuration consist of a module includes two DC voltage sources and a single DC source is utilized. Here conventional structures consist of three H-bridges. Both cascaded and proposed converters are simulated using BUP406 IGBTs with the given data in [15] and 10v DC voltage sources values and load parameters of 30 ohm and 20 mH. As seen in this figure power loss of proposed topology is less than conventional one.

5. Simulation and Experimental Results

5.1 Simulation results

Fig. 8 shows the 11-level hybrid Advanced cascade (AC) converter in symmetric form which has two basic unit so

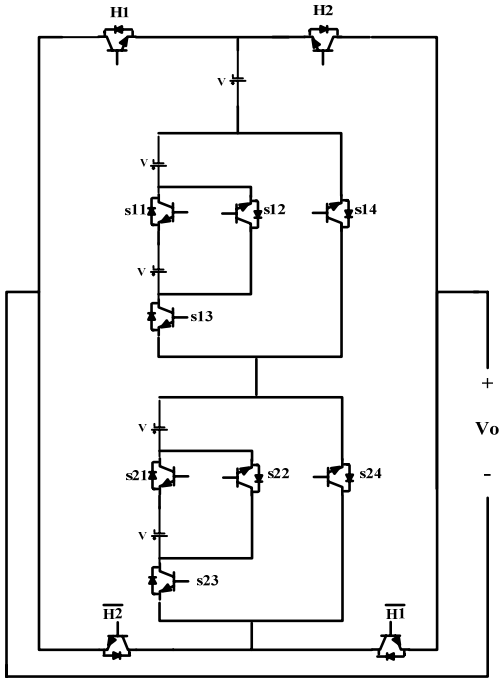


Fig. 8. The 11-level symmetric hybrid Advanced cascade

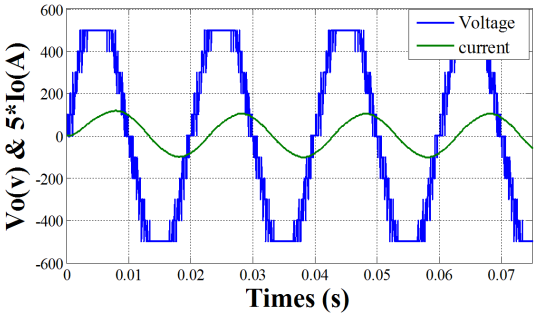
Table 5. Switching states of 11-level proposed topology in symmetric form

S. No	Switching state						Vo
	S_{11}	S_{21}	S_{13}	S_{23}	H_1	H_2	
1	1	1	1	1	1	0	$+5V_1$
2	1	1	1	0	1	0	$+4V_1$
3	1	1	0	0	1	0	$+3V_1$
4	1	0	0	0	1	0	$+2V_1$
5	0	0	0	0	1	0	$+V_1$
6	0	0	0	0	1	1	0
7	0	0	0	0	0	1	$-V_1$
8	1	0	0	0	0	1	$-2V_1$
9	1	1	0	0	0	1	$-3V_1$
10	1	1	1	0	0	1	$-4V_1$
11	1	1	1	1	0	1	$-5V_1$

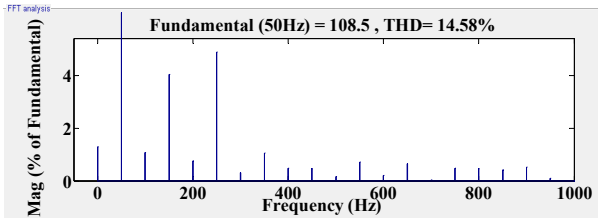
n=5 and number of IGBTs according to Table 1 are 2n+2 where yield 12 IGBTs. Switching states of 11-level proposed converter have been illustrated in Table 5 to make operational principle of AC multilevel converter much more comprehensible. The switch S is ON when its state is 1 and is OFF when its state is 0.

Figs. 9 and Fig 10 illustrate simulation results. It should be noticed that in symmetric and asymmetric proposed topologies two modules and one module as well as a single DC sources are implemented respectively. In presented simulation and experimental results the DC voltage sources are considered 100V. Therefore output voltage waveforms consist of 100 V steps in the simulation and experimental results. Dc voltage sources in asymmetric form for proposed configuration are selected according to a geometric progression with a factor of two. Fig. 9 (a) show simulation results of output voltage and current for 11-level

proposed symmetric topology under RL load. Fig. 9 (b) shows THD analysis and magnitudes of different harmonic components in output voltage waveform for proposed symmetric topology.

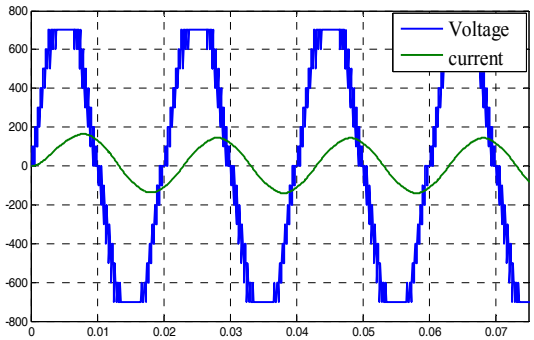


(a) Output voltage and current

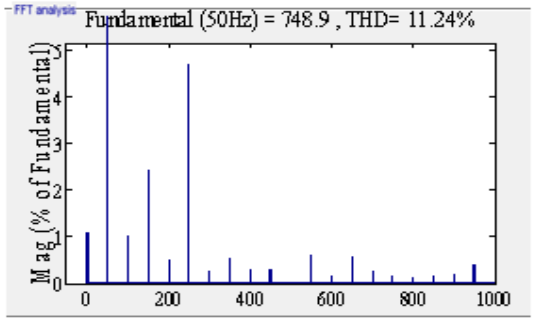


(b) THD and FFT analysis of output voltage

Fig. 9. Simulation results of 11-level proposed converter in symmetric mode



(a) Output voltage and current



(b) THD and FFT analysis of output voltage

Fig. 10. Simulation results of 15-level proposed converter in asymmetric mode

Fig. 10 (a) presents simulation result of 15-level asymmetric configuration (output voltage and current). Fig. 10 (b) shows THD analysis and magnitudes of different harmonic in output voltage waveform for proposed asymmetric topology. For this case, THDs of the output voltage based on simulations are 14.58% and 11.24% in suggested symmetric and asymmetric forms respectively.

As it can be seen in these waveforms, the output current has a low THD, meaning near sinusoidal waveform. To produce a desired output with high power quality, the number of voltage levels should be increased.

5.2 Experimental results

To evaluate the performance of the suggested multilevel converter, shown in Fig. 8, a single-phase 11-level prototype has been modeled and implemented. The Fig. 11 shows the implemented laboratory prototype photograph. The IGBTs used in the prototype are BUP406 with internal anti-parallel diodes and voltage and current ratings equal to 1200V and 20 A, respectively. The switching required pulses are produced by the DsPIC30F4011 microcontroller. The Hcpl316j is used as IGBT gate derives. In the implemented proposed symmetric multilevel converter the DC voltage sources are 100 V.

Figs. 12 and Fig. 13 illustrate experimental results. Amplitude of the smallest DC voltage source for the asymmetric proposed topology is 70 V in the experimental test so the output voltage waveform is obtained with 70 V steps. Figs. 12 (a) and (b) present experimental results of output voltage waveforms for 11-level proposed symmetric topology in no load and under RL load respectively.

Figs. 13 (a) and (b) depict experimental results of output voltage waveforms for 15-level proposed asymmetric topology in no load and under RL load respectively. Fig. 13 (c) shows the FFT analysis and magnitudes of different

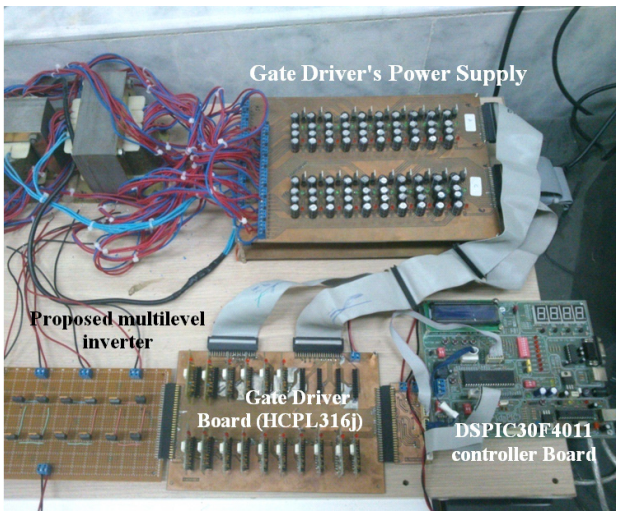
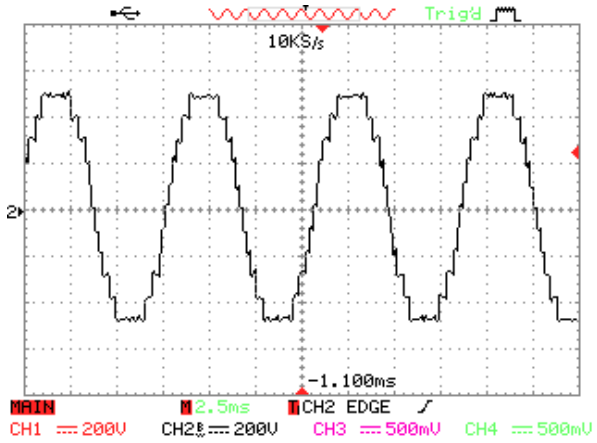
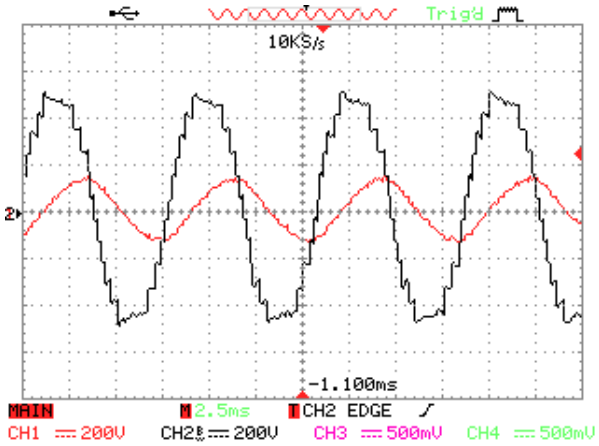


Fig. 11. The implemented laboratory prototype



(a) Output voltage in no load case



(b) Output voltage and current under load condition

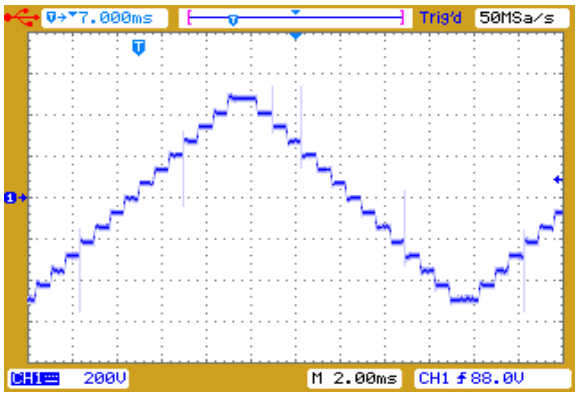
Fig. 12. Experimental results of 11-level proposed symmetric configuration

harmonic components of output voltage. As seen in this figure main harmonic is related to 50Hz which devotes the greatest magnitude to itself.

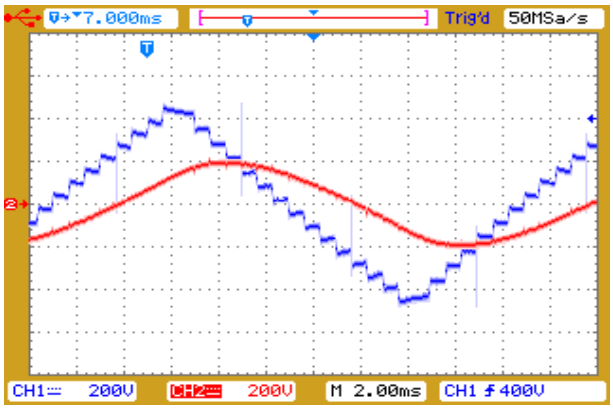
As seen in this figure the simulation and experimental results are match as saliently. Partial difference between the magnitudes of the simulation and experimental results is because of the voltage drops on switches in the prototype.

6. Conclusion

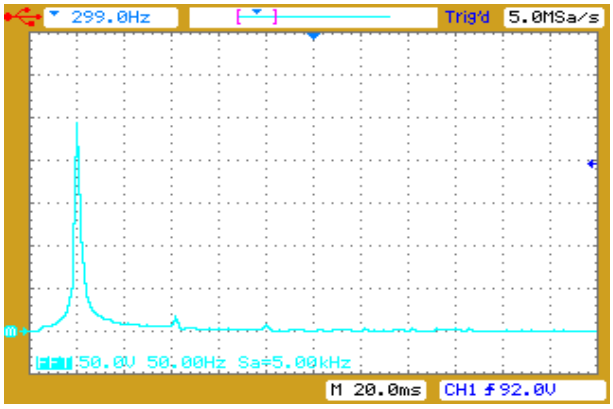
In this paper, a new converter topology has been proposed which has many superior features over conventional topologies. In the proposed topology less number of power switches is required compared to conventional converter. Furthermore suggested topology needs lower number of isolated dc voltage sources in comparison to conventional topologies. The number of on state switches in current path is less than conventional topologies. Therefore, the voltage drop in output voltage,



(a) Output voltage in no load case



(b) Output voltage and current under load condition



(c) FFT analysis for output voltage in asymmetric proposed topology

Fig. 13. Experimental results of 15-level asymmetric configuration

cost, and volume of proposed converter are low too. In the comparison part these advantages have been shown clearly. The experimental results of the developed prototype for an eleven-level converter of the proposed topology are demonstrated in this paper.

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