

# Surface Treatment of Ge Grown Epitaxially on Si by *Ex-Situ* Annealing for Optical Computing by Ge Technology

Xiaochi Chen<sup>1</sup>, Yijie Huo<sup>1</sup>, Seongjae Cho<sup>2</sup>, Byung-Gook Park<sup>3</sup>, and James S. Harris, Jr<sup>1</sup>

<sup>1</sup>Department of Electrical Engineering, Stanford University / Stanford, California 94305-2311, USA

<sup>2</sup>Department of Electronic Engineering, Gachon University / Seongnam-si, Gyeonggi-do 461-741, Republic of Korea

<sup>3</sup>Department of Electrical and Computer Engineering with Inter-university Semiconductor Research Center (ISRC), Seoul National University / Seoul 151-744, Republic of Korea bgpark@snu.ac.kr

\* Corresponding Author: Byung-Gook Park

Received January 15, 2014; Revised March 17, 2014; Accepted July 28, 2014; Published October 31, 2014

\* Extended from a Conference: Preliminary results of this paper were presented at the ISCE 2014. This present paper has been accepted by the editorial board through the regular reviewing process that confirms the original contribution.

**Abstract:** Ge is becoming an increasingly popular semiconductor material with high Si compatibility for on-chip optical interconnect technology. For a better manifestation of the meritorious material properties of Ge, its surface treatment should be performed satisfactorily before the electronic and photonic components are fabricated. *Ex-situ* rapid thermal annealing (RTA) processes with different gases were carried out to examine the effects of the annealing gases on the thin-film quality of Ge grown epitaxially on Si substrates. The Ge-on-Si samples were prepared in different structures using the same equipment, reduced-pressure chemical vapor deposition (RPCVD), and the samples annealed in N<sub>2</sub>, forming gas (FG), and O<sub>2</sub> were compared with the unannealed (deposited and only cleaned) samples to confirm the improvements in Ge quality. To evaluate the thin-film quality, room-temperature photoluminescence (PL) measurements were performed. Among the compared samples, the O<sub>2</sub>-annealed samples showed the strongest PL signals, regardless of the sample structures, which shows that *ex-situ* RTA in the O<sub>2</sub> environment would be an effective technique for the surface treatment of Ge in fabricating Ge devices for optical computing systems.

**Keywords:** Germanium, Si compatibility, Si photonics, On-chip optical interconnect, Epitaxial growth, Rapid thermal annealing, Ge-on-Si, Photoluminescence, Surface treatment

## 1. Introduction

Recently, Ge has attracted considerable interest owing to its pseudo-direct bandgap behavior, high carrier mobility and compatibility of Si processing technology [1]. These features of Ge make Si photonics more applicable to on-chip optical interconnects for the next-generation central processing unit by optical technology [2-4], which has been also highlighted in the most recent semiconductor technology roadmaps [5]. Fig. 1 presents a schematic diagram of an on-chip optical interconnect composed of both electronic and photonic components. The optical part includes not only the optical waveguide itself but also the light source, photodetector and modulator, because all the signal processing units that can be fabricated on a single Si

chip with conventional CMOS logic circuits [6]. In optical telecommunication technology, 1310-nm and 1550-nm wavelengths have been used in the locations, where the attenuation of the power delivered through a silica optical fiber is locally minimized, and the global minimum is observed at 1550 nm over the entire optical communication channel [7].

The fabrication of lasers operating at either 1310 nm or 1550 nm has been difficult because of the complexity in accurately making up the active materials, which include quaternary and quinary compound semiconductors, such as GaInNAs and GaInNAsSb [8-10]. On the other hand, owing to its pseudo-direct bandgap with a magnitude of 0.8 eV (energy bandgap at  $\mathbf{k} = 0$ ), Ge is capable of realizing light emission at 1550-nm as a single-atom material without necessitating complicated epitaxy

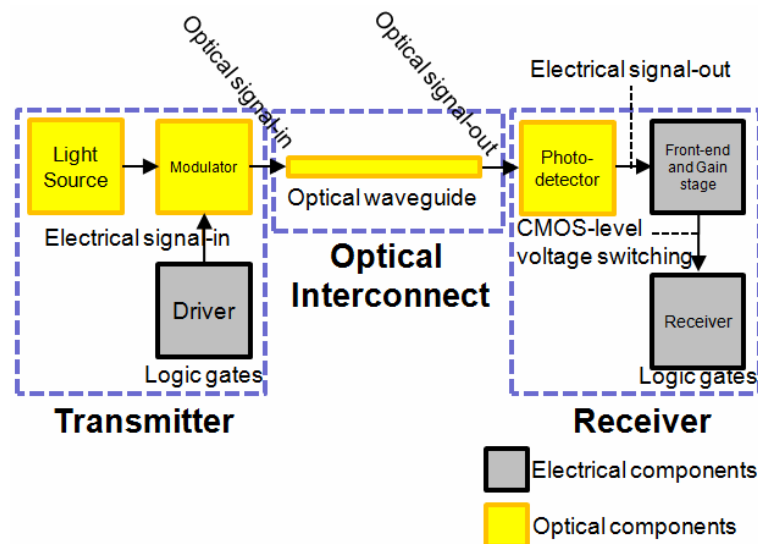


Fig. 1. Schematic diagram of the on-chip optical interconnect (the optical components are highlighted in yellow).

processing to adjust the atomic fractions accurately either in quaternary or quinary compound semiconductors. Therefore, Ge is considered as an optical material for active devices, such as laser and light-emitting diodes (LEDs) [11, 12]. Ge can also be adopted to other active and passive devices including modulators, optical waveguides and photodetectors owing to its higher refractive index ( $n_{\text{Ge}} = 4.0$ ) than Si ( $n_{\text{Si}} = 3.47$ ), optical confinement stronger than Si and higher electron and hole mobilities,  $3,900 \text{ cm}^2/\text{V}\cdot\text{s}$  and  $1,900 \text{ cm}^2/\text{V}\cdot\text{s}$ , respectively [6, 13-16]. In addition, Ge can form an alloy with Si relatively easy or be grown directly on Si starting from low-temperature epitaxy despite their large lattice mismatch (Si:  $5.431 \text{ \AA}$  and Ge:  $5.658 \text{ \AA}$ ) as confirmed by a part of this work. For these advantageous optical and electrical properties along with its outstanding Si compatibility, Ge is expected to play an essential role in the optical interconnects on Si chips.

Prior to device fabrication, Ge thin films grown epitaxially on Si substrates need to undergo a careful surface treatment to maximize its merits. In this study, the effect of *ex-situ* rapid thermal annealing (RTA) on the Ge surface quality was validated experimentally by photoluminescence (PL) spectroscopy at room temperature.

## 2. Experiments

To prepare the Ge samples and test the material quality of Ge grown epitaxially on Si substrates, a number of samples were grown using different precursors in a reduced-pressure chemical vapor deposition (RPCVD) system ( $\sim 5\text{-}100 \text{ Torr}$ ) by Applied Materials. Fig. 2(a)-(c) presents three samples with different structures. Sample 1 has a 200-nm thick intrinsic Ge layer grown directly on a Si substrate at  $405 \text{ }^\circ\text{C}$ , as shown in Fig. 2(a). After epitaxial growth, *in-situ*  $\text{H}_2$  annealing at  $850 \text{ }^\circ\text{C}$  was performed for 30 min. to recrystallize the Ge thin film. Sample 2 in Fig. 2(b) has a 200-nm-thick *n*-doped Ge layer grown on a 200-nm-thick *p*-doped SiGe buffer layer on a

Si substrate. The *p*-doped buffer layer was grown at  $405 \text{ }^\circ\text{C}$  followed by *in-situ*  $\text{H}_2$  annealing at  $850 \text{ }^\circ\text{C}$  for 30 min. The Ge content and doping concentration in the SiGe buffer layer was 88% and  $\sim 5 \times 10^{18} \text{ cm}^{-3}$ , respectively. The  $\text{SiH}_4$  and  $\text{GeH}_4$  gas flows were controlled precisely to obtain a  $\text{Si}_{0.12}\text{Ge}_{0.88}$  buffer layer. A 200-nm-thick *n*-doped Ge layer was then grown on top of the SiGe buffer layer at  $405 \text{ }^\circ\text{C}$  without a subsequent *in-situ* annealing process. The doping concentration in the Ge layer was *n*-type  $\sim 2 \times 10^{18} \text{ cm}^{-3}$ . Sample 3 in Fig. 2(c) had a 2- $\mu\text{m}$ -thick bulky intrinsic Ge layer grown on a Si substrate using a low-high temperature growth technique with cyclic *in-situ* annealing performed three times. To investigate the effects of different annealing gases on the material quality, *ex-situ* rapid thermal annealing (RTA) was performed with  $\text{N}_2$ , forming gas (FG), and  $\text{O}_2$  on each group of samples. Fig. 3 presents a scanning electron microscopy (SEM) image from the cross-section of Sample 1 with an intrinsic Ge layer grown directly on a Si substrate. The Ge surface is quite smooth because there are few hillocks and dislocations along the Ge/Si interface, which are projected substantially to the surface using a low-high temperature two-step growth technique.

Photoluminescence (PL) spectroscopy was performed to evaluate the quality of the Ge layer. A PL test is a basic and efficient characterization technique that can quickly measure the optical transitions within a material [17]. In the case of semiconductors, a PL test can determine the peak emission wavelength, emission spectrum and material quality in terms of the crystallinity for a device structure, all of which are parameters that can gauge the utility for a desired application of the structure. Fig. 4 presents the PL measurement setup used for the characterization of Ge grown epitaxially on a Si substrate. The photons are emitted out from a Nd:YAG green laser (pumped laser), which is connected to a laser controller and powered by a HP E3610 DC power supply. Most of the emitted photons have a wavelength of 532 nm (after frequency doubling) with a minority having a wavelength of 1064 nm (original wavelength). A fast calculation by  $E_G [\text{eV}] = 1.24/\lambda [\mu\text{m}]$

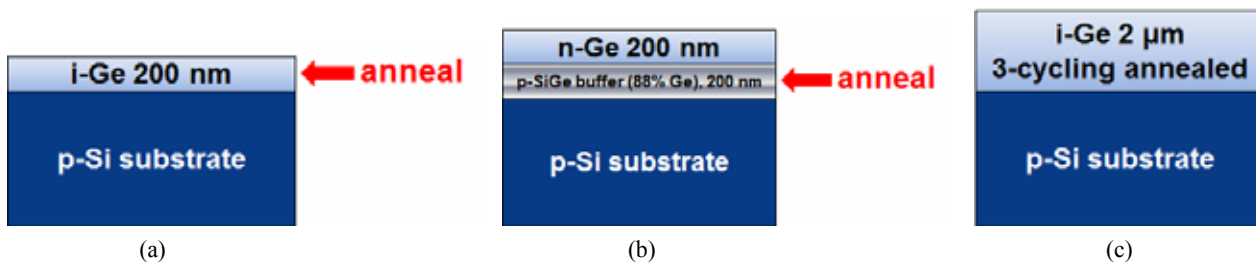


Fig. 2. Sample structures (a) Sample 1 with an intrinsic Ge layer, (b) Sample 2 with SiGe-buffered Ge layer, (c) Sample 3 with a thick Ge layer.

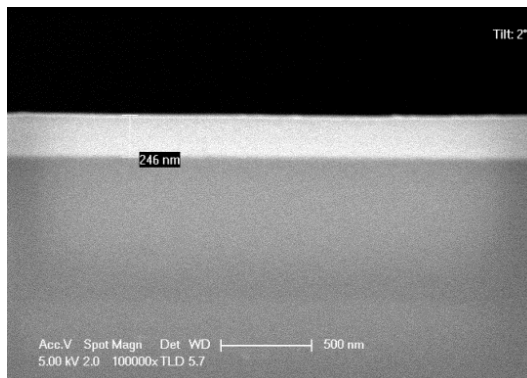


Fig. 3. SEM image of a cross-section of Sample 1.

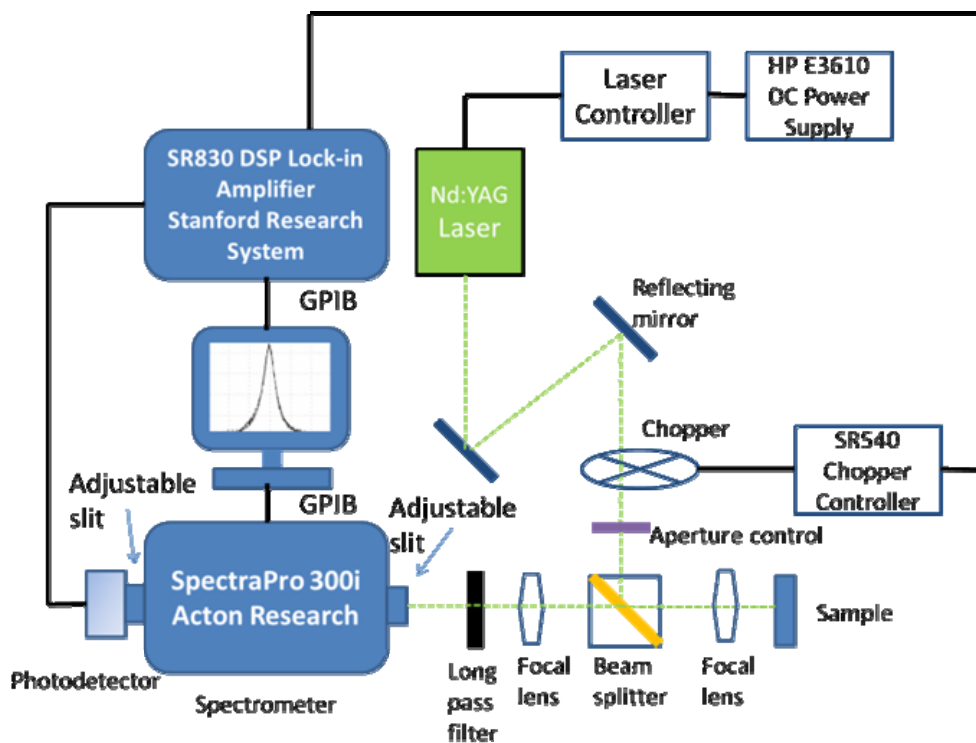


Fig. 4. Photoluminescence measurement setup.

( $E_G$ : bandgap energy) revealed the energy of photons (2.33 eV) emitted from the pumped laser, which is larger than the direct band-to-band transition energy of Ge (0.8 eV).

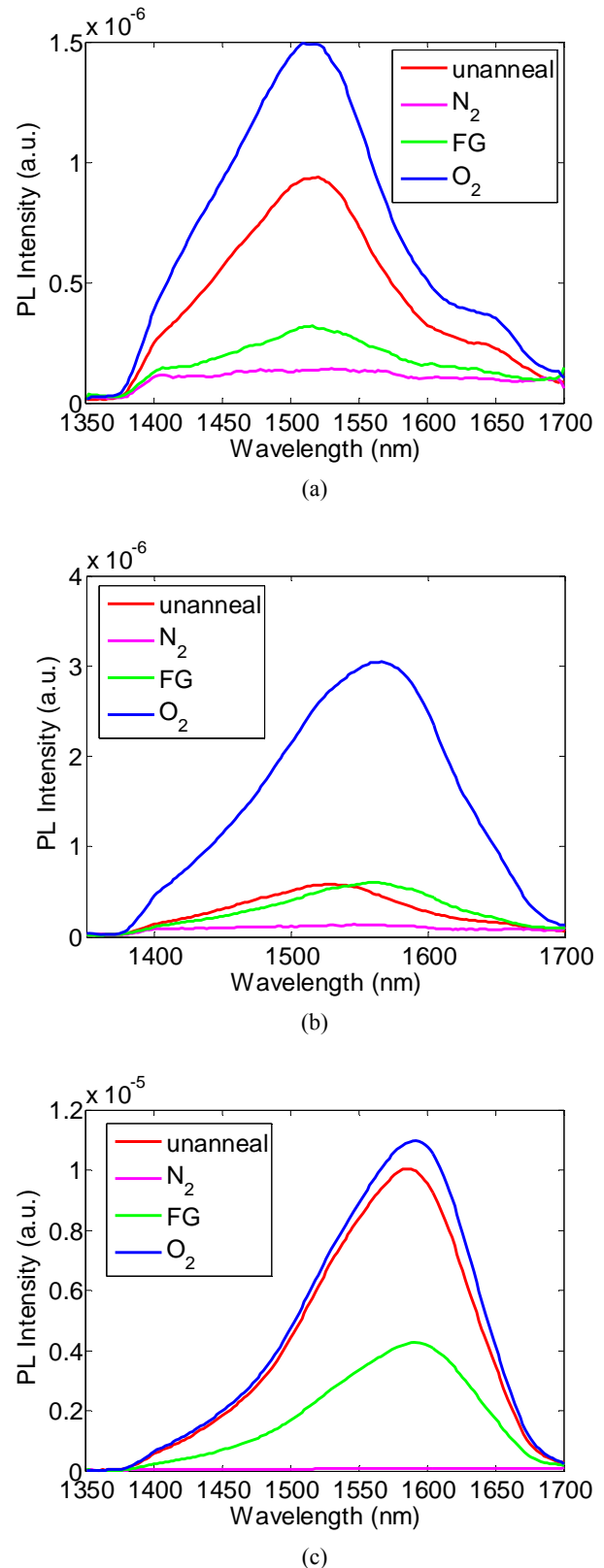
The green light beam is then directed by two reflecting mirrors and then passes a mechanical chopper through which the light is modulated. The purpose of this

modulation was to remove the extraneous noise and detect the desired PL signal. In more detail, the lock-in amplifier is a phase-sensitive instrument, which can take an input signal and extract the component of the signal that matches the frequency of the chopper. Therefore, the unmodulated signals, for example, room light, can be filtered out. After

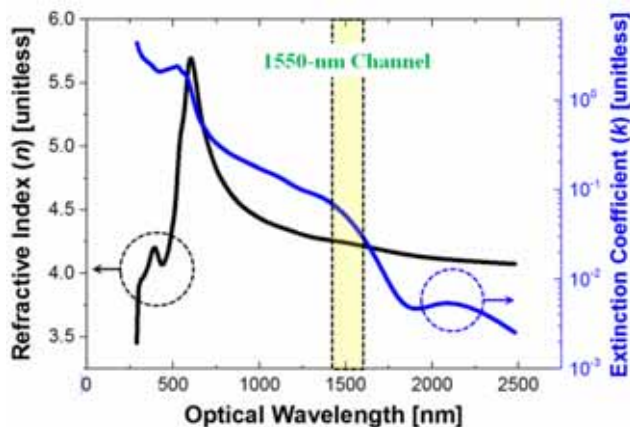
passing the chopper, light passes through a beam splitter and then hits on the surface of the tested sample. The light re-emitted from the tested sample is collimated by focal lenses and then coupled into the spectrometer. Inside the spectrometer, a chosen grating diffracts light and photons with a selected wavelength to an appropriate photodetector, which can transfer the optical signals into electrical signals. The electrical signals are sent to the lock-in amplifier and the output to the computer responsible for taking data, controlling the spectrometer, carrying out analyses, and plotting the relevant data.

### 3. Results and Discussion

Figs. 5(a)-(c) depicts the PL measurements of each sample annealed in different ambient gases. The PL peaks from the Ge layers annealed in a  $N_2$  atmosphere had the lowest values regardless of the sample structure. Those annealed in FG ( $N_2$  and 4%  $H_2$  mixture) exhibited the next lowest PL intensities. The peaks from these two types of samples were even lower than those from the unannealed samples because the Ge surface was passivated slightly during RTA processing. On the other hand, the samples annealed in an  $O_2$  atmosphere showed the strongest PL intensities compared to the unannealed samples. When the samples were annealed in an  $O_2$  environment, smooth Ge dioxide ( $GeO_2$ ) was formed on the Ge surface. On the other hand, high annealing temperature removed  $GeO_2$  with a smaller release of energy from the surface to the air. Therefore, Ge was etched and the surface became very smooth, which benefits stronger PL signals. On the other hand, this surface etching effect was not achieved by either  $N_2$  or FG annealing. Although there might be a decrease in the Ge thickness and the PL peak can be lowered, the volume effect should be negligible when compared with the peak increase because of an improvement in surface quality, which consequently shows that the  $O_2$ -annealed samples exhibit even stronger PL signals than those of the unannealed samples. Among the samples tested, Sample 2 showed more concentrated peaks around 1550 nm. Samples 1 and 3 showed blue- and red-shifted optical spectra, respectively, which suggests that the emission wavelength of the Ge epitaxy layer can be adjusted to 1550 nm by the SiGe buffer with an appropriate Ge fraction. With Sample 2, however, the PL peaks could move more readily unless the sample was not annealed in the  $O_2$  environment, whereas the other samples showed a rather constant wavelength where the PL peak were located. This was attributed to the absence of high-temperature finishing *in-situ* annealing 850 °C in the case of Sample 2, through which the necessity of *in-situ* annealing after low-temperature growth can be confirmed to secure higher predictability and stability of the center peak position. Fig. 6 presents the measured refractive index ( $n$ ) and extinction coefficient ( $k$ ) of Ge grown epitaxially by RPCVD as a function of the optical wavelength. The yellow-colored window contains a 1550-nm on-chip optical communication channel by Ge, where  $n$  was found to be  $n = 4.23$  at  $\lambda = 1550$  nm. Owing to the high  $k$  ( $k = 0.03$  at  $\lambda = 1550$  nm), a precise adjustment of the Ge fraction in the



**Fig. 5.** PL measurement results from (a) Sample 1, (b) Sample 2, (c) Sample 3, with  $N_2$ , FG, and  $O_2$  annealing gases (red: unannealed sample, pink:  $N_2$ , green: FG, and blue:  $O_2$ ).



**Fig. 6. Measured  $n$  and  $k$  as a function of the optical wavelength. The yellow-colored window contains a 1550-nm on-chip optical communication channel by Ge.**

SiGe waveguide needs to be performed for less optical loss [15]. Although several Ge surface finishing methods based on wet etching and plasma techniques have been reported [18, 19], the emphases have been placed only on applications in electronic devices, and the capacitance vs. voltage (C-V) curves are the main indices in those cases without studies of the changes in the optical properties of the Ge surface. On the other hand, RTA processing would be a faster, more reproducible and more cost-effective solution for a Ge surface treatment. In addition, comparative PL studies would be a guideline for related research on Ge-incorporated Si optical engineering.

#### 4. Conclusion

In this study, a processing technique for improving the quality of Ge grown epitaxially on a Si substrate was exploited. An *ex-situ* RTA process with  $O_2$  flow has a practical effect of enhancing the PL signal intensity of Ge. The surface treatment of Ge should be performed in advance of fabricating Ge electronic and optical devices to reduce the surface recombination leakage, minimize the optical loss, and 1550-nm operation ability. RTA in an  $O_2$  environment developed in this work is a feasible and fast surface treatment technique for integrated Ge technology toward the next-generation optical computing systems.

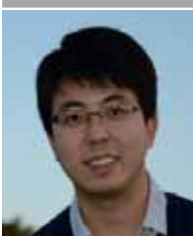
#### Acknowledgement

This study was supported by the Center for Integrated Smart Sensors funded by the Korean Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2012M3A6A6054186) and in part by the National Research Foundation of Korea (NRF) funded by the Korean Ministry of Science, ICT & Future Planning (NRF-2014R1A1A1003644).

#### References

- [1] C. Claeys and E. Simoen, *Germanium-Based Technologies: From Materials to Devices*, Elsevier (Oxford, UK), 2007. [Article \(CrossRef Link\)](#)
- [2] J. W. Goodman, F. I. Leonberger, S.-Y. Kung, and R. A. Athale, "Optical Interconnections for VLSI Systems," *Proceedings of the IEEE*, Vol. 72, No. 7, pp. 850–866, Jul. 1984. [Article \(CrossRef Link\)](#)
- [3] D. A. B. Miller, "Rationale and Challenge for Optical Interconnects to Electronic Chips," *Proceedings of the IEEE*, Vol. 88, No. 6, pp. 728–749, Jun. 2000. [Article \(CrossRef Link\)](#)
- [4] D. A. B. Miller, "Device Requirements for Optical Interconnects to Silicon Chips," *Proceedings of the IEEE*, Vol. 97, No. 7, Jul. 2009. [Article \(CrossRef Link\)](#)
- [5] International Technology Roadmap for Semiconductors (ITRS) 2013 Edition. [Article \(CrossRef Link\)](#)
- [6] D. A. B. Miller, "Optics for low-energy communication inside digital processors: quantum detectors, sources, and modulators as efficient impedance converters," *Optics Letters*, Vol. 14, No. 2, pp. 146–148, Jan. 1989. [Article \(CrossRef Link\)](#)
- [7] M. Gilmore, *Fibre Optic Cabling: Theory, design and installation practice*, Butterworth-Heinemann Ltd. (Oxford, UK), 1991. [Article \(CrossRef Link\)](#)
- [8] H. Zhao, A. Haglund, P. Westburgh, S. M. Wang, J. S. Gustavsson, M. Sadeghi, and A. Larsson, "1310 nm GaInNAs triple quantum well laser with 13 GHz modulation bandwidth," *Electronics Letters*, Vol. 45, No. 7, pp. 356–357, Mar. 2009. [Article \(CrossRef Link\)](#)
- [9] S. Bank, W. Ha, V. Gambin, M. Wistey, H. Yuen, L. Goddard, S. Kim, and J. S. Harris Jr., "1.5  $\mu\text{m}$  GaInNAs(Sb) lasers grown on GaAs by MBE," *Journal of Crystal Growth*, Vol. 251, No. 1–4, pp. 367–371, Apr. 2003. [Article \(CrossRef Link\)](#)
- [10] R. K. Schaevitz et al., "Simple Electroabsorption Calculator for Designing 1310 nm and 1550 nm Modulators Using Germanium Quantum Wells," *IEEE Journal of Quantum Electronics*, Vol. 48, No. 2, pp. 187–197, Feb. 2012. [Article \(CrossRef Link\)](#)
- [11] R. E. Camacho-Aguilera et al., "An electrically pumped germanium laser," *Optics Express*, Vol. 20, No. 10, pp. 11316–11320, May 2012. [Article \(CrossRef Link\)](#)
- [12] S. Cho, B.-G. Park, C. Yang, S. Cheung, E. Yoon, T. I. Kamins, S. J. B. Yoo, and J. S. Harris, Jr., "Room-temperature electroluminescence from germanium in an  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{Ge}$  heterojunction light-emitting diode by  $\Gamma$ -valley transport," *Optics Express*, Vol. 20, No. 14, pp. 14921–14927, Jul. 2012. [Article \(CrossRef Link\)](#)
- [13] E. H. Edwards, L. Lever, E. T. Fei, T. I. Kamins, Z. Ikonik, J. S. Harris, R. W. Kelsall, and D. A. B. Miller, "Low-voltage broad-band electroabsorption from thin Ge/SiGe quantum wells epitaxially grown on silicon," *Optics Express*, Vol. 21, No. 1, pp. 867–876, Jan. 2013. [Article \(CrossRef Link\)](#)

- [14] Y.-H. Kuo, Y. K. Lee, Y. Ge, S. Ren, J. E. Roth, T. I. Kamins, D. A. B. Miller, and J. S. Harris, "Strong quantum-confined Stark effect in germanium quantum-well structures on silicon," *Nature*, Vol. 437, No. 7063, pp. 1334 – 1336, Oct. 2005. [Article \(CrossRef Link\)](#)
- [15] S. Cho, J. Park, H. Kim, R. Sinclair, B.-G. Park, and J. S. Harris Jr., "Effects of germanium incorporation on optical performances of silicon germanium passive devices for group-IV photonic integrated circuits," *Photonics and Nanostructures: Fundamentals and Applications*, Vol. 12, No. 1, pp. 54–68, Feb. 2014. [Article \(CrossRef Link\)](#)
- [16] C. Auth et al., "45nm High-k + Metal Gate Strain-Enhanced Transistors," in *Technical Dig. Of 2008 VLSI Symposium*, pp. 128–129, Jun. 2008. [Article \(CrossRef Link\)](#)
- [17] C. R. Brundle, C. A. Evans, Jr., and S. Wilson, *Encyclopedia of Materials Characterization: Surface, Interfaces, Thin Films*, Butterworth-Heinemann Ltd. (Oxford, UK), 1992. [Article \(CrossRef Link\)](#)
- [18] S. Sun, Y. Sun, Z. Liu, D.-I. Lee, S. Peterson, and P. Pianetta, "Surface termination and roughness of Ge(100) cleaned by HF and HCl solutions," *Applied Physics Letters*, Vol. 88, No. 1, pp. 021903-1–021903-3, Jan. 2006. [Article \(CrossRef Link\)](#)
- [19] M. Lin, M. Li, X. An, Q. Yun, M. Li, Z. Li, P. Liu, X. Zhang, and R. Huang, "Surface passivation of the Ge substrate by novel nitrogen plasma immersion treatment," *Semiconductor Science and Technology*, Vol. 28, No. 8, pp. 85010–85013, Aug. 2013. [Article \(CrossRef Link\)](#)



**Xiaochi Chen** received his B.E. degree in electronic science and technology in 2010 from Huazong University of Science and Technology, Wuhan, China, and the M.S. degree from Stanford University, Stanford, CA, USA, where he is currently working toward a Ph.D. degree in

electrical engineering. His research interests include germanium lasers and silicon photonics for optical interconnects.



**Yijie Huo** received his B.E. degree in electrical engineering from Tsinghua University in 2002, M.S. degree in electrical engineering from University of Maryland College Park in 2004, and Ph.D. degree in electrical engineering from Stanford University in 2010. Currently, Dr. Yijie Huo is a research

associate in the Department of Electrical Engineering at Stanford University. His research is focused on group-IV materials and devices for on-chip interconnection and nano-structured crystal thin-film solar cells.



**Seongjae Cho** received his B.S. and Ph.D. degrees in electrical engineering from Department of Electrical and Computer Engineering, Seoul National University, Seoul, Republic of Korea, in 2004 and 2010, respectively. He worked as an exchange researcher at the National Advanced Industrial Science and Technology (AIST), Tsukuba, Ibaraki, Japan, in 2009. He worked as a postdoctoral researcher at Seoul National University in 2010, and at the Department of Electrical Engineering, Stanford University, from 2010 to 2013. He has been working as an assistant professor at the Department of Electronic Engineering and the Department of IT Convergence Engineering (Graduate School), Gachon University, Seongnam-si, Republic of Korea, since 2013. His main research interests include nanoscale CMOS devices, device-circuit co-optimization, emerging memory technologies, optical and photonic devices, and electronic-photonic integrated circuits.



**Byung-Gook Park** received his B.S. and M.S. degrees in electronic engineering from Seoul National University, Seoul, Republic of Korea, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, USA, in 1990. From 1990 to 1993,

he was with AT&T Bell Laboratories, where he contributed to the development of 0.1- $\mu\text{m}$  CMOS and its characterization. From 1993 to 1994, he was with Texas Instruments, developing 0.25- $\mu\text{m}$  CMOS. In 1994, he joined Seoul National University, where he is a professor. In 2002 and 2010, he was with Stanford University as a visiting professor. He led the Inter-university Semiconductor Research Center (ISRC) at Seoul National University as the director from 2008 to 2010. He has authored more than 1,000 journal and conference papers and holds 122 Korea and international patents with 222 pending patents. His current research interests include design and fabrication of nanoscale CMOS, 3-D nonvolatile memory devices and architectures, silicon quantum-dot devices, and neuromorphic systems. Dr. Park has served as a committee member at several international conferences, including Microprocesses and Nanotechnology, IEEE International Electron Devices Meeting (IEDM), International Conference on Solid State Devices and Materials (SSDM), and Technical Program Chairs and General Chairs for eh IEEE Silicon Nanoelectronics Workshop (SNW). In addition, he worked as an editor of IEEE Electron Device Letters. He received the Best Teacher Award from the School of Electrical Engineering, Seoul National University, in 1997, Education Award from the College of Engineering, Seoul National University in 2006, Haedong Academic Award from The Institute of Electronics and Information Engineers of Korea (IEIE) in 2008, and Nano-Innovation Award from the minister of the Ministry of Science, ICT and Future Planning (MSIP) of Korea in 2013.



**James S. Harris, Jr.** received his B.S., M.S., and Ph.D. degrees from Stanford University, Stanford, CA, USA, in 1964, 1965, and 1969, respectively, all in electrical engineering. In 1969, he joined the Rockwell International Science Center, Thousand Oaks, CA, where he was one of the key

contributors to ion implantation, molecular beam epitaxy, and heterojunction devices, leading to their preeminent position in GaAs technology. In 1980, he became the Director of the Optoelectronics Research Department. In 1982, he joined the Solid State Electronics Laboratory, Stanford University, as a professor of electrical engineering, where he was the Director of the Solid State Electronics Laboratory (1984-1998), the Director of the Joint Services Electronics Program (1985-1999), and is currently the James and Ellenor Chesebrough Professor of Electrical Engineering, Applied Physics, and Materials Science in the Center for Integrated Systems. He has supervised more than 110 Ph.D. students, is the author of more than 900 publications, and holds 28 issued U.S. patents. His research interests include the physics and applications of ultra-small structures and novel materials to new high-speed and optoelectronic devices and systems. Dr. Harris is a member of the U.S. National Academy of Engineering and a Fellow of the American Physical Society, Optical Society of America, and Materials Research Society. He was the recipient of the 2000 IEEE Morris N. Liebmann Memorial Award, the 2000 International Compound Semiconductor Conference Walker Medal, the IEEE 3rd Millennium Medal, an Alexander von Humboldt Senior Research Prize in 1998, and the 2008 International MBE Conference MBE Innovator Award for his contributions to compound semiconductor materials, devices and technology.