



Characterization of Conduction Mechanism in Cu Schottky Contacts to p-type Ge

Se Hyun Kim, Chan Yeong Jung, and Hogyong Kim[†]

Department of Visual Optics, Seoul National University of Science and Technology (Seoultech), Seoul 139-743, Korea

Received September 29, 2014; Revised October 6, 2014; Accepted October 10, 2014

Germanium (Ge) is a promising material for next generation nanoelectronics and multiple junction solar cells. This work investigated the electrical properties in Cu/p-type Ge Schottky diodes, using current-voltage (I-V) measurements. The Schottky barrier heights were 0.66, 0.59, and 0.70 eV from the forward $\ln(I)$ -V, Cheung, and Norde methods, respectively. The ideality factors were 1.92 and 1.78 from the forward $\ln(I)$ -V method and Cheung method, respectively. Such high ideality factor could be associated with the presence of an interfacial layer and interface states at the Cu/p-Ge interface. The reverse-biased current transport was dominated by the Poole-Frenkel emission rather than the Schottky emission.

Keywords: p-type Ge, Schottky barrier heights, Ideality factors, Poole-Frenkel effect

1. INTRODUCTION

Germanium (Ge) has gained considerable interest for next generation nanoelectronics, due to its high mobility (its electron mobility is two times higher than that of Si [1]). However, Ge n-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) have been shown to have inferior drive current performance, compared to Si n-channel MOSFETs, which was attributed to electrically active defects on the Ge surfaces [2]. Another problem for realizing high performance Ge n-MOSFETs is the large effective Schottky barrier height at the metal/Ge interface, which results from the strong Fermi-level pinning [3]. It has been shown that the charge neutrality level (CNL) is located very close to the valence band edge EV of Ge [4], which eventually leads to a high contact resistance between metal/n-Ge contacts. In addition, this gives rise to the problem of the absence of Schottky barriers on p-type Ge [5]. As a result the investigation of electrical properties in Ge has mainly focused on n-type material [6]. Recently, concentrator photovoltaics (CPVs) based on In-

GaP/(In)GaAs/Ge triple junction solar cells have been reported to achieve more than 30% efficiency [7]. In triple junction solar cells, p-type Ge wafer can be used as starting material, because it is easy to form p-n Ge bottom cells by diffusion of As or P atoms from the nucleation layer, such as GaAs or InGaP, during the overgrowth. To improve the cell efficiency, further understanding of p-type Ge layer with a high quality of metal contact is required.

Metal-semiconductor (MS) contacts are used to understand the carrier transport across the MS contacts, which are required to achieve high-performance Ge-based devices. Until now, several methods, such as In plating [8], passivation of the Ge surface [9,10], and insertion of a thin insulation layer [11,12], have been employed to obtain the metal/p-Ge Schottky contacts. Based on the results of hydrogen plasma treatment on p-type Ge, Kolkovsky et al. suggested that earlier difficulties in making good Schottky barriers were due to the presence of hydrogen acting as an acceptor in p-type Ge [5]. Thathachary et al. [9] reported on the fabrication of Zr and Al Schottky contacts by sulfur passivation of the Ga-doped Ge surface. The barrier heights for the metals were evaluated as 0.6 and 0.57 eV for Zr and Al, respectively. Using Se treatment, Janardhanam et al. obtained a barrier height of 0.33 eV for Al/p-Ge Schottky contact [10]. Nishimura et al. showed that by inserting a very thin oxide layer, such as GeO_x or AlO_x, Al and Au metal contacts to p-Ge can be changed from ohmic to rectifying characteristics, by varying the thickness of

[†] Author to whom all correspondence should be addressed:
E-mail: hogyongkim@gmail.com

Copyright ©2014 KIEEME. All rights reserved.

This is an open-access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (<http://creativecommons.org/licenses/by-nc/3.0>) which permits unrestricted noncommercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

the oxide layer [11].

Among contact metals, Cu possesses excellent electrical and thermal conductivities. It is well known that Cu is prone to diffuse into Si semiconductor, without any diffusion barrier [13]. The failure mechanism and indiffusion parameters for Cu contacts with the InGaP layer have also been demonstrated [14]. These indicate that Cu atoms can diffuse into a Ge layer. Thus, detailed studies of the interface characteristics between Cu and Ge layers are very important for achieving high performance in Ge-based devices. To the best of our knowledge, however, there is little knowledge concerning the Cu Schottky contacts with p-type Ge. This work conducted electrical characterization of Cu/p-type Ge Schottky contacts, to understand the current transport mechanism across the Cu/p-Ge interface.

2. EXPERIMENTS

Ga-doped Ge (100) wafers (thickness: 500 μm, size: 2 inch) were used in this investigation. Single side polished Ge wafer, grown by the Czochralski method, was purchased from i-Nexus Inc. The room-temperature carrier concentration was about $\sim 1 \times 10^{17} \text{ cm}^{-3}$. These samples were cut into small pieces. Copper (Cu) Schottky contacts with a thickness of 50 nm were deposited by radio-frequency (RF) magnetron sputtering through a shadow mask onto the Ge surface, after solvent cleaning. For Ohmic contact, In metal was rubbed over approximately half of the sample. Current-voltage (I-V) measurements were performed at room temperature, using an HP 4155C semiconductor parameter analyzer.

3. RESULTS AND DISCUSSION

Figure 1 shows the (a) linear, and (b) semilogarithmic I-V characteristics measured at room temperature. The forward bias characteristics of a Schottky diode based on the thermionic emission (TE) model are given by [15]:

$$I = I_0[\exp(q(V - IR_s) / nkT) - 1] \tag{1}$$

$$I_0 = AA^{**}T^2 \exp(-q\phi_b / kT) \tag{2}$$

where, I_0 is the reverse bias saturation current, A is the diode area, A^{**} is the effective Richardson constant ($48 \text{ Acm}^{-2}\text{K}^{-2}$ for p-type Ge [11]), ϕ_b is the effective Schottky barrier height, n is the ideality factor, V is the applied voltage, and R_s is the series resistance. For values of V greater than $3 kT/q$, the ideality factor can be obtained from the slope of the linear region of the $\ln(I)$ - V curves. The forward I-V analyses revealed that $\phi_b = 0.66 \text{ eV}$ and $n = 1.92$. The ideality factor at room temperature was larger than unity, which has been attributed to the presence of interfacial states and an insulator layer between the metal and the semiconductor [16]. The bias-voltage-dependent ideality factor $n(V)$ could be obtained through the relation of $n(V) = q / kT [dV / d(\ln I)]$.

The corresponding curve in Fig. 2 shows that the ideality factor increases slowly with increasing forward bias in the region where the effect of the series resistance is small (e.g. linear region of $\ln(I)$ - V), and then increases more rapidly with increasing forward bias, where the effect of the series resistance dominates the $\ln(I)$ - V characteristics. The latter effect gives rise to the cur-

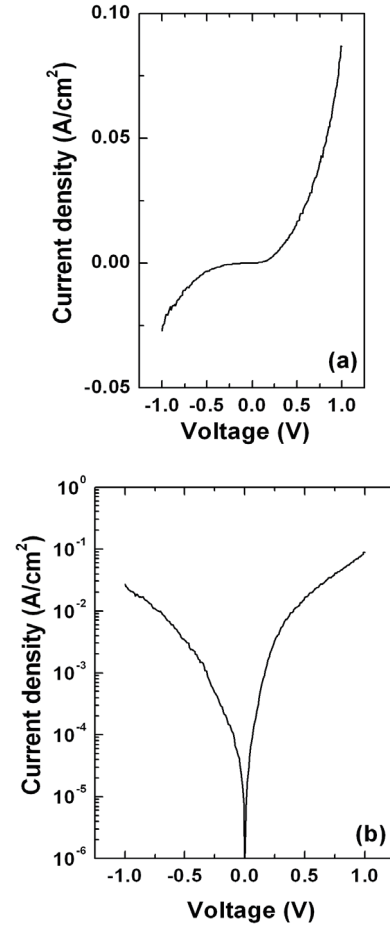


Fig. 1. (a) Linear and (b) semilogarithmic current-voltage (I-V) characteristics, for the Cu/p-Ge Schottky diode.

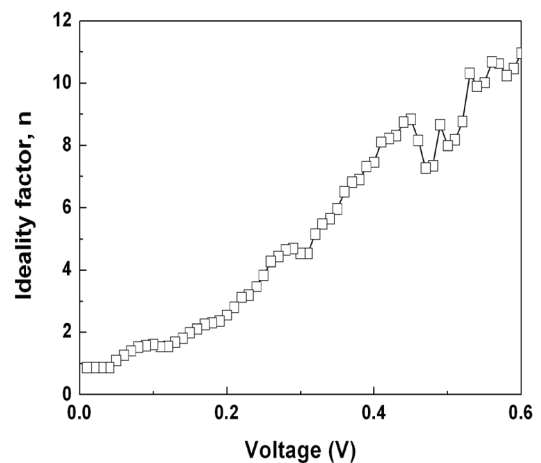


Fig. 2. Voltage-dependent ideality factor.

vature at higher current in the semilogarithmic I-V plot, as Fig. 1(b) shows.

The series resistance (R_s), an important parameter in the electrical characteristics of Schottky barrier diodes, results from contact wires, or from the bulk resistance of the semiconductor, the interfacial layer, and the interface states. According to Cheung's model, the values of series resistance can be determined from the slopes of the following equations [17]:

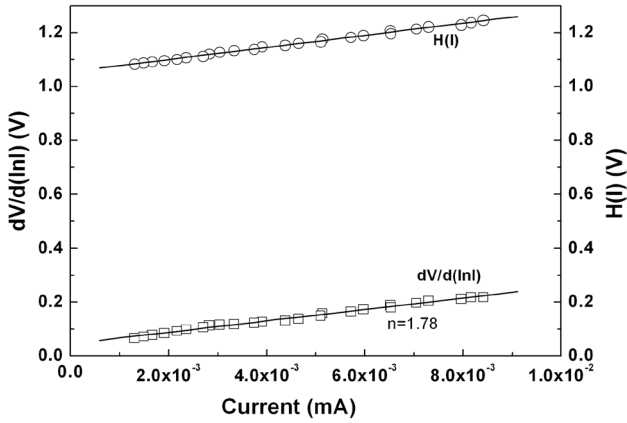


Fig. 3. Plots of $dV/d(\ln I)$ vs. I and $H(I)$ vs. I for the Cu/p-Ge Schottky diode.

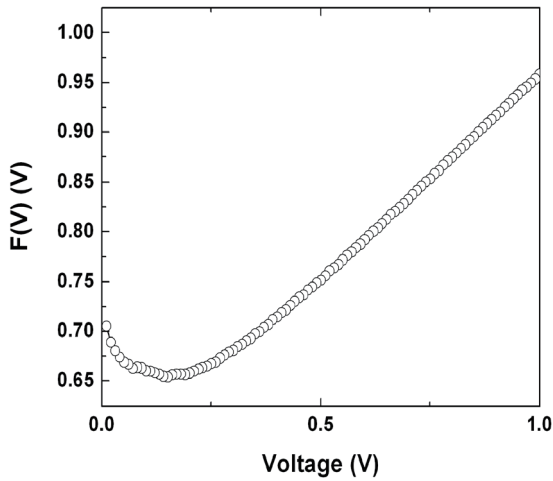


Fig. 4. Plot of $F(V)$ vs. V from the Norde method.

$$dV / d(\ln I) = nkT / q + IR_s \tag{3}$$

$$H(I) = V - (nkT / q) \ln(I / AA^*T^2) \tag{4}$$

where, $H(I)$ is given by $H(I) = n\phi_B + IR_s$. Figure 3 shows the plots of $dV/d(\ln I)$ vs. I and $H(I)$ vs. I . From the $dV/d(\ln I)$ vs. I plot, the ideality factor and the series resistance were obtained as 1.78 and 21.1 k Ω , respectively. From the $H(I)$ vs. I plot, the barrier height and the series resistance were found to be 0.59 eV and 22.4 k Ω , respectively. The R_s values from Eqs. (3) and (4) are in good agreement with each other, showing the consistency of Cheung's approach. However, the R_s values obtained are very high. The presence of an interfacial layer and possibly interface states might contribute significantly to the series resistance for the Cu/p-Ge Schottky diode.

Norde proposed an empirical function to calculate both the barrier height and series resistance for a Schottky diode [18]. The Norde function is defined as:

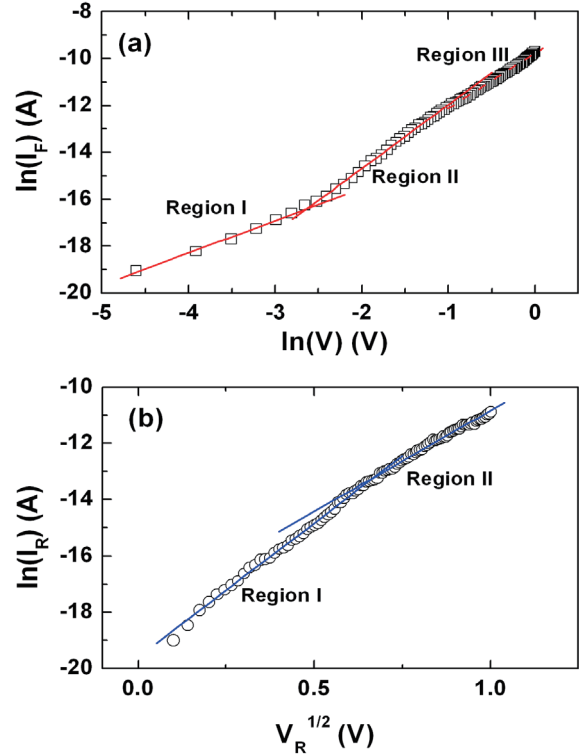


Fig. 5. (a) Plot of $\ln(I)$ vs. $\ln(V)$ under forward bias and (b) plot of $\ln(I)$ vs $V^{1/2}$ under reverse bias.

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q} \ln\left(\frac{I}{AA^*T^2}\right) \tag{5}$$

where, γ is an integer (dimensionless) greater than the ideality factor. In this work, the value two was used for the calculation. From the minimum of the F - V plot, the effective barrier height can be expressed as:

$$\phi_B = F(V_{min}) + V_{min} / 2 - kT / q \tag{6}$$

where, $F(V_{min})$ is the minimum value of $F(V)$, and V_{min} is the corresponding voltage. Figure 4 shows the $F(V)$ - V curve of the Cu/p-Ge Schottky diode. The barrier height obtained was 0.70 eV. The barrier height obtained from the Norde method is a little higher than those from the forward bias $\ln(I)$ - V and Cheung methods. Such differences in the barrier height values could be attributed to the extraction from different regions of the forward-bias I - V plot. In other words, forward $\ln(I)$ - V and Cheung methods are applied to the linear (low voltage) and non-linear (high voltage) sections of the forward-bias $\ln(I)$ - V characteristics, respectively. On the other hand, the Norde method is applied to the full forward-bias region of the $\ln(I)$ - V characteristics of the junctions [6].

As Fig. 5 (a) shows, the forward-bias $\ln(I)$ - $\ln(V)$ curve is characterized by three linear regions, indicating different conduction mechanisms. At low voltages (Region I), an ohmic conduction is dominant where the logarithmic slope is about 1.4. In this region, the injection of charge carriers from the electrodes into the semiconductor material is considerably reduced, due to the low bias voltage, and tunneling is the dominant current trans-

port mechanism. In Region II, a square law region appears with a slope of 2.7, and charge transport is mainly governed by the space charge limited current (SCLC), with an exponential distribution of traps in the band gap [19]. At high voltages (Region III), the slope decreases to about 2.3, indicating that the device approaches trap-free SCLC [6]).

As shown in Fig. 5(b), the reverse-biased current transport was analyzed using the form of $\ln(I)$ vs. $V^{1/2}$. The linearity in the curve can be interpreted via either the Schottky effect, or the Poole-Frenkel effect. Current-voltage expressions are given as [20]:

$$I = AA^* T^2 \exp\left(-\frac{\phi_s}{kT}\right) \exp\left(\frac{\beta_s}{kT} \sqrt{\frac{V}{d}}\right) \quad (7)$$

for the Schottky effect, and as:

$$I = J_0 A \exp\left(\frac{\beta_{PF}}{kT} \sqrt{\frac{V}{d}}\right) \quad (8)$$

for the Poole-Frenkel effect. Here, $J_0 = (\sigma_0 F)$, where σ_0 is the low-field conductivity, which depends on the carrier mobility and the donor activation energy) is the low-field current density. β_s and β_{PF} are, respectively, the Schottky and the Poole-Frenkel field lowering coefficients given by $2\beta_s = \beta_{PF} = (e^3 / \pi \epsilon_s \epsilon_0)^{1/2}$. The theoretical values of β_s and β_{PF} for Ge were determined as 1.20×10^{-5} and $2.40 \times 10^{-5} \text{ Vm}^{1/2} \text{ V}^{-1/2}$, respectively [21].

For the Cu/p-Ge Schottky contact, we observed two regions of linear variation with a slope of $9.60 \times 10^{-5} \text{ eV m}^{1/2} \text{ V}^{-1/2}$ in the lower bias region (Region I), and $7.20 \times 10^{-5} \text{ eV m}^{1/2} \text{ V}^{-1/2}$ in the higher bias region (Region II). A comparison of the experimental and theoretical slopes revealed that the experimental slopes for both in the low and high bias regions were much closer to those of the Poole-Frenkel effect. In Schottky emission, the carrier that absorbs the thermal energy emits over the potential barrier at the interface; whereas in Poole-Frenkel emission, the carrier transport occurs through trap states, by applying an electric field [22]. Furthermore, Kobayashi *et al.* observed a very large ideality factor in the thicker SiN region for the Al/SiN/n-Ge Schottky diode, which they explained by the transport mechanism due to the tunneling and/or the Poole-Frenkel emission [23]. Based on the results so far, we can deduce that the effect of the presence of an interfacial layer and interface states is significant on the current transport in the Cu/p-Ge Schottky diode. Further investigation employing various surface treatments on p-type Ge is underway.

4. CONCLUSIONS

We performed current-voltage (I-V) measurements, to characterize the electrical properties in Cu/p-type Ge Schottky contacts. We obtained Schottky barrier heights of 0.66, 0.59, and 0.70 eV from the forward $\ln(I)$ -V, Cheung, and Norde methods, respectively. We obtained the ideality factors of 1.92 and 1.78 from the forward $\ln(I)$ -V and Cheung methods, respectively. A higher ideality factor than unity would be due to the presence of an interfacial layer and interface states across the Cu/p-Ge interface. The reverse-biased current transport was more closely related to the Poole-Frenkel effect, than to the Schottky effect.

ACKNOWLEDGMENT

This study was supported by the Research Program, funded by Seoul National University of Science and Technology.

REFERENCES

- [1] P. Lim, D. Chi, X. Wang, and Y. Yeo, *Appl. Phys. Lett.*, **101**, 172103 (2012). [DOI: <http://dx.doi.org/10.1063/1.4762003>].
- [2] A. Chroneos, U. Schwingenschlog, and A. Dimoulas, *Ann. Phys.*, **524**, 123 (2012). [DOI: <http://dx.doi.org/10.1002/andp.201100246>].
- [3] T. Nishimura, K. Kita, and A. Toriumi, *Appl. Phys. Lett.*, **91**, 123123 (2007). [DOI: <http://dx.doi.org/10.1063/1.2789701>].
- [4] D. Kuzman, K. Martens, T. Krishnamohan, and K. Saraswat, *Appl. Phys. Lett.*, **95**, 252101 (2009). [DOI: <http://dx.doi.org/10.1063/1.3270529>].
- [5] V. Kolkovsky, S. Klemm, M. Allardt, and J. Weber, *Semicond. Sci. Technol.*, **28**, 025007 (2013). [DOI: <http://dx.doi.org/stacks.iop.org/SST/28/025007>].
- [6] Z. Khurelbaatar, Y. Kil, H. Yun, K. Shim, J. Nam, K. Kim, S. Lee, and C. Choi, *J. Alloys Compd.*, **614**, 323 (2014). [DOI: <http://dx.doi.org/10.1016/j.jallcom.2014.06.132>].
- [7] R. King, D. Law, K. Edmondson, C. Fetzer, G. Kinsey, H. Yoon, R. Sherif, and N. Karam, *Appl. Phys. Lett.*, **90**, 183516 (2007). [DOI: <http://dx.doi.org/10.1063/1.2734507>].
- [8] P. Clauws, G. Huylebroeck, E. Simoen, P. Vermaercke, F. Smet, and J. Vennik, *Semicond. Sci. Technol.*, **4**, 910 (1989). [DOI: <http://dx.doi.org/10.1088/0268-1242/4/11/003>].
- [9] V. Thathachary, N. Bhat, N. Bhat, and S. Hegde, *Appl. Phys. Lett.*, **96**, 152108 (2010). [DOI: <http://dx.doi.org/10.1063/1.3387760>].
- [10] V. Janardhanam, H. Yun, J. Lee, V. Reddy, H. Hong, K. Ahne, and C. Choi, *Scripta Mater.*, **69**, 809 (2011). [DOI: <http://dx.doi.org/10.1016/j.scriptamat.2013.09.004>].
- [11] T. Nishimura, K. Kita, and A. Toriumi, *Appl. Phys. Exp.*, **1**, 051406 (2008). [DOI: <http://dx.doi.org/10.1143/APEX.1.051406>].
- [12] V. Kishore, P. Paramahans, S. Sadana, U. Ganguly, and S. Lodha, *Appl. Phys. Lett.*, **100**, 142107 (2012). [DOI: <http://dx.doi.org/10.1063/1.3700965>].
- [13] A. Cros, M. Aboelfotoh, and K. Tu, *J. Appl. Phys.*, **67**, 3328 (1990). [DOI: <http://dx.doi.org/10.1063/1.345369>].
- [14] D. Liu and C. Lee, *J. Appl. Phys.*, **92**, 987 (2002). [DOI: <http://dx.doi.org/10.1063/1.1487439>].
- [15] S. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981) p. 270.
- [16] J. Sullivan, R. Tung, M. Pinto, and W. Graham, *J. Appl. Phys.*, **70**, 7403 (1991). [DOI: <http://dx.doi.org/10.1063/1.349737>].
- [17] S. Cheung and N. Cheung, *Appl. Phys. Lett.*, **49**, 85 (1986). [DOI: <http://dx.doi.org/10.1063/1.97359>].
- [18] H. Norde, *J. Appl. Phys.*, **50**, 5052 (1979). [DOI: <http://dx.doi.org/10.1063/1.325607>].
- [19] M. Sharma and S. Tripathi, *J. Appl. Phys.*, **112**, 024521 (2012). [DOI: <http://dx.doi.org/10.1063/1.4737589>].
- [20] J. Simmons, *J. Phys. D: Appl. Phys.*, **4**, 613 (1971). [DOI: <http://dx.doi.org/10.1088/0022-3727/4/5/202>].
- [21] A. Kumar, V. Reddy, V. Janardhanam, M. Seo, H. Hong, K. Shin, and C. Choi, *J. Electrochem. Soc.*, **159**, H33 (2012). [DOI: <http://dx.doi.org/10.1149/2.041201jes>].
- [22] J. Lin, S. Banerjee, J. Lee, and C. Teng, *IEEE Electron Device Lett.*, **11**, 191 (1990). [DOI: <http://dx.doi.org/10.1109/55.55246>].
- [23] M. Kobayashi, A. Kinoshita, K. Saraswat, H. Wong, and Y. Niishi, *J. Appl. Phys.*, **105**, 023702 (2009). [DOI: <http://dx.doi.org/10.1063/1.3065990>].