Wide Voltage Input Receiver with Hysteresis Characteristic to Reduce Input Signal Noise Effect

Arnab Kumar Biswas

In this paper, an input receiver with a hysteresis characteristic that can work at voltage levels between 0.9 V and 5 V is proposed. The input receiver can be used as a wide voltage range Schmitt trigger also. At the same time, reliable circuit operation is ensured. According to the research findings, this is the first time a wide voltage range Schmitt trigger is being reported. The proposed circuit is compared with previously reported input receivers, and it is shown that the circuit has better noise immunity. The proposed input receiver ends the need for a separate Schmitt trigger and input buffer. The frequency of operation is also higher than that of the previously reported receiver. The circuit is simulated using HSPICE at 0.35-µm standard thin oxide technology. Monte Carlo analysis is conducted at different process conditions, showing that the proposed circuit works well for different process conditions at different voltage levels of operation. A noise impulse of (V_{CC}/2) magnitude is added to the input voltage to show that the receiver receives the correct logic level even in the presence of noise. Here, V_{CC} is the fixed voltage supply of 3.3 V.

Keywords: Wide voltage input receiver, 0.9 V to 5 V, regenerative input receiver, wide voltage Schmitt trigger, hysteresis characteristic.

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I. Introduction

With the continuation of scaling in very large scale integration technology and the simultaneous increase in frequency of operation, there has been an increase in various types of parasitic effects. The parasitic components associated with pins, bond wires, packages, transmission lines, and so on are becoming more and more prominent. Thus, there are effects, such as crosstalk, reflection, oscillation of signal, and so on, that cause sudden changes in the signal level. So, the need for an input receiver that is capable of receiving the correct logic level in all conditions (that is, high noise immunity) is growing. For the case of a wide voltage range input receiver with high noise immunity, the problem is more severe because the method currently available, which is the use of the Schmitt trigger, is only applicable for the single-voltage level of operation. Until now, it seems that a wide voltage range Schmitt trigger has not been reported.

A Schmitt trigger is used to convert a varying input voltage into a stable logical signal (high or low). It needs a hysteresis characteristic to reduce the sensitivity to noise and disturbances [1]. Schmitt triggers have various kinds of applications. Herein, only the application in the input receiver is considered. Schmitt triggers have been widely used in input receivers to increase noise immunity. A block diagram of the conventional input receiver is shown in Fig. 1.

This receiver includes a Schmitt trigger followed by an input buffer. This input buffer may include a level-down converter if the receiver is to be used in a mixed voltage environment. The Schmitt trigger circuit receives input signals from the I/O pad and rejects input noise. A Schmitt trigger circuit with different high to low and low to high transition threshold voltages (V_{10} and V_{01}) has better noise immunity than any inverter [2]. Two

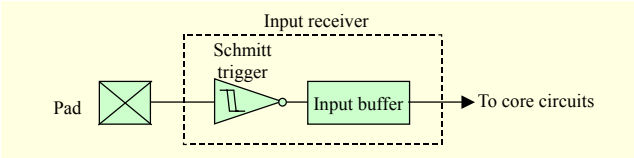

Fig. 1. Conventional input receiver block diagram.

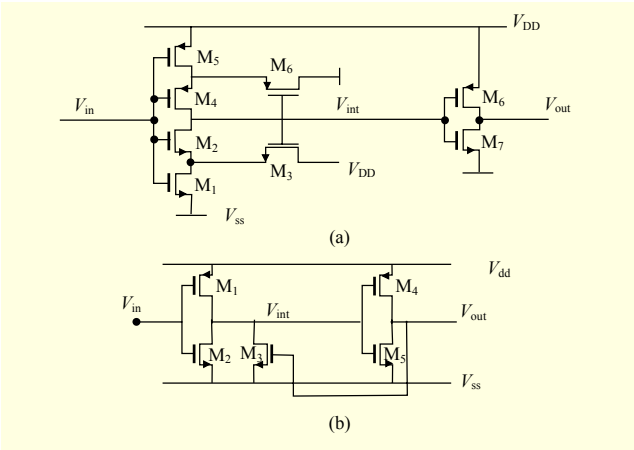

Fig. 2. (a) Commonly used Schmitt trigger and (b) Schmitt trigger with reduced MOSFETs [1].

conventional Schmitt trigger circuits are shown in Fig. 2. The most commonly used Schmitt trigger circuit is shown in Fig. 2(a). Detailed analysis of this can be found in [3] and [4]. Figure 2(b) shows a Schmitt trigger that uses fewer transistors [1].

The switching threshold (V_{01}) for the low to high transition of the input for the circuit shown in Fig. 2(b) was reported in [1].

$$V_{01} = \frac{V_{tn} + (V_{DD} - V_{tp})m}{1+m} \quad (1)$$

with

$$m = \sqrt{\frac{K_p (W/L)_1}{K_n (W/L)_2}},$$

where V_{tn} and V_{tp} are the threshold voltages and K_n and K_p are the transconductance parameters of the NMOS and PMOS transistors, respectively. This is the same as the normal CMOS inverter switching threshold voltage. Now, the switching threshold (V_{10}) for the high to low transition of the input for the circuit shown in Fig. 2(b) is

$$V_{10} = V_{01} - \frac{(V_{DD} - V_{tn})n}{2(1+m)} \quad (2)$$

with

$$n = \sqrt{\frac{K_n (W/L)_3}{K_p (W/L)_1}}.$$

It is worth noting that V_{10} can be varied, which means the amount of hysteresis can also be varied, by varying the W/L ratio of NMOS M_3. This also means that the noise margin can be varied as required. It is well known that the low noise margin (N_{ML}) is

$$N_{ML} = V_{IL} - V_{OL} \quad (3)$$

and the high noise margin (N_{MH}) is

$$N_{MH} = V_{OH} - V_{IH}, \quad (4)$$

where V_{IL} is the highest input voltage that can be regarded as low logic at the input and V_{IH} is the lowest input voltage that can be regarded as high logic at the input. V_{OL} is the stable input voltage for low logic and V_{OH} is the stable input voltage for high logic.

The above-mentioned Schmitt triggers cannot be used in wide voltage applications. They can operate only at a fixed operating voltage; that is, if the input voltage swing is less than the supply voltage, they will not operate correctly because of their fixed switching threshold voltage. The rail-to-rail voltage swing at the output will not be possible if the input voltage swing is less than the supply voltage. The Schmitt trigger will not be able to pull up or pull down the load with its full capacity because the switching threshold is not dependent on the input voltage swing. That is why an input receiver that employs a Schmitt trigger at the front end cannot operate in a wide range of input voltages. There is an input receiver depicted in [2] that uses a Schmitt trigger in front of a level-down converter. The circuit is not based upon a standard thin oxide CMOS process and, at the same time, can only receive a 3.3-V input signal with 1-V/2.5-V devices. This means that the circuit cannot support a wide voltage operation, which is an essential capability in a mixed voltage environment. With the advancement of technology, the supply voltage is decreasing day by day. Therefore, an input receiver that can work at a low voltage swing, such as from 0 V to 0.9V, as well as a high voltage swing, such as from 0 V to 5 V, is needed. This is because the board voltage and certain interfaces still use a 5-V supply.

In [5], a wide-range 5.0-V/3.3-V/1.8-V I/O buffer was reported. In [6], a 5.5-V-tolerant robust input receiver was reported. A high-voltage-tolerant input buffer for a 1.9-V external cache interface and for a 3.3-V system interface using 1.9-V MOS transistors was reported in [7]. A digital 3.3-V powered 3.3-V/5-V input buffer was reported in [8]. In [9], a 1.2-V/2.5-V-tolerant input buffer with only thin gate oxide devices was reported. In [10], a design methodology for mixed-voltage input buffers to receive $3\times V_{DD}$ input signals was verified. In [11], an NMOS blocking technique for a mixed-voltage I/O buffer realized with only $1\times V_{DD}$

devices that can receive $2\times V_{DD}$, $3\times V_{DD}$, and even $4\times V_{DD}$ input signals without the gate-oxide reliability issue was proposed. In that paper, 2.5-V/5-V and 1-V/3-V interfaces were reported. In [12], a novel 3.3-V/5-V compatible I/O circuit was proposed and measured to be effective in terms of reliability and speed. A 3.3-V/5-V compatible I/O buffer was reported in [13]. An overview and design of mixed-voltage I/O buffers with low-voltage thin oxide CMOS transistors was reported in [14]. A 2.5-V/5-V I/O buffer was also reported in that paper. In [15], the design of a 2.5-V/5-V mixed-voltage CMOS I/O buffer with only a thin oxide device and dynamic n-well bias circuit was reported. An I/O buffer with a 1.8-V/3.3-V interface was reported in [16]. The I/O driver reported in [17] supports a 3.3-V/2.5-V/1.8-V interface. A circuit design for mixed-voltage I/O buffers to prevent hot-carrier degradation was proposed in [18]. It can receive 1.5-V/3.3-V input signals.

In [19] and [20], a 0.9-V/1.2-V/1.8-V/2.5-V/3.3-V/5.0-V wide-range input/output buffer was reported. It uses an NMOS blocking technique to control the maximum voltage applicable to the gate of the receiving inverter. By doing that, the circuit ensures the reliability of the operation but it does not have high noise immunity. The reason is that the Schmitt trigger is not used in the circuit.

Apart from the wide voltage reliable operation, an input receiver also needs to have input noise rejection capability, which is only achievable if a Schmitt trigger is used. Thus, a new input receiver with hysteresis characteristic that can operate at input voltage levels between 0.9 V and 5 V is proposed herein. The receiver can work in a wide range of process variation conditions and a wide temperature range, which will be shown in section III. The operation of the proposed circuit will be compared to that of the input receiver reported in [19] and [20].

II. Proposed Input Receiver

A schematic diagram of the proposed input receiver is shown in Fig. 3. The input receiver needs two supply voltages for proper operation. One is V_{CC}, which is fixed at 3.3 V. The other is V_{DD}, which varies according to the input voltage range. For example, if the input voltage is from 0 V to 0.9 V, then the V_{DD} is 0.9 V. Actually, the voltage range for a specific technology node is fixed. For the start of communication, this V_{DD} value can be set according to the technology node that is communicating with this receiver.

The proposed input receiver operation is as follows. The NMOS pass transistor, npass, passes the pad voltage to the gate of the first inverter stage. The circuit consists of 0.35-μm 3.3-V devices. So, a voltage more than 3.3 V (such as 5 V) can cause

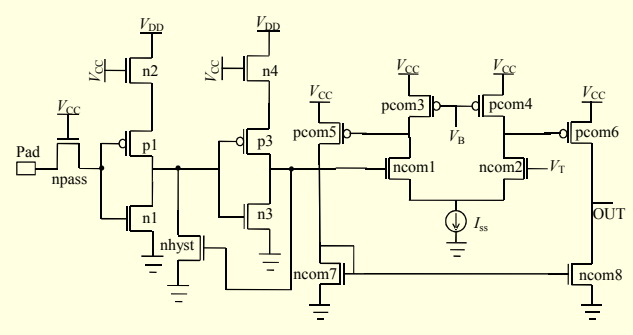

Fig. 3. Proposed input receiver.

the gate oxide to be overstressed. Thus, the npass transistor is there to protect the first inverter stage. Its gate voltage is fixed to V_{CC}, which is fixed at 3.3 V. If a voltage higher than 3.3 V arrives at the I/O pad, then npass will pass only $(V_{CC} - V_{tn})$, where V_{tn} is the threshold voltage of NMOS. This ensures reliable operation of the circuit. If the pad voltage is $(V_{CC} - V_{tn})$ or less, then npass will directly pass that to the gate.

However, this pass transistor has another effect, that is, it affects the voltage swing of the inverter because the switching threshold of the inverter is independent of the input voltage swing. Because the intention is to create a Schmitt trigger and hysteresis characteristic, the same voltage range must be maintained for the gate and the power supply, that is, the source of PMOS of the inverter stage. For this reason, the extra NMOS n2 is connected. It gives the required voltage drop at the source end of the PMOS p1. By this method, the voltage swing and the switching of the inverter stage are controlled. The exact configuration is used for the next inverter stage also. There is a feedback NMOS nhyst whose gate is connected to the output of the second inverter stage. The feedback NMOS guarantees the hysteresis characteristic of the receiver.

When the input voltage is low, the output of the first inverter is high. Because the output of the second inverter is low, the feedback NMOS is off. The switching threshold is from low to high; that is, V_{01} is similar to that of a simple inverter because the feedback NMOS does not affect the operation. However, when the second inverter is switching, then this NMOS is on and provides positive feedback. So, the Schmitt trigger operation is there.

When the input is high, the output of the first inverter is low. Because the output of the second inverter is high, the feedback NMOS is on. This means that the input must go down more than the earlier switching threshold voltage of V_{01} to switch the first inverter. These two different switching threshold voltages ensure a hysteresis characteristic. As the feedback NMOS is causing this behavior, the hysteresis and the noise margin can be controlled by controlling the (W/L) ratio of this NMOS.

Actually, the noise margin is decided by V_{IL} and V_{IH}. These two quantities change as soon as the switching threshold changes. If the *W*/*L* ratio of the feedback NMOS increases, then the N_{MH} will go up. Therefore, the *W*/*L* ratio can be set according to the noise margin requirement.

This is actually a tradeoff. If the *W*/*L* ratio of nhyst is increased, the pull-down strength will be enhanced because the first-stage pull-down NMOS n1 also pulls down the output of the first inverter stage. This in turn helps p3 of the second inverter stage to pull up the gate of the NMOS nhyst. This can be detrimental if the *W*/*L* ratios are not checked properly because then the only pull-up transistor p1 may not be able to pull the output of the first inverter stage at any input voltage. Of course the second inverter stage pull-down NMOS n3 helps p1 by pulling down the gate voltage of nhyst and turning it off, but that will happen only after n3 turns on. This means p1 has to pull the output voltage to a certain level; after that, n3 starts its operation and, together, they counteract n1, nhyst, and p3. Therefore, the *W*/*L* ratio of the hysteresis feedback NMOS nhyst can be changed after considering the above situations.

The remaining portion of the receiver is a two-stage comparator. This is added to ensure low voltage reception and a 0 V to 3.3 V voltage swing at the OUT terminal. The signal from the OUT node goes into the core circuit of the chip. This signal swing is fixed at 0 V to 3.3 V irrespective of the input voltage swing. This ensures reliable wide voltage range operation of the receiver. Here, the assumption is that the internal core circuit is operating at V_{CC}, that is, 3.3 V. The comparator consists of eight MOSFETs without taking the current source I_{ss} into account, which is used to bias the circuit. V_B is the biasing voltage, and V_T is the comparator threshold voltage. V_T is a parameter that can be selected based upon requirement. It directly affects the rising and falling, that is, delay of the OUT node. In this study, it is fixed at 0.8 V to ensure 0.9-V input reception. The 5-V input voltage is received correctly if V_T remains fixed at this voltage.

So, it can be seen that the proposed receiver has hysteresis for all voltage levels of the operation. This ensures the reduction of sensitivity to noise and disturbances [1]. On the other hand, this receiver works at several voltage levels (that is, 0.9 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5.0 V), and the maximum voltage received is not limited to the supply voltage of the technology node (that is, 3.3 V). Again, the reliability of the operation of the entire circuit is ensured by eliminating the problem of the gate oxide being overstressed, and the hot carrier effect is eliminated because all the node and junction voltages are kept within 3.3 V, that is, the rating of the 0.35-µm technology node. The simulation results and discussion are given in the next section.

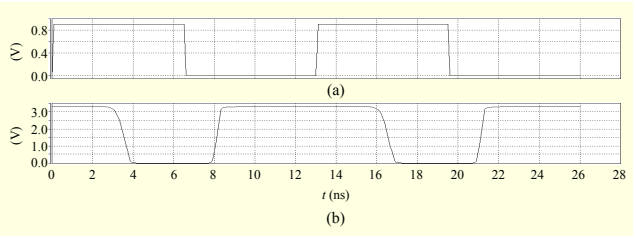

Fig. 4. (a) Input (0 V to 0.9 V) voltage at pad and (b) output (0 V to 3.3 V) voltage to core.

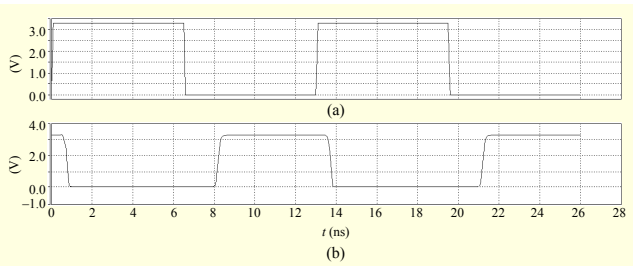

Fig. 5. (a) Input (0 V to 3.3 V) voltage at pad and (b) output (0 V to 3.3 V) voltage to core.

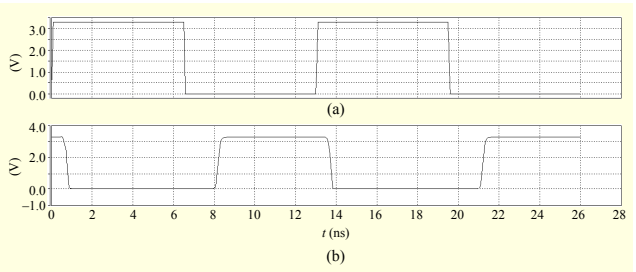

Fig. 6. (a) Input (0 V to 5 V) voltage at pad and (b) output (0 V to 3.3 V) voltage to core.

III. Simulation Results

1. Time Domain Analysis

The circuit is simulated using HSPICE at the 0.35-µm technology node. The time domain input and output waveforms at 0.9 V, 3.3 V, and 5 V are shown in Figs. 4, 5, and 6, respectively. The load capacitance is 50 fF.

The input rise and fall time (10% to 90%) for all voltage levels is kept at 100 ps, and time period is 13 ns, that is, the frequency is 77 MHz. The rise and fall time (10% to 90%) and average power of the output signal (without comparator) for all voltage level values are given in Table 1.

It can be seen that the rise and fall time decreases as the supply voltage increases. However, the average power increases as the supply voltage increases. This effect is due to the fact that a higher supply voltage helps a MOSFET charge a load more rapidly while causing more current, which results in

Table 1. Rise and fall time and average power for different voltage levels.

V_{DD} (V)	0.9	1.2	1.5	1.8	2.5	3.3	5
Rise time (ps)	447.82	344.41	260.05	251.56	244.05	231.42	223.16
Fall time (ps)	558.72	378.86	263.62	244.72	239.94	224.63	217.27
Ave. power (mW)	4.6	7.9	8.4	8.6	9.07	9.2	9.4

Table 2. Maximum frequency of operation for different voltage levels.

V_{DD} (V)	0.9	1.2	1.5	1.8	2.5	3.3	5
Max. freq. (MHz)	143	344	500	500	500	500	500

an increase in the average power. Another trend that can be seen is a relative decrease of the fall time with respect to the rise time with an increase in the supply voltage. The reason is that the MOSFETs are chosen to operate at the different voltage levels between 0.9 V and 5 V. For that, the pull-down portion is relatively weak for the lower voltages, and, with an increase of the supply voltage, the feedback NMOS nhyst switches on more quickly and the pull-down operation starts to dominate. As a result, the fall time becomes relatively small compared to the rise time with an increase in the supply voltage. The maximum frequency of the operation for different voltage level values is indicated in Table 2.

The internal core circuit does not have a very big parasitic capacitance. Therefore, the load capacitance value of 50 fF is justified. With a decrease in the supply voltage, the capacity of the circuit to charge the output node also decreases and that results in a decrease in the maximum frequency of the operation. There is an indication in [20] of a 50-MHz frequency of operation for the same input receiver reported in [19].

2. DC Analysis

The hysteresis characteristics for operation at 0.9 V, 3.3 V, and 5 V are shown in Figs. 7, 8, and 9, respectively. For all the figures, the output voltage is along the Y axis and the input voltage is along the X axis. The amount of hysteresis for different voltage levels is shown in Table 3.

From the simulation of the receiver previously reported in [19], the noise margin values obtained are $N_{ML} = 0.128$ V and $N_{MH} = 2.3$ V. These two values are fixed for all voltage level values because, for this case, the supply voltage is constant for all voltage level values. For the proposed circuit, the noise

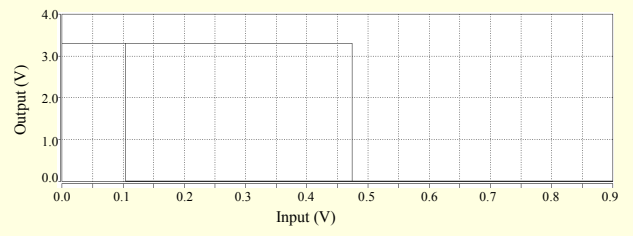

Fig. 7. Hysteresis characteristic for 0.9 V input voltage swing.

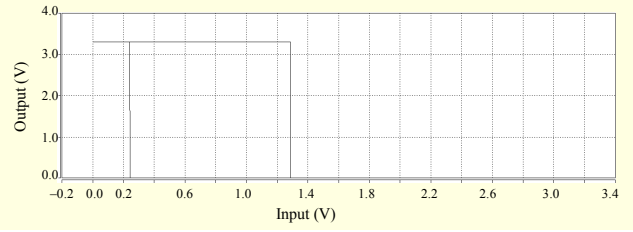

Fig. 8. Hysteresis characteristic for 3.3 V input voltage swing.

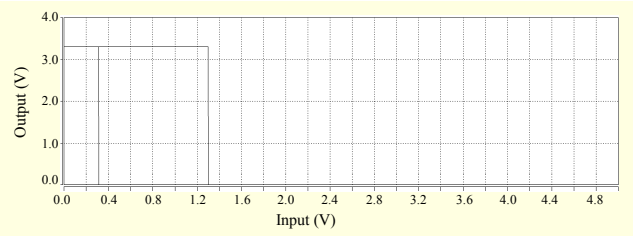

Fig. 9. Hysteresis characteristic for 5 V input voltage swing.

Table 3. Amount of hysteresis for different voltage levels.

V_{DD} (V)	0.9	1.2	1.5	1.8	2.5	3.3	5
Hysteresis (V)	0.37	0.406	0.459	0.544	0.98	1.045	1.06

Table 4. Different noise margin values for all voltage levels.

V_{DD} (V)	0.9	1.2	1.5	1.8	2.5	3.3	5
N_{ML} (V)	0.474	0.622	0.785	0.958	1.256	1.285	1.3
N_{MH} (V)	0.796	0.984	1.174	1.386	2.224	3.06	4.76

margin varies for different voltage levels. The various noise margin values for the different voltage level values are shown in Table 4. Both N_{ML} and N_{MH} increase with an increase in V_{DD} because the noise margin depends upon V_{DD}. The N_{MH} value can change by varying the W/L ratio of the feedback NMOS nhyst.

3. Circuit Performance in Presence of Noise

A (V_{DD}/2) noise impulse is added to the input pad voltage.

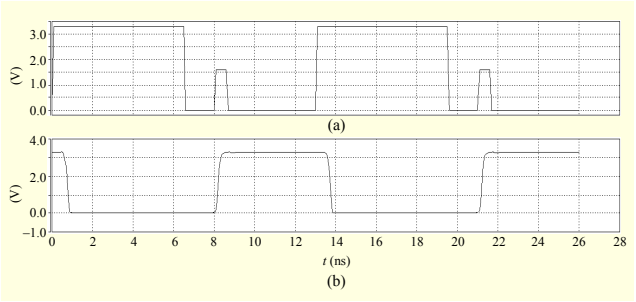

Fig. 10. (a) Input voltage with noise impulse at logic zero and (b) output voltage without any false peak.

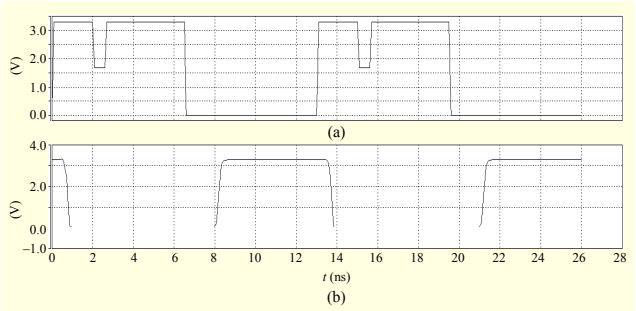

Fig. 11. (a) Input voltage with noise impulse at logic one and (b) output voltage without any false peak.

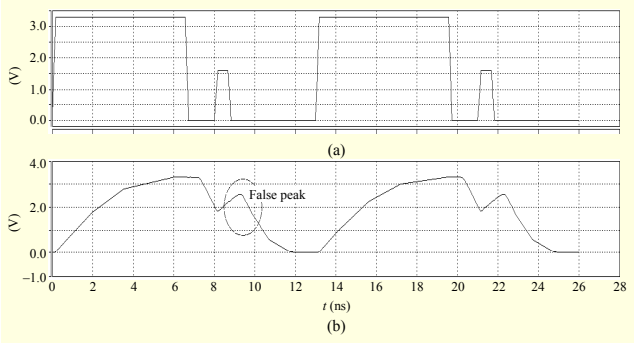

Fig. 12. (a) Input voltage with noise impulse and (b) output voltage with false peak.

The noise impulse width is 500 ps and the rise and fall time is 100 ps. This noise impulse is added to simulate the sudden voltage fluctuations in the input voltage owing to such an unwanted effect as crosstalk or reflection. The voltage fluctuation can cause false logic reception in the core. The main objective is to design a high noise immunity receiver that can tolerate this type of sudden noise impulse in the input signal. The resulting voltage waveforms are shown in Figs. 10 and 11. A noise impulse is added to logic level zero (Fig. 10) as well as to logic level one (Fig. 11).

From the above figures, it is clear that the proposed receiver has shown noise immunity to (V_{DD}/2) amplitude noise impulses. For comparison, the receiver reported in [19] is simulated under similar noise condition. The time domain waveform is shown below. As shown in Fig. 12, the chance of false logical reception is higher for receiver reported in [19].

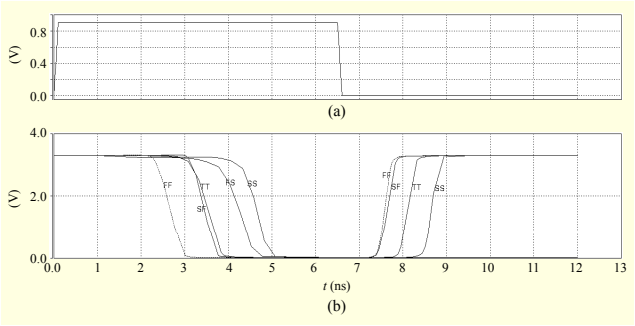

Fig. 13. (a) Input (0 V to 0.9 V) voltage at pad and (b) output (0 V to 3.3 V) voltage to core at five corners.

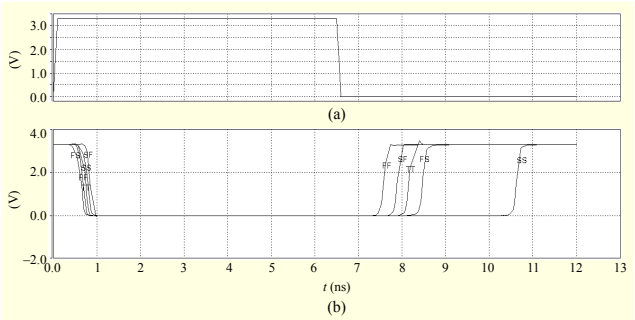

Fig. 14. (a) Input (0 V to 3.3V) voltage at pad and (b) output (0 V to 3.3 V) voltage to core at five corners.

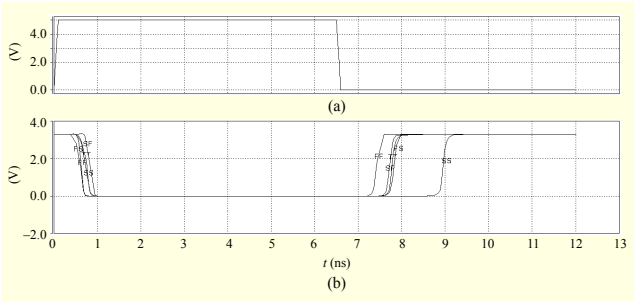

Fig. 15. (a) Input (0 V to 5 V) voltage at pad and (b) output (0 V to 3.3 V) voltage to core at five corners.

4. Time Domain Corner Analysis

Corner analysis is conducted at 0.9 V, 3.3 V, and 5 V. The time domain waveforms are shown in Figs. 13 through 15. In these figures, the following labels are added for the corresponding output signals: typical (TT), slow (SS), fast (FF), fast-slow (FS), and slow-fast (SF).

As shown in Fig. 13, for the 0.9-V FS corner, only the pull-down operation exists, not the pull-up operation. In any other situation, all the corners at all voltages work properly. The

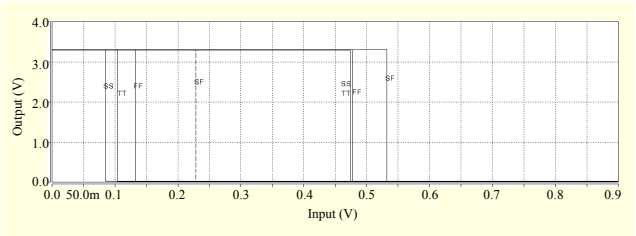

Fig. 16. Hysteresis characteristics for 0.9 V input voltage swing at five corners.

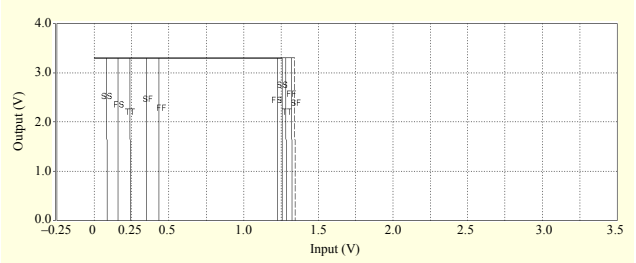

Fig. 17. Hysteresis characteristics for 3.3 V input voltage swing at five corners.

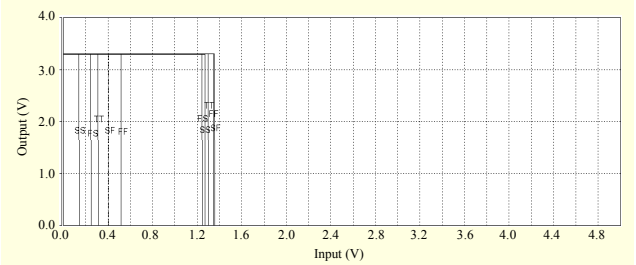

Fig. 18. Hysteresis characteristics for 5 V input voltage swing at five corners.

apparent anomaly is caused by the fact that at the FS corner, NMOS is made stronger compared to PMOS. As stated earlier in the time domain analysis, this strong NMOS causes the pull-down operation to be stronger and the pull-up operation to be weaker than normal. A low voltage such as 0.9 V adds to this effect, and the weak PMOS cannot counterbalance the strong (fast) NMOS's pulling action as a result. This is why only the pull-down operation is available, not the pull-up operation.

5. DC Domain Corner Analysis

DC domain corner analysis is conducted at 0.9 V, 3.3 V, and 5 V. The resultant waveforms are shown in Figs. 16 through 18, with all the five corner labels on the corresponding output voltages. In Fig. 16, the hysteresis for the FS corner is not included because only the pull-down operation occurs at 0.9 V, not the pull-up operation, and, thus, the hysteresis loop is not created.

The amount of hysteresis, N_{MH} and N_{ML}, for every corner at 0.9V, 3.3 V, and 5 V is calculated. The results are given in Tables 5 through 7. From Figs. 16, 17, and 18 and Tables 5, 6, and 7, it can be concluded that the proposed receiver can work almost all the corners for all the voltages with hysteresis.

Table 5. Amount of hysteresis (in volts) at the five corners for 0.9 V, 3.3 V, and 5 V.

	FF	FS	TT	SS	SF
0.9 V	0.344	*NC	0.37	0.389	0.303
3.3 V	0.892	1.07	1.045	1.176	0.995
5 V	0.828	1.002	1.06	1.131	0.951

*NC = not created

Table 6. N_{ML} in volts at the five corners for 0.9 V, 3.3 V, and 5 V.

	FF	FS	TT	SS	SF
0.9 V	0.477	X	0.474	0.474	0.532
3.3 V	1.323	1.23	1.285	1.26	1.343
5 V	1.345	1.248	1.3	1.271	1.358

Table 7. N_{MH} in volts at the five corners for 0.9 V, 3.3 V, and 5 V.

	FF	FS	TT	SS	SF
0.9 V	0.767	X	0.796	0.815	0.671
3.3 V	2.869	3.14	3.06	3.216	2.952
5 V	4.483	4.754	4.76	4.86	4.593

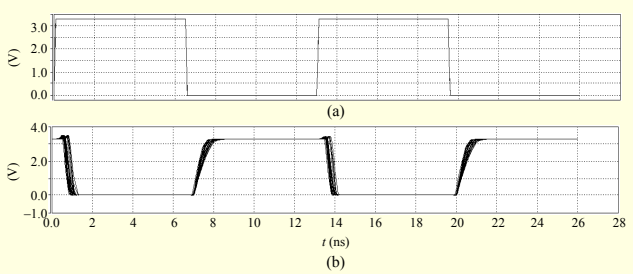

Fig. 19. (a) Input voltage at pad (0 V to 3.3 V) and (b) output waveforms for different process conditions.

6. Monte Carlo Analysis

Monte Carlo analysis is conducted on the proposed input receiver to check the robustness of the circuit by changing different process parameters, such as oxide thickness, threshold voltage, and so on. The resulting waveform for the 3.3 V operation is shown in Fig. 19.

Clearly, the proposed input receiver works well at different

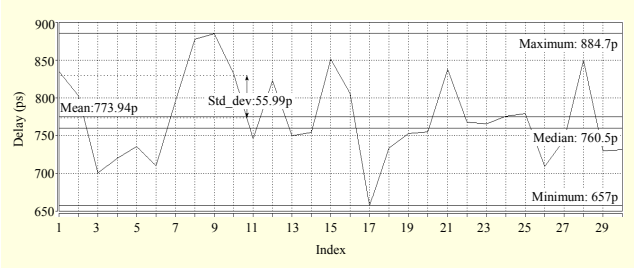

Fig. 20. Variation in delay, obtained from Fig. 19.

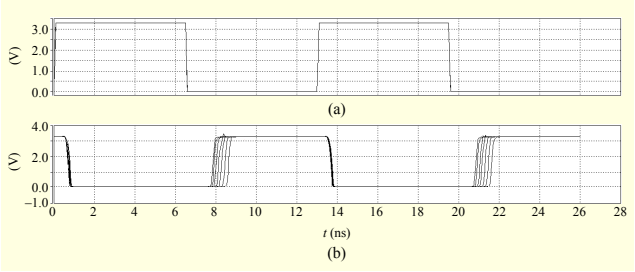

Fig. 21. (a) Input voltage (0 V to 3.3 V) and (b) output waveforms for different channel length of MOSFET.

process conditions at 3.3 V. For a proper Monte Carlo simulation, 30 iterations are made. As shown in Fig. 19, there is a variation in delay. A plot of the resultant variation in delay is shown in Fig. 20. From Fig. 20, it can be seen that the mean of variation in delay is 773.94 ps, the standard deviation is 55.99 ps, and the median is 760.5 ps. DC simulation is conducted, and the values obtained from that simulation are N_{MH} (mean) = 2.302 V and standard deviation = 0.16 V and N_{ML} (mean) = 1.5354 V and standard deviation = 0.0861 V.

7. Input Loading Effect

The input loading effect is the effect caused by the input pad. The input pad can have a capacitive loading effect. However, this does not affect the receiver output voltage in any way. The reason is that the first stage CMOS inverter has a high input impedance. The capacitive load of the input pad cannot have any influence because of the gate isolation of the first stage inverter, an effect verified by simulating the receiver at every voltage after connecting a load capacitance value of 10 pF to the pad. There is no change of any parameter in either transient or DC domain.

8. Channel Length Variation

The channel length of every MOSFET in the proposed receiver is varied from 335 nm to 365 nm, and the circuit is simulated at 3.3 V. Figure 21 shows the time domain waveforms. As shown in Fig. 21, the rise of the output voltage has more variation in effect and delay than does the fall of the output voltage. This is because of the strong pull down of the receiver at 3.3 V. A variation in delay is obtained for both the rise and fall transitions. Figure 22 shows the variation in delay for the rise transitions, and Fig. 23 shows the variation in delay for the fall transitions.

DC simulation is conducted for channel length variation at 3.3 V. The resultant waveforms are shown in Fig. 24. Here, the output voltage is along the Y axis and the input voltage is along the X axis. In Fig. 24, variations can be seen, but hysteresis exists for every channel length; the graph reflects a shift toward the left with an increase in channel length. So, N_{MH} increases

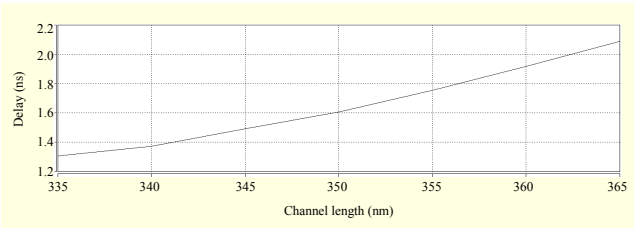

Fig. 22. Variation in delay for rise transitions of output voltage.

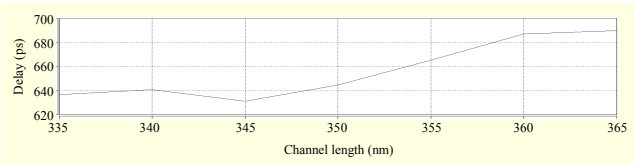

Fig. 23. Variation in delay for fall transitions of output voltage.

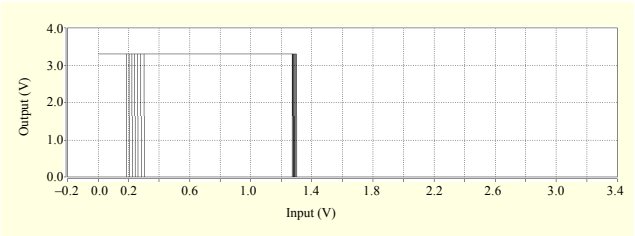

Fig. 24. Hysteresis characteristics for different channel lengths of MOSFET (335 nm to 365 nm).

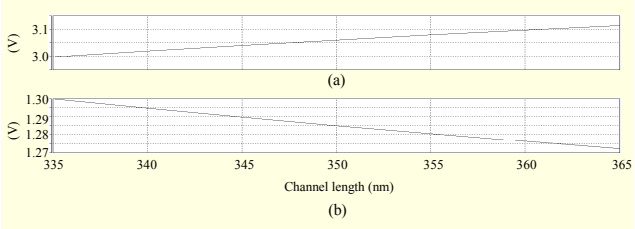

Fig. 25. (a) N_{MH} variation and (b) N_{ML} variation with change in channel length.

because it is the difference ($V_{DD} - V_{IH}$), and N_{ML} decreases because it is the same as V_{IL} (as $V_{OL} = 0$). The resultant waveforms are shown in Fig. 25.

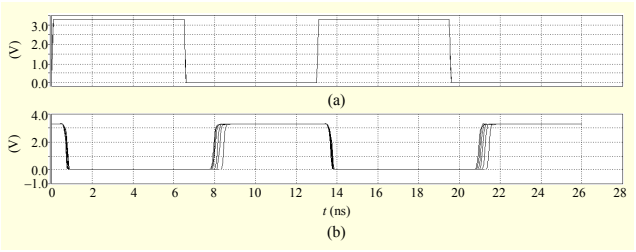

Fig. 26. (a) Input voltage (0 V to 3.3 V) and (b) output waveforms at different temperatures (0ºC to 75ºC range).

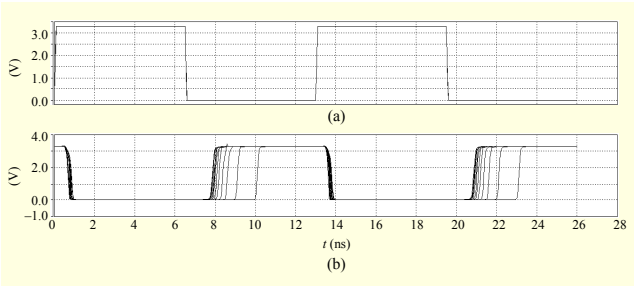

Fig. 27. (a) Input voltage (0 V to 3.3 V) and (b) output waveforms at different temperatures (–40ºC to 125ºC range).

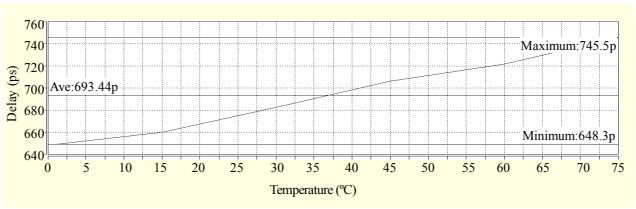

Fig. 28. Delay variation for 0ºC to 75ºC temperature range.

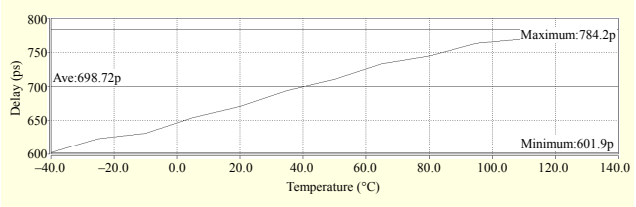

Fig. 29. Delay variation for –40ºC to 125ºC temperature range.

The reason for the phenomenon shown in Fig. 25 is that both NMOS and PMOS grow weaker (due to an increase in channel resistance) when the channel length increases. On the contrary, the pull down becomes stronger. In other words, the pull down happens more quickly. However, regarding pulling up, PMOS requires more change in the input voltage level. The input voltage level must be lower than the previous value so that the circuit can pull up for the output. This is why both transitions shift toward the left.

9. Circuit Temperature Variation

When the circuit operates, there is power dissipation in the form of heat. To study this effect, the circuit operation is simulated for different temperatures. Generally, the circuit may have to work within the 0ºC to 75ºC range for consumer electronics and within the –40ºC to 125ºC range for car electronics. As such, the circuit is simulated for both the ranges. The resulting time domain waveforms are shown in Figs. 26 and 27.

From Figs. 26 and 27, it can be seen that the proposed receiver works for both temperature ranges. The delay associated with the larger temperature range is obviously more than that for the shorter temperature range. The rise delays of the output waveforms are larger than the fall delays of the output waveforms. The reason is the same as that discussed in subsection III.8. The variations in delay for the 0ºC to 75ºC range and for the –40ºC to 125ºC range are shown in Figs. 28 and 29, respectively. In each figure, only the rise delays are indicated, as they are larger than the fall delays. From both figures, it is evident that the delay increases with an increase in temperature, which is due to the degradation in mobility resulting from the increase in temperature.

Table 8. Comparison with prior works.

	Conventional receiver [5]	Receiver reported in [19], [20]	Proposed receiver
Voltage range	1.8 V - 5 V	0.9 V - 5 V	0.9 V - 5 V
Technology	0.35 µm	0.35 µm	0.35 µm
V_{DD}	3.3 V	3.3 V	3.3 V
Amount of hysteresis	X	X	1.045 V
N_{ML}	0.7165 V	0.128 V	1.285 V
N_{MH}	1.15 V	2.3 V	3.06 V
Max. freq. of operation	80 MHz	50 MHz	500 MHz
Avg. power dissipation	15.5 mW	16.15 mW	9.2 mW

10. Reliability Consideration

As the node voltages are always less than 3.3 V, the gate oxide is not overstressed in the proposed receiver, which uses 0.35-µm 3.3-V devices. As the absolute values at the different terminals of the devices never cross 3.3 V, the junction voltage difference of any junction cannot cross the 3.3 V level. Thus, neither a junction breakdown nor a hot carrier effect can occur. Therefore, neither the lifetime of the device nor the lifetime of the circuit decreases rapidly. Even at the 5-V input voltage level, the npass transistor protects the gate by passing only ($V_{CC} - V_{tn}$) to the gate of the first inverter stage, where $V_{CC} = 3.3$ V and V_{tn} is the threshold voltage of NMOS. This means that the whole circuit operation is reliable for all voltage levels. Table 8 shows

a specification comparison of the proposed design with those of prior works.

In [5], [19], and [20], only voltage range, technology, and V_{DD} were clearly reported. The rest of the data comes from the simulation of those circuits produced in this study. Those values might have been different when the authors of those papers did their simulation, but, indeed, the above table represents values that are quite representative. Again none of those papers' objectives were to design a receiver that only has high noise immunity. So, noise considerations were totally absent in those papers. The average power value in this work is without the comparator portion. Clearly, the proposed design only supports hysteresis and therefore higher noise immunity. The data is given for the 3.3-V input voltage level condition for all circuits.

IV. Conclusion

An input receiver using 0.35-µm CMOS technology that can work at the following voltage levels was proposed: 0.9 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V. The frequency of operation was high for different voltage levels. In fact, 500 MHz is higher than any other receiver circuit frequency reported before now. As discussed in this paper, the whole circuit operation of the proposed input receiver is reliable. The noise margin at different voltage levels was high compared to those of input receivers reported in [5], [19], and [20]. The noise immunity was higher because of its hysteresis characteristic. Therefore, the false reception of the logic level in the core was minimized. The proposed input receiver ends the need for a separate Schmitt trigger and input buffer. It combines both in a single circuit. As such, the overall required area is less compared to the total area of the Schmitt trigger and input buffer (which may include a level-down converter). The proposed circuit uses only thin oxide devices, which results in a low processing cost compared to that of a dual oxide process. Monte Carlo analysis at different voltage levels was conducted. Results showed that the proposed receiver works well in different process conditions and at different voltage levels. Time domain and DC domain corner analysis at five process corners was conducted and showed that the proposed receiver works on most of the process corners. The channel length and circuit temperature were varied, and the proposed circuit proved to work under the different conditions.

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