Reverse-Conducting IGBT Using MEMS Technology on the Wafer Back Side

Jongil Won, Jin Gun Koo, Taepok Rhee, Hyung-Seog Oh, and Jin Ho Lee

In this paper, we present a 600-V reverse conducting insulated gate bipolar transistor (RC-IGBT) for soft and hard switching applications, such as general purpose inverters. The newly developed RC-IGBT uses the deep reactive-ion etching trench technology without the thin wafer process technology. Therefore, a freewheeling diode (FWD) is monolithically integrated in an IGBT chip. The proposed RC-IGBT operates as an IGBT in forward conducting mode and as an FWD in reverse conducting mode. Also, to avoid the destructive failure of the gate oxide under the surge current and abnormal conditions, a protective Zener diode is successfully integrated in the gate electrode without compromising the operation performance of the IGBT.

Keywords: IGBT, FWD, reverse conduction, RIE, Zener diode.

I. Introduction

The insulated gate bipolar transistor (IGBT) is widely used as a high voltage semiconductor device for general purpose inverters and motor drivers because it has desirable characteristics for high forward blocking voltage and on-state voltage drop. Much attention has been focused on the development of low cost, small, and highly reliable IGBTs, which show low loss in terms of both the on-state and the off-state. However, it has weak turn-off switching characteristics compared to those of power MOSFETs [1]-[3]. A freewheeling diode (FWD) is needed to conduct reverse operations in many switching applications and is usually used in externally anti-parallel devices with two chips in a package. A further development on the basis of the IGBT is the integration of a reverse diode into the IGBT structure, that is, a reverse conducting IGBT (RC-IGBT). The concept of an RC-IGBT in a productive volume was first realized with an optimization for lamp ballast applications. These RC-IGBTs combine a low saturation voltage and low switching losses of the IGBT [4]-[6]. As the IGBT and FWD are integrated into a monolithic chip, the total chip size, the testing cost, and the package cost are reduced. This also improves the reliability of the power modules due to the parasitic effects brought about by the bonding wires between the IGBT and FWD chips. However, because the RC-IGBT has a thin wafer (< 70 μm), the wafer processing of the back side on the collector side is very difficult. Using a thin wafer, the RC-IGBT needs the ability to handle such processing steps as implantation, annealing, back side metallization, and the front side lithographic and etching process that is necessary when the wafers are already thinned [7]. Thus, the fabrication of RC-IGBT is complex and costly for the requirement of a back side process [8].

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In this paper, the deep reactive-ion etching (RIE) trench technology that does not require a thin wafer process is utilized to overcome the aforementioned problems encountered in the RC-IGBT. Also, a Zener diode is integrated in our RC-IGBT to prevent the destructive failure of the gate oxide. Therefore, an RC-IGBT structure with an FWD and a protective Zener diode is proposed and demonstrated.

II. Device Structure and Fabrication

1. Proposed Device Structure

Figure 1 shows a cross-sectional view and equivalent circuit of the proposed RC-IGBT with a monolithic FWD and a protective Zener diode. Unlike the conventional RC-IGBT, the proposed RC-IGBT features an easy back side process that does not use a thin wafer. The protective Zener diode is inserted into the electrode between the gate and the emitter.

The reverse and forward conduction states of the proposed device are as follows. The N+ buffer layer/N-drift acts as a cathode (collector of IGBT) of the diode, and the P-body/P+ acts as an anode (emitter of IGBT) of the diode. When the polarity of the collector-emitter voltage is reverse biased, the electrons are provided by the N+ buffer layer electrode at the cathode of the diode, and holes are injected from the P+ electrode at the anode of diode to the N-drift. The junction between the P-body and N-drift becomes forward biased, and it behaves like an FWD, as reflected by Path 1 in Fig. 1(b).

During the forward conduction state of the device, an N-type channel forms due to the gate being forward biased and the electron current beginning to flow from the N+ emitter via the channel to the N+ buffer collector (Path 2). Unlike the conventional IGBT, the RC-IGBT has an electron current path from the emitter to the collector, which means the electrons are no longer confined in the N-drift or N+ buffer. This phenomenon leads to a decay of the minority carrier injection (holes) and conductivity modulation in the N-drift region. It contributes to the snapback characteristic. As the collector voltage becomes higher and when the electron current is large enough, the collector-based junction of the PNP is biased in the forward direction by potential in the P+ substrate/N+ buffer region. Then, the electron current serves as the base drive current for the PNP (Path 3). It induces the injection of the hole current from P+ substrate to N+ buffer (Path 4). The conductivity modulation occurs and improves because of the high level injection of the minority carrier. The IGBT turns on [6]. Consequently, current flow occurs from the collector to the emitter with a component of PNP and MOSFET currents. Also, as shown in Fig. 1, the protective Zener diode is placed between the gate and emitter electrode. The Zener diode is used to protect the gate oxide when a voltage spike and surge current occurs at the gate.

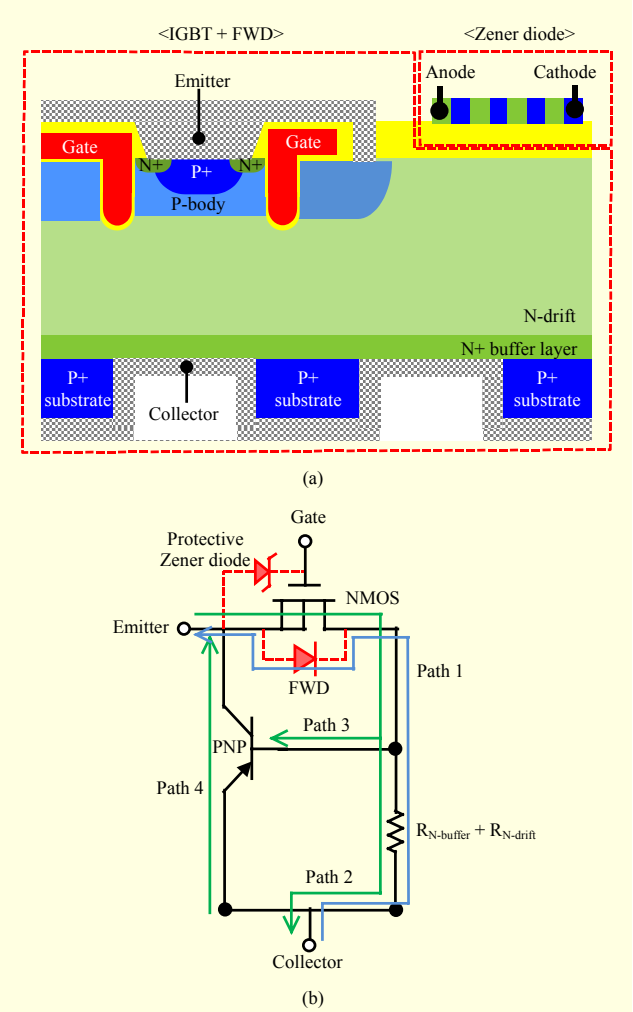

Fig. 1. (a) Cross-sectional view and (b) equivalent circuit of proposed RC-IGBT. Integrated FWD is formed in P+ emitter, P-body, and N+ buffer layer. Protective Zener diode is located in between gate and emitter electrode of IGBT.

2. Device Fabrication

The processes of the proposed device are equal to the normal trench IGBT process and include seven photomasks except for the back side process. The starting material is a double epitaxial layer (N+ buffer layer, N-drift) grown on a heavily doped P+ substrate. An adequate starting material is chosen for a forward blocking ability of over 600 V. A summary of the key front process steps is as follows: 1) trench process; 2) gate and P-body formation; 3) P+ and N+ formation in IGBT emitter region; 4) contact and front metal; 5) back side process. In general, the back side process of the RC-IGBT is that a highly

resistive substrate with a processed front side is grinded to a thickness of about 70 µm, and additional P-/N-doped layers are implanted on the back side of the wafer after photomask patterning. This method of processing is very difficult, and the back side processing costs are high.

We could approach the back side process in another way, and a key process is as follows. The wafer with a processed front side is grinded to a thickness of about 250 µm, and an additional N-doped layer is etched on the back side after photomask patterning. The back side etching is created by deep RIE in the MEMS technology through a photoresist mask of the 8-µm thickness. The summary of the key back side process step of the proposed device and SEM cross-section images of the back side deep etching are shown in Figs. 2 and 3, respectively.

As shown in Fig. 1, the protective Zener diode embedded in the proposed device is connected between the gate and emitter to protect the destructive failure of the gate oxide. It is located under the gate pad metal area, which does not change the electrical characteristics of the proposed device, nor is its size increased. It is composed of ten devices based on the poly silicon with a serial connection. The P+ and N+ are implanted on the un-doped poly silicon after the gate patterning of the IGBT. The P+/N+ implantation of the Zener diode is fabricated during the process of the IGBT P+/N+ emitter. It requires no extra photomasking step or implantation process.

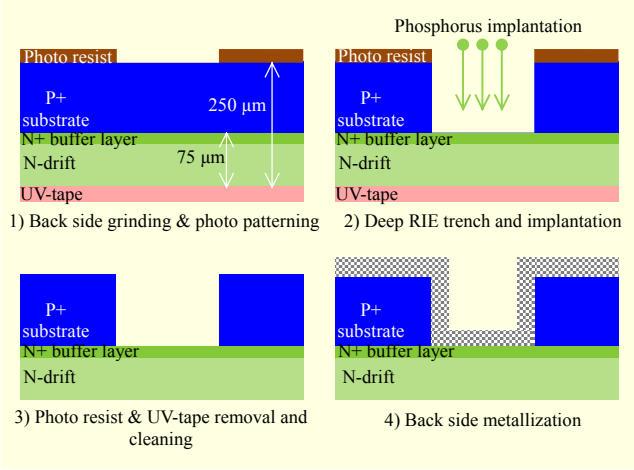

Fig. 2. Back side process step of proposed RC-IGBT.

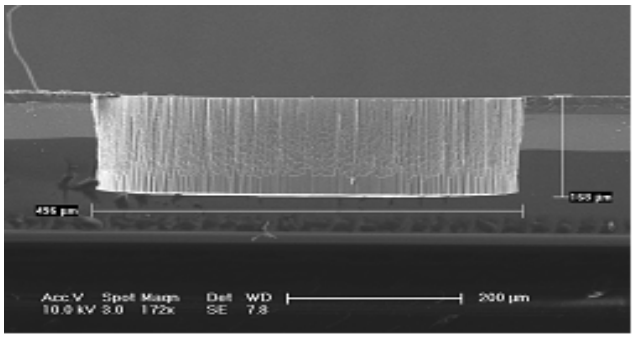

Fig. 3. SEM cross-sectional view of back side deep trench. Total wafer thickness is set to 250 µm. Trench depth is 180 µm; trench pitch is 400 µm. Trench depth is brought to focus upon N+ buffer layer position. Residual thickness of wafer is 75 µm after deep trench process.

III. Experiment Results

The proposed RC-IGBT is fabricated the same way a conventional punch-through IGBT (PT-IGBT) is fabricated, and their electrical characteristics are compared. The electrical characteristics (forward blocking voltage, forward conducting characteristics, threshold voltage, reverse conducting characteristics, switching performance, protective Zener diode characteristics, and so on) of the conventional device and the proposed device are measured with a 370 Curve Tracer, a 4156 Semiconductor Parameter Analyzer, and a 5300HX Semiconductor Tester.

1. Forward Blocking Voltage

Both the conventional device and the proposed device are based on the 600-V PT-IGBT with a thickness and N-drift resistivity of 65 µm and 18 Ω-cm, respectively. In addition, the thickness and resistivity of the N+ buffer layer is 10 µm and 0.03 Ω-cm, respectively. Also, to overcome the electric field crowing effect at the periphery junction of the device, the multiple field limit rings are designed to improve the blocking voltage. The field limit rings each have a width of 3 µm, and the number of rings is 11. The total width of the field limit rings

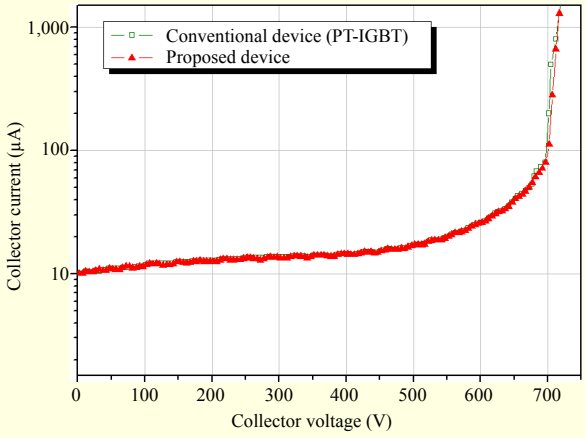

Fig. 4. Forward blocking voltage of proposed and conventional devices at gate voltage $V_g = 0$ V in forward conducting state. Leakage current of devices is below 30 µA at 600 V of collector voltage.

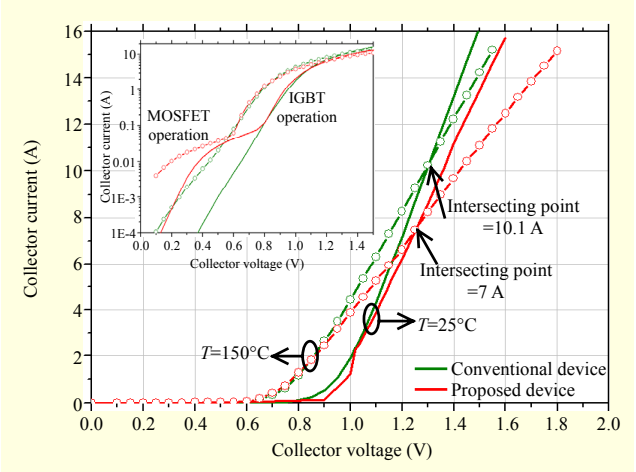

Fig. 5. Forward conducting characteristics of proposed and conventional devices at gate voltage $V_g = 15$ V with different temperatures. To distinguish between MOSFET and IGBT operations of proposed device, log scale figure is inserted.

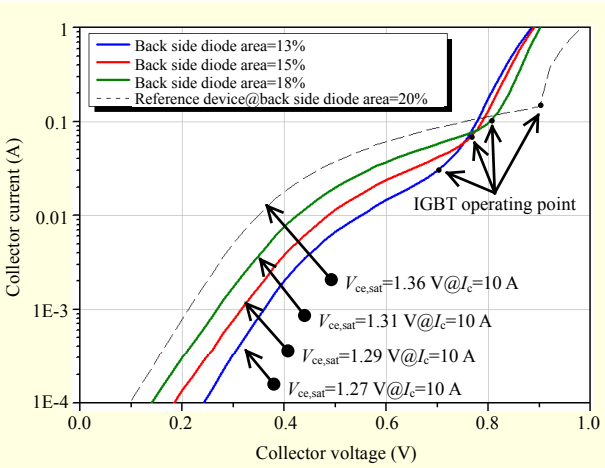

Fig. 6. Dependence of forward conducting characteristics of proposed device in FWD area.

is less than 150 μm. Figure 4 shows the measured forward blocking characteristics of the conventional device and the proposed device. The conventional device and the proposed device each have a forward blocking voltage of 710 V.

2. Forward Conducting Characteristics

Figure 5 depicts the forward conducting characteristics of the proposed and conventional devices at the room (25ºC) and high temperature (150ºC). The collector to emitter saturation voltage ($V_{ce,sat}$) is 1.25 V for the conventional IGBT and 1.36 V for the proposed IGBT at the room temperature. At the high temperature, the saturation voltage of the conventional device is equal to the saturation voltage of the proposed device at the room temperature, and the proposed device is increased to 1.43 V. As depicted in Fig. 5, the conventional and proposed devices have either positive or negative temperature coefficients at the intersecting point. The intersecting point of the devices in conjunction with temperature coefficients reveal 10.1 A for the conventional device and 7 A for the proposed device. The main reason for this characteristic is the different influence of the back side diode characteristics. The proposed device has lower performance than the conventional device at the high temperature because the temperature coefficient of the proposed device has a more positive characteristic than that of the conventional device. However, it ensures desirable current sharing within the chip as well as when chips are paralleled to handle larger current [2].

Also, unlike the conventional device, the proposed device shows weak snapback characteristics. In the low current mode (MOSFET operating mode), the N+ buffer layer of the proposed device provides an electron current path. The P+ substrate/N+ buffer layer junction remains negative biased unless the electron current is large enough. The snapback characteristics depend on the electron current density, which is concerned with the monolithic FWD area. To analyze the electrical tendency of the proposed device in the FWD area, forward conducting characteristics are investigated, as shown in Fig. 6.

As the FWD area increases, the electron current increases. Then, the electron current prevents a minority carrier injection from the P+ substrate (collector), which leads to an IGBT operation delay. As a result, the IGBT operating voltage (move point from MOSFET operation to IGBT operation) and the forward saturation voltage increase. The dependence of the forward conduction characteristics in the diode area shows that RC-IGBT switching applications can be determined by the FWD area.

3. Reverse Conducting Characteristics

Figure 7 depicts the reverse conducting characteristics of the conventional device and the proposed device with a reverse bias. The reverse conducting voltage of the proposed device is 3.5 V at the reverse conducting current 1 A. When a reverse conducting state is applied to the proposed device, the P+ substrate/N+ buffer layer junction becomes forward biased. Its reverse conducting characteristics are nearly the same as a general diode except for a higher built-in potential voltage. On the other hand, in the case of the conventional device, the P+ substrate/N+ buffer layer junction becomes reverse biased and is limited by the avalanche breakdown. Also, we investigate the reverse conducting characteristics in the FWD area (Fig. 8).

By decreasing the FWD area, the forward voltage of the

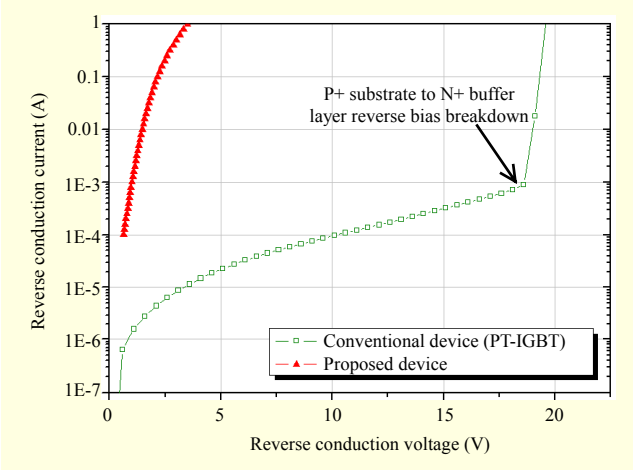

Fig. 7. Reverse conducting characteristics of conventional and proposed device in reverse operating mode.

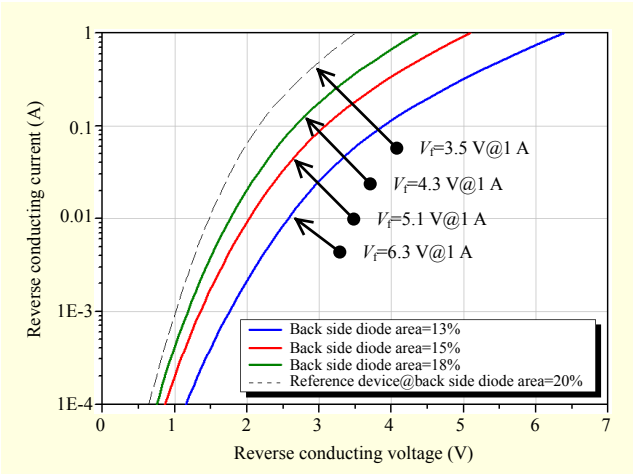

Fig. 8. Dependence of reverse conducting characteristics of proposed device in FWD area.

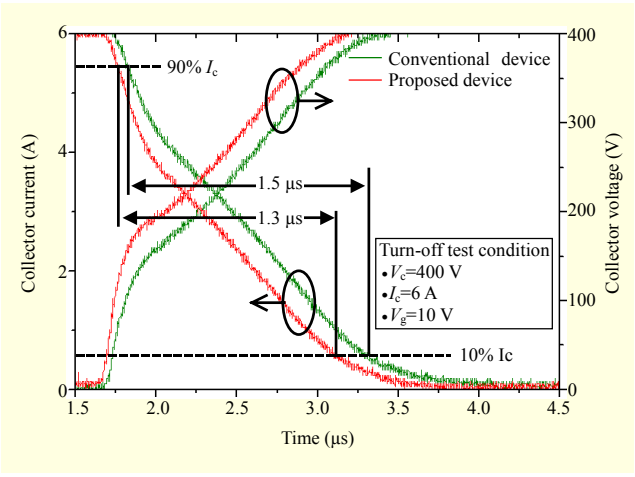

Fig. 9. Switching waveforms (turn-off current and voltage) of proposed and conventional devices.

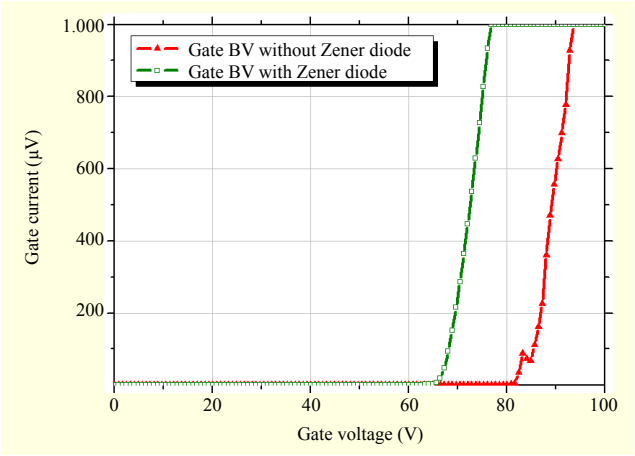

Fig. 10. Measured gate oxide breakdown characteristics with/ without protective Zener diode.

diode is elevated in the reverse conducting state. The diode area has a significant influence on the reverse conducting state.

4. Turn-Off Characteristics

The switching waveforms in the inductive load of the conventional device and the proposed device are shown in Fig. 9. In the turn-off measurements, the devices are turned off at the forward conduction current of 6 A and blocking voltage of 400 V. The turn-off time of the conventional device and the proposed device is 1.5 μs and 1.3 μs, respectively. The proposed device decreases by 13% compared with that of the conventional device, so its turn-off loss is lower.

5. Protective Zener Diode Characteristics

Figure 10 shows the *I-V* characteristics of the proposed device with and without the Zener diode. The 10-series of the protective Zener diodes is constructed with polysilicon and has about 60 V of Zener breakdown voltage (BV). The gate oxide thickness of the proposed device is 1,000 Å, and the BV of the gate oxide is about 80 V. When an over-voltage or surge current occurs in the gate electrode, the protective Zener diode is activated to protect against a breakdown of the gate oxide. Therefore, the Zener BV must be smaller than the gate oxide BV of the IGBT.

IV. Conclusion

In this paper, we proposed a 600-V RC-IGBT for soft and hard switching application that includes a protective Zener diode. The newly developed RC-IGBT using deep RIE trench technology does not require thin wafer handling. Nevertheless, an FWD was monolithically integrated into an IGBT chip. A

Table 1. Summary of experiment results.

Device	Wafer thickness	Forward blocking voltage	Forward conducting voltage	Turn-off time
Conventional device	250 μm	710 V	1.25 V@25℃ 1.25 V@150℃	1.5 μs
Proposed device	250 μm		1.36 V@25℃ 1.43 V@150℃	1.3 μs
RC-IGBT with thin wafer [9]	70 μm	600 V	1.45 V@25℃ 1.7 V@150℃	0.145 μs

fabricated RC-IGBT was verified and compared to a conventional device (PT-IGBT). The electrical characteristics of the conventional device, the proposed device, and an additional RC-IGBT with a thin wafer [9] are summarized in Table 1. Results of the comparison show that the proposed device has lower forward conducting loss but a much higher turn-off time. However, we confirmed that the proposed device can be processed without a thin wafer and makes for a low-cost fabrication technique for switching applications. We aim to further improve performance of the proposed device with a higher turn-off time using an optimized back side diode area and additional lifetime killing technique in the near future.

Additionally, to avoid gate oxide destruction, protective Zener diodes were successfully integrated between the gate and emitter electrode without an additional photomasking step, compromising the operation performance of the IGBT. As a result, the proposed device was successfully demonstrated to have a higher reliability than the conventional device.

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