# Printed Organic One-Time Programmable ROM Array Using Anti-fuse Capacitor

Byung-Do Yang, Jae-Mun Oh, Hyeong-Ju Kang, Soon-Won Jung, Yong Suk Yang, and In-Kyu You

**This paper proposes printed organic one-time programmable read-only memory (PROM). The organic PROM cell consists of a capacitor and an organic p-type metal-oxide semiconductor (PMOS) transistor. Initially, all organic PROM cells with unbroken capacitors store "0." Some organic PROM cells are programmed to "1" by electrically breaking each capacitor with a high voltage. After the capacitor breaking, the current flowing through the PROM cell significantly increases. The memory data is read out by sensing the current in the PROM cell. 16-bit organic PROM cell arrays are fabricated with the printed organic PMOS transistor and capacitor process. The organic PROM cells are programmed with –50 V, and they are read out with –20 V. The area of the 16-bit organic PROM array is 70.6 mm$^2$.**

**Keywords: Anti-fuse, capacitor breaking, organic memory, printed electronics, programmable read-only memory (PROM).**

Manuscript received Nov. 28, 2012; revised Mar. 18, 2013; accepted Apr. 2, 2013.

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2012R1A1A4A01015759). This work was supported by the IT R&D program of MKE/KEIT (Grant No. 10041416, The core technology development of light and space adaptable new mode display for energy saving on 7inch and 2W) and development of new materials and solution process for LCD backplane funded by ISTK. The chip fabrication was supported by the IC Design Education Center (IDEC).

Byung-Do Yang (phone: +82 43 261 3583, bdyang@cbnu.ac.kr) and Jae-Mun Oh (ace157@cbnu.ac.kr) are with the Department of Electronics Engineering, Chungbuk National University, Cheongju, Rep. of Korea.

Hyeong-Ju Kang (hjkang@kut.ac.kr) is with the School of Computer Science & Engineering, Korea University of Technology and Education, Cheonan, Rep. of Korea.

Soon-Won Jung (jungsoonwon@etri.re.kr), Yong Suk Yang (jullios@etri.re.kr), and In-Kyu You (ikyou@etri.re.kr) are with the Components & Materials Research Laboratory, ETRI, Daejeon, Rep. of Korea.

http://dx.doi.org/10.4218/etrij.13.1912.0010

## I. Introduction

Printed organic electronics has become a new area for low-cost and flexible devices, such as flexible displays, smart sensors, and radio frequency identification (RFID) tags [1]-[3]. Recently, remarkable improvements have been achieved for low-cost, high-performance, and low-power printed organic devices [4], [5]. Most research focuses on the high-performance and low-voltage printed organic transistors, which are essential devices for the organic electronics [6]-[9]. Other research focuses on the organic nonvolatile memory that expands a wide variety of the applications of the organic electronics [4], [10]-[12].

Memory effects can be observed in organic capacitor, resistor, and transistor structures. Among these, the nonvolatile memory using a single transistor structure has gained considerable attention in recent years and has been embedded in integrated circuits [11], [13]. In the case of ferroelectric nonvolatile memory, it is hard to obtain long retention time from the devices because of the rough surface and high leakage current through the gate ferroelectric film [10], [13], [14]. Another approach to replacing leaky ferroelectrics is the development of metals [12] or nanoparticles (NPs) [15] as floating gates. However, the fabrication of the inorganic floating gates requires vacuum evaporation of metals or other complicated processes [12], [15], which are not compatible with low-cost manufacturing of organic memories.

In this paper, a printed organic one-time programmable read-only memory (PROM) array is proposed. Each organic PROM cell consists of an organic capacitor and an organic p-type metal-oxide semiconductor (PMOS) transistor. The PROM cell is selectively programmed by electrically breaking the capacitor with a high voltage. The capacitor breaking changes

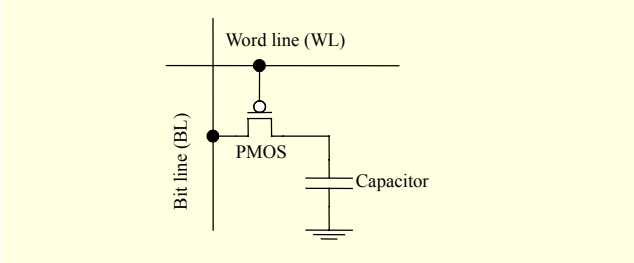



Fig. 1. Schematic of printed organic PROM cell.

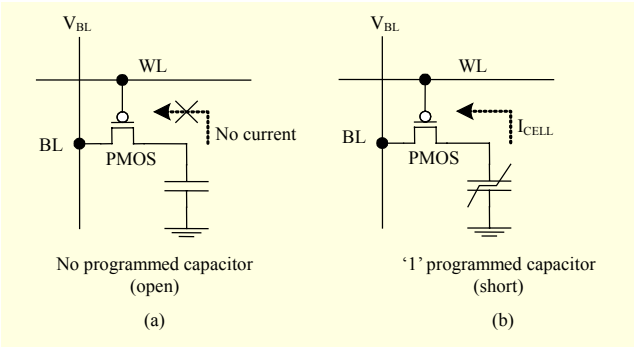



Fig. 2. (a) 0-programmed PROM cell and (b) 1-programmed PROM cell.

the capacitor permanently from being open to being short, and the data retention time of the PROM cell becomes infinite. Thus, we call the broken capacitor an anti-fuse capacitor.

The printed organic PROM is suitable for organic electronic devices requiring one-time programming, such as identification data, circuit trimming data, and look-up tables. Besides, if the number of write operations in the nonvolatile memory is strictly limited to a few numbers, the printed organic PROM can replace the nonvolatile memory by writing data in unused memory cells instead of overwriting data in previously used memory cells. The printed organic PROM can be an effective and inexpensive substitute for printed organic nonvolatile memory. However, the implemented 16-bit organic PROM is not small enough to be commercialized. More research on shrinking the printed organic transistor and capacitor is required.

The rest of the paper is organized as follows. Section II describes the proposed printed organic PROM. Section III shows the measurement results of the fabricated organic PROM arrays. Finally, the conclusion is drawn in section IV.

## II. Printed Organic PROM Array

### 1. Printed Organic PROM Cell

Figure 1 shows a schematic of the printed organic PROM cell consisting of an organic capacitor and an organic PMOS transistor. The PROM cell is selected by a word line (WL), and its data is written and read through a bit line (BL).

Initially, all capacitors in a printed organic PROM array are electrically open, as shown in Fig. 2(a). All PROM cells are 0-programmed PROM cells. During read operations, no current flows through the 0-programmed PROM cell when applying a read voltage to the BL. During write operations, some PROM cells are selectively programmed to "1" by applying a voltage over the breakdown voltage of the capacitor to the BL. In the 1-programmed PROM cells, their capacitors are broken and thus electrically shorted, as shown in Fig. 2(b). During read operations, cell current ($I_{CELL}$) flows in the 1-programmed PROM cell. A read-out circuit for the PROM

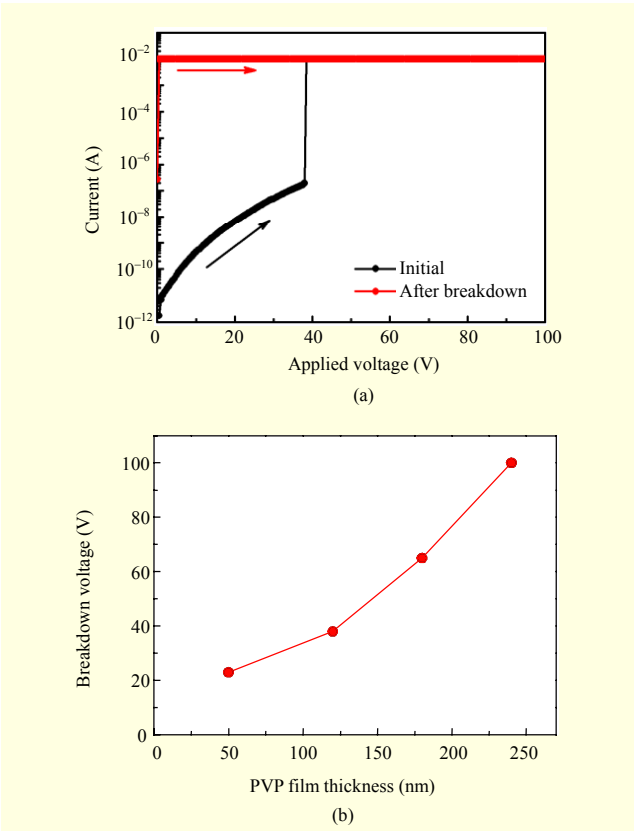



Fig. 3. (a) Measured leakage current of printed organic capacitor according to applied voltage and (b) measured breakdown voltage of printed organic capacitor according to PVP film thickness.

determines the stored data by detecting whether the cell current flows or not.

Figure 3(a) shows the measured leakage current of the printed organic capacitor according to its applied voltage. Initially, the capacitor has a very high resistance, so the leakage current is less than 0.1 μA until the applied voltage is under the breakdown voltage of the capacitor ($BV \approx 38$ V). The breakdown voltage changes according to the PVP film

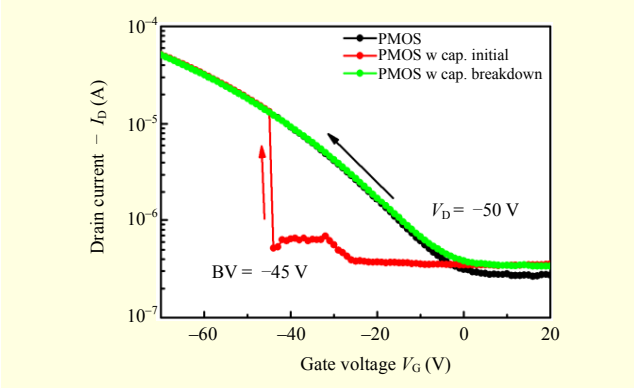



Fig. 4. Measured cell current of PROM cell.

thickness, as shown in Fig. 3(b). Over the breakdown voltage, the capacitor is broken and thus electrically shorted. However, the maximum of the measured leakage current is about 10 mA due to the limitation of the measurement equipment. The printed organic capacitor acts similarly to an anti-fuse capacitor, as it is initially open and then becomes permanently short by applying a high voltage, whereas the conventional fuse made of a metal line is initially short and then becomes permanently open by applying a high current.

Figure 4 shows the measured cell current ($I_D$) of the PROM cell according to the gate voltage ($V_G$), where the drain voltage ($V_D$) is –50 V. As shown in Fig. 1, the gate, drain, and source of the PMOS are connected to the WL, BL, and capacitor, respectively. Before the capacitor breaking, the source voltage ($V_S$) is equal to $V_G$+$V_{TP}$, where $V_{TP}$ is the absolute value of the threshold voltage of the PMOS, and $V_D$ is lower than $V_G$. The source voltage is applied to the capacitor. As a result, the voltage difference of the capacitor increases proportionally to the absolute value of $V_G$. Initially, the cell current ($I_D$) is much less than 1 μA, before $V_G$ reaches the voltage for breaking the capacitor ($BV$≈–45 V). After the capacitor breaking, the broken capacitor acts like a short circuit. Therefore, the drain current of the PMOS transistor with the broken capacitor ("PMOS w/cap. breakdown" in Fig. 4) is the same as that of the PMOS transistor without a capacitor ("PMOS" in Fig. 4) whose source is connected to the ground. The gate voltage ($V_G$) for breaking the capacitor is –45 V. Therefore, the writing and reading voltages are determined to be –50 V and –20 V, respectively. These voltages can be reduced by lowering the breakdown voltage of the capacitor, as shown in Fig. 3(b).

In the broken capacitor, the leakage current is over 10 mA when its applied voltage is 20 V, as shown in Fig. 3(a); therefore, its resistance is under 2 kΩ. In the PROM cell with the broken capacitor, the drain current is about 2 μA when $V_G$ is –20 V, so its resistance is about 1 MΩ. Therefore, the broken capacitor behaves like a short circuit in the PROM cell.

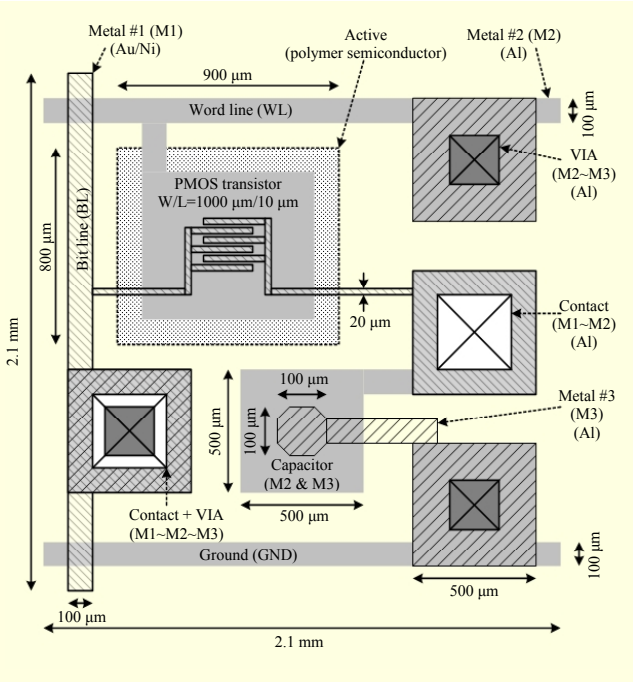



Fig. 5. Printed organic PROM cell layout.

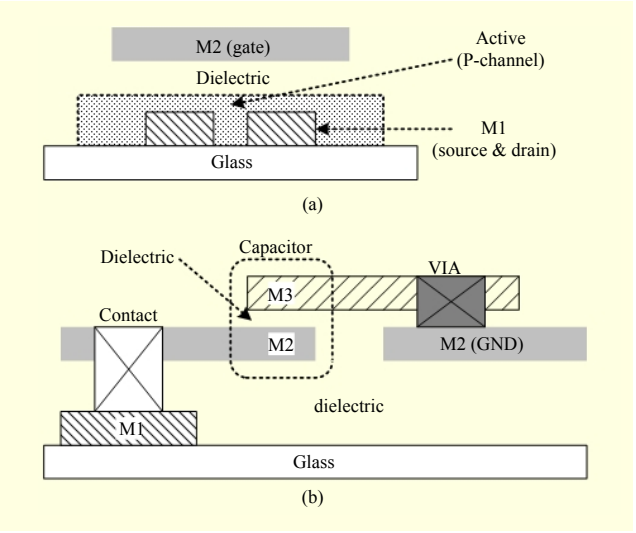



Fig. 6. Printed organic PROM cell structure: (a) cross-section of transistor and (b) cross-section of capacitor.

Figure 5 shows the layout of the printed organic PROM cell. All circuits are fabricated on glass. Three metal layers (M1 to M3) and an active layer, a contact, and a VIA are used to implement the PMOS transistor and capacitor. Two dielectric layers are used to separate the metal layers. Figure 6 illustrates the structure of the printed organic PROM cell, Fig. 6(a) showing a cross-section of the PMOS transistor and Fig. 6(b) showing a cross-section of the PMOS capacitor.

The M1 layer is used for the source and drain of the transistor and the BL. Au/Ni (15-nm/3-nm thick) is used for the

M1 layer by the lift-off technique on Corning Eagle 2000 glass substrates. The width of the metal lines for the source and drain is 20 μm. The width and length (*W*/*L*) of the channel of the transistor are 1,000 μm and 10 μm, respectively. The M2 layer is used for the gate of the transistor, the WL, the ground line, and the bottom plate of the capacitor. After inter-metallic dielectric deposition, the M3 layer is used for the top metal for the bonding wires and the top plate of the capacitor. The M2 and M3 layers are made of Al (50-nm thick) by the thermal evaporation method. These layers are patterned by the shadow mask process. The minimum width of the M2 and M3 layers is selected to be 100 μm.

The active layer for the PMOS transistor is patterned over the source and drain metal lines. A p-type polymer semiconductor containing dodecyl-substituted thienylenevinylene (TV) and dodecylthiophene (PC12TV12T) is synthesized using a previously published procedure [16]. This mixture is dissolved in anhydrous p-xylene to obtain 3 mg/ml of solution, and the solution is filtered through a 0.2-μm polytetrafluoroethylene (PTFE) syringe filter prior to use. A custom-built research inkjet printer (UJ200MF, Unijet, Korea) is utilized to inkjet-print the semiconductor solution onto Au/Ni patterned substrates at room temperature. A piezoelectric-type drop-on-demand dispensing head (Microfab Tech.) with a 50-μm orifice diameter is used at an operating frequency of 1 kHz. The semiconductor film is thermally annealed at 200°C for 30 minutes in a $N_2$-purged glove box with low oxygen and moisture levels (<5 ppm) [17]. For the polymer gate dielectric layers, PMMA (Aldrich, MW = 120 kD) is used without further purification. The PMMA (80 mg/mL) is dissolved in n-butylacetate (nBA) and filtered before spin-coating. After the dielectric coating, the devices are finally annealed at 80°C for one to two hours in the glove box.

The PVP material is selected as capacitor dielectric. To fabricate high performance top-gated polymer transistors, the selection of a benign gate dielectric solvent is quite important to avoid performance degradation via dissolution or swelling of a semiconducting polymer. The PVP can find a benign solvent easily since common conjugated polymers do not dissolve its fluorinated or alcoholic solvent. The orthogonal solvents selected for PMMA and PVP are nBA and 2-butanolas, respectively. The used conjugated polymers do not dissolve in these orthogonal solvents, and the roughness of semiconducting polymer films is almost similar after one minute of spin-coating.

The bottom and top layers of the capacitor are M2 and M3, respectively. To control the breakdown voltage precisely, we adjust the PVP concentration. In a capacitor, the PVP (10 mg/mL, 20 mg/mL, 30 mg/mL, and 40 mg/mL) is dissolved in 2-butanol, and the solution is filtered via a 0.2-μm PTFE syringe filter before being spin-coated at 2,000 rpm for one minute. After the dielectric coating, the devices are annealed at 100°C for an hour in a nitrogen environment glove box.

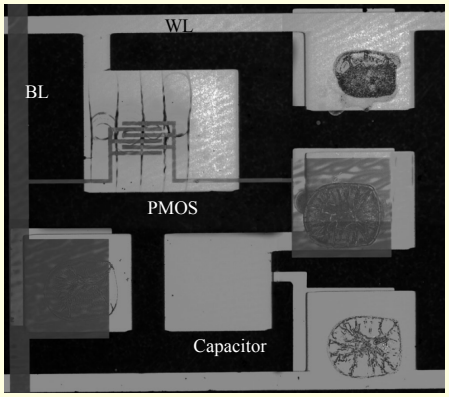



Fig. 7. Microphotograph of printed organic PROM cell.

The contact connects the M1 and M2 layers. After the PMMA gate dielectric film coating, pure solvent (anhydrous chlorobenzene) is inkjet-printed on a PMMA-coated device to make VIA holes. The VIA connects the M2 and M3 layers. After the PVP dielectric film coating, the 2-butanol solvent is inkjet-printed on a PVP-coated device to make VIA holes.

In the layout, the align margin for each layer is set to 100 μm. The total area of the printed organic PROM cell is 4.41 $mm^2$ (2.1 mm × 2.1 mm). The areas of the transistor, capacitor, contact, and VIA are shown in Fig. 5. Figure 7 shows a microphotograph of the printed organic PROM cell.

## 2. Operations of Printed Organic PROM Array

The printed organic PROM arrays with 4×4 cells are fabricated, as shown in Fig. 8. Four WLs (WL1 to WL4) and four BLs (BL1 to BL4) have their PADs for the bonding wires to connect the PROM test board. A WL with a negative voltage selects four PROM cells among 16 PROM cells. The selected four PROM cells are programmed and read out through four BLs.

Figure 9(a) shows the write operation in a PROM cell. The voltage of a selected WL becomes –50 V, and the other WLs remain at 0 V. The voltage of the BL ($V_{BL}$) varies according to program data. The BL supplies 0 V or –50 V to the capacitor in the PROM cell when the program data is "0" or "1," respectively. If $V_{BL}$ = 0 V, the capacitor remains electrically open. If $V_{BL}$ = –50 V, the capacitor is broken, and it changes to an electrically short circuit.

Figure 9(b) shows the read operation in a PROM cell. At this time, the voltage of the selected WL becomes –20 V, and the

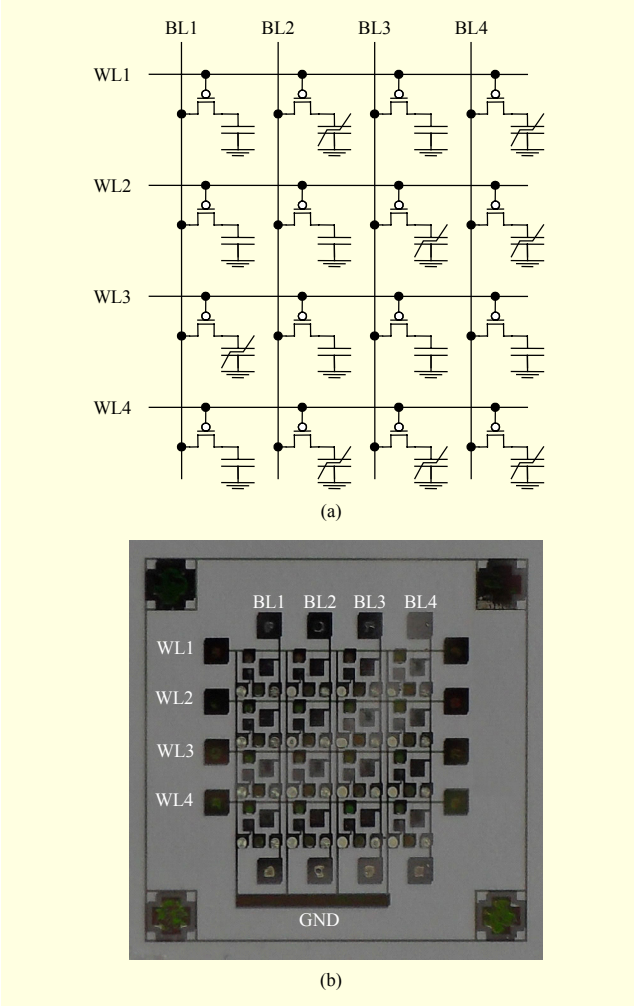



Fig. 8. Printed organic PROM array with 4×4 cells: (a) schematic and (b) microphotograph.

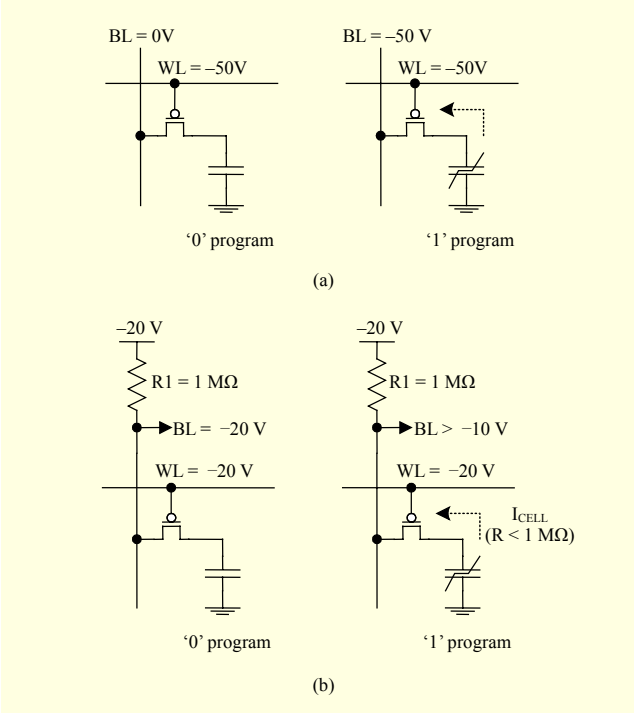



Fig. 9. PROM cell operations: (a) write and (b) read.

other WLs remain at 0 V. The BL is connected to –20 V through the resistor R1. If the program data is "0," $V_{BL}$ becomes –20 V because the capacitor is electrically open. If the program data is "1," $V_{BL}$ becomes –10 V due to the voltage division between the resistor R1 (=1 MΩ) and the resistance of 1-programmed PROM cell (≈1 MΩ). Therefore, the data stored in the PROM cell can be read out by comparing the BL voltage ($V_{BL}$ = –20 V or –10 V) and a reference voltage ($V_{REF}$ ≈ –15 V).

Figure 10 shows a schematic and a photo of the implemented PROM test board. The test board consists of a 16-bit PROM cell array board, a WL decoder, a read-write circuit, and a controller. The PROM cell array board has the printed organic PROM array with 4×4 cells, bonding wires, and test board connection pins. The WL decoder is made of five relay switches. A relay switch selects the WL voltage ($V_{WL}$) between the writing voltage ($V_{write}$ = –50 V) and the reading voltage ($V_{read}$ = –20 V) by a write enable signal (write_EN). Four relay switches connect the WLs (WL1 to WL4) to $V_{WL}$ or the ground by four WL enable signals (WL1_EN to WL4_EN). The read-write circuit has four BL read-write circuits. Each BL read-write circuit consists of two relay switches, an operation amplifier (AMP), and a resistor R1 (=1 MΩ). The read or write circuit is selected by the write_EN signal. The read circuit (AMP and R1) detects the programmed data in the PROM cell. The write circuit connects the BL to $V_{write}$ or 0 V by the BL program signal (BL_program). The controller makes 5 V control signals for all relay switches.

Figure 11 shows the signal waveforms of the PROM test board. Two operation modes (read and write) are controlled by the write enable signal (write_EN). Four WLs (WL1 to WL4) are selected by the WL enable signals (WL1_EN to WL4_EN). At the read operation before the write operation, all capacitors in the PROM cells are unbroken, and the value of the data is "0." Therefore, the voltage of BL1 is –20 V and the output voltage of the operational amplifier (OUT1) is also –20 V. At the write operation, the PROM cells are sequentially programmed by changing the selected WLs. The voltage of BL1 becomes 0 V or –50 V according to the program data ("0" or "1"). In this example, four-bit data "1011" is programmed. At the read operation after the write operation, the stored data "1011" is read out. The voltage of BL1 becomes –20 V or –10 V according to the program data ("0" or "1"). The outputs of the operational amplifier (OUT1) become "1011."

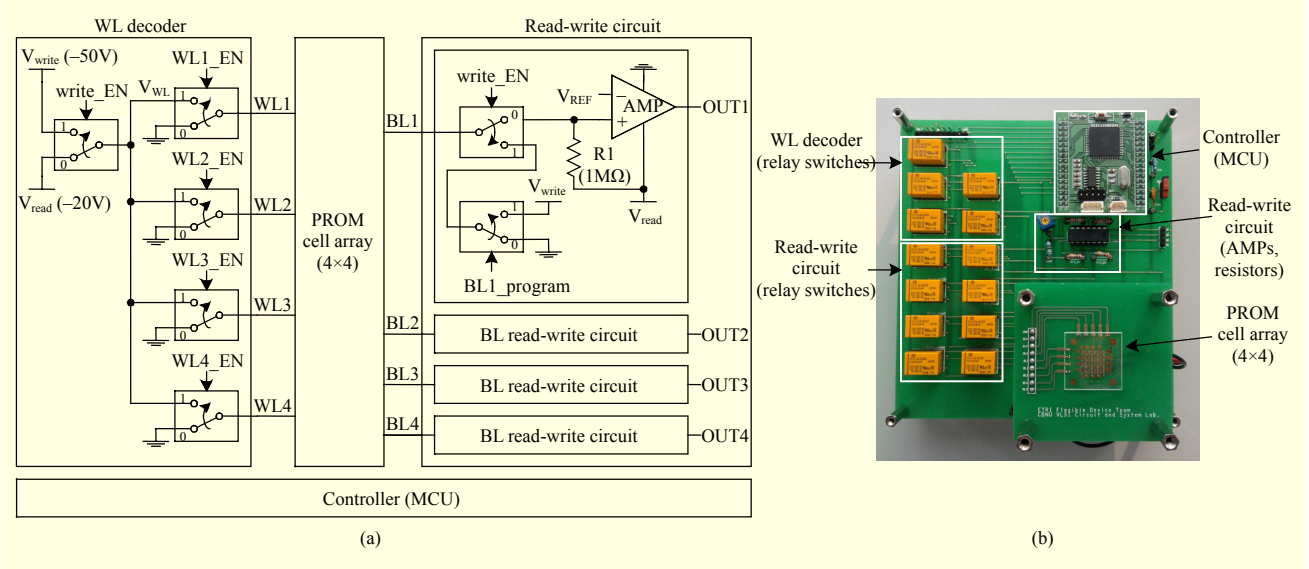



Fig. 10. PROM test board: (a) schematic and (b) photo.

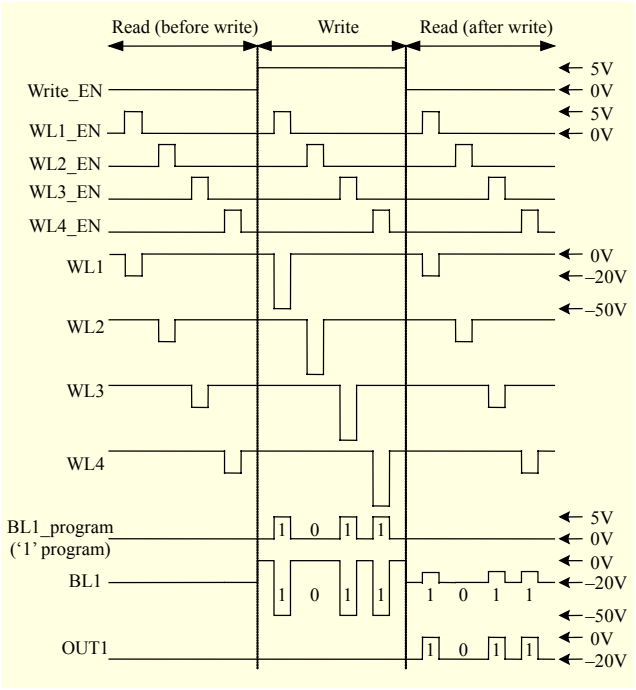



Fig. 11. Signal waveforms of PROM test board.

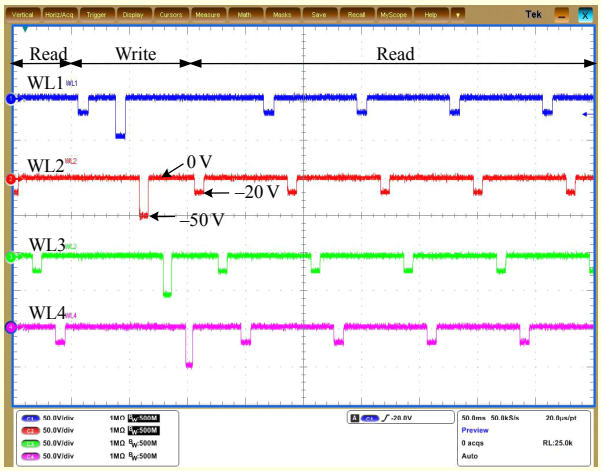
## III. Measurement Results

Figure 12 shows the measured waveforms of the PROM test board. The four WLs shown in Fig. 12(a) are sequentially activated with –20 V ($V_{read}$) and –50 V ($V_{write}$) at the read and write modes, respectively. Figures 12(b) and 12(c) show voltages of the BL and OUT, where the program data is "1000" and "1010," respectively. At the read operation before the write operation, the stored data is "0000." At the read operation after the write operation, the programmed data is accessed. The voltage of the BL is about –10 V instead of –20 V ($V_{read}$), when data is "0." The voltage change in the BL comes from the resistance of the oscilloscope probe ($R_{probe}$=1 MΩ). The BL voltage becomes –10 V from –20 V due to the voltage division between R1 (1 MΩ), shown in Fig. 9(b), and the probe resistance (≈1 MΩ). The BL voltage varies from –2 V to –5.5 V in Figs. 12(b) and 12(c), because the 1-programmed cells have a wide range of resistances. However, as shown in Figs. 12(b) and 12(c), the output voltage of the operational amplifier (OUT) becomes 0 V or –20 V ($V_{read}$) according to the programmed data.

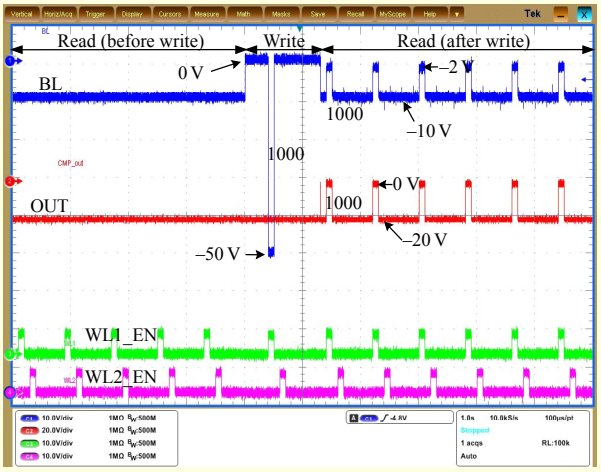
The features of the printed organic PROM array are summarized in Table 1. The printed organic PROM array with 16-bit PROM cells is implemented with the printed organic PMOS transistor and capacitor process. The breakdown voltages are –47 V to –40 V for 10 samples of the PROM cells. The 0-programmed and 1-programmed cells have the leakage currents of 0.1 μA to 0.4 μA and 1.5 μA to 10.5 μA, respectively. The writing and reading voltages are –50 V and –20 V, respectively. The area of the PROM cell is 4.41 $mm^2$. The areas of 16-bit ROM arrays with and without PADs are 132 $mm^2$ and 70.6 $mm^2$, respectively.

## IV. Conclusion

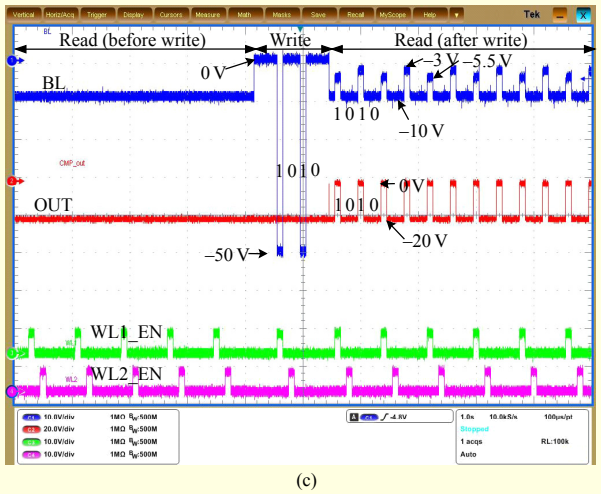
Printed organic one-time PROM was proposed. The organic PROM cell consists of a capacitor and an organic PMOS transistor. In this study, initially, all organic PROM cells with unbroken capacitors stored "0." Some organic PROM cells were programmed to "1" by electrically breaking the capacitors




(a)




(b)




(c)

Fig. 12. Measured waveforms of PROM test board: (a) WLs, (b) when PROM data is "1000,"and (c) when PROM data is "1010."

with a high voltage. After the capacitor breaking, the current flowing through the PROM cell significantly increased. The memory data was read out by sensing the current in the PROM cell. 16-bit organic PROM cell arrays were fabricated with the printed organic PMOS transistor and capacitor process. The organic PROM cells were programmed with –50 V, and they were read out with –20 V. The area of the 16-bit organic PROM array was 70.6 $mm^2$.

Table 1. Features of printed organic PROM array.

| | |
|---|---|
| Fabrication process | Printed organic PMOS transistor and capacitor process with printed polymer semiconductor, 3 metal layers |
| Memory organization | 16-bit PROM cells (4×4) |
| Breakdown voltage | –47 V to –40 V for 10 samples |
| Leakage current | 0.1 μA to 0.4 μA @ 0-programmed cells<br>1.5 μA to 10.5 μA @ 1-programmed cells |
| Writing voltage | –50 V |
| Reading voltage | –20 V |
| PROM cell area | 4.41 $mm^2$ (2.1 mm × 2.1 mm) |
| PROM array area (16 cells) | 70.6 $mm^2$ (8.4 mm × 8.4 mm) without PADs<br>132 $mm^2$ (11 mm × 12 mm) with PADs |

## References


[1] E. Cantatore et al, "A 13.56-MHz RFID System Based on Organic Transponders," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, Jan. 2007, pp. 84-92.

[2] K. Myny et al., "A 128b Organic RFID Transponder Chip, Including Manchester Encoding and ALOHA Anticollision Protocol, Operating with a Data Rate of 1529 b/s," *IEEE ISSCC Dig. Tech. Papers*, 2009, pp. 206-207.

[3] K. Myny et al., "Unipolar Organic Transistor Circuits Made Robust by Dual-Gate Technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, May 2011, pp. 1223-1230.

[4] K.-J. Baeg et al., "High-Performance Top-Gated Organic Field-Effect Transistor Memory Using Electrets for Monolithic Printed Flexible NAND Flash Memory," *Adv. Funct. Mater.*, vol. 22, 2012, pp. 2915-2926.

[5] K.-J. Baeg et al., "Polymer Dielectrics and Orthogonal Solvent Effects for High-Performance Inkjet-Printed Top-Gated P-Channel Polymer Field-Effect Transistors," *ETRI J.*, vol. 33, no. 6, Dec. 2011, pp. 887-896.

[6] S.-W. Jung et al., "Low-Voltage-Operated Top-Gate Polymer Thin-Film Transistors with High-Capacitance P(VDF-TrFE)/PVDF-Blended Dielectrics," *Current Appl. Phys.*, vol. 11, 2011, pp. S213-S218.

[7] K.-J. Baeg et al., "Remarkable Enhancement of Hole Transport in Top-Gated N-Type Polymer Field-Effect Transistors by a High-k Dielectric for Ambipolar Electronic Circuits," *Adv. Mater.*, vol.

24, 2012, pp. 5433-5439.
[8] S.-W. Jung et al., "Low-Voltage-Operated Top-Gate Polymer Thin-Film Transistors with High Capacitance Poly(vinylidene fluoride-trifluoroethylene)/Poly(methylmethacrylate) Dielectrics," *J. Appl. Phys*., vol. 108, 2010, pp. 102810:1-102810:5.
[9] S.-W. Jung et al., "Top-Gate Ferroelectric Thin-Film-Transistors with P(VDF-TrFE) Copolymer," *Current Appl. Phys.*, vol. 10, 2010, pp. S58-S61.
[10] S.-M. Yoon et al., "Fully Transparent Non-volatile Memory Thin-Film Transistors Using an Organic Ferroelectric and Oxide Semiconductor Below 200°C," *Adv. Funct. Mater*., vol 20, 2010, pp. 921-926.
[11] G. Gelinck et al., "Organic Transistors in Optical Displays and Microelectronic Applications," *Adv. Mater.*, vol. 22, 2010, pp. 3778-3798.
[12] T. Sekitani et al., "Organic Nonvolatile Memory Transistors for Flexible Sensor Arrays," *Sci.*, vol. 326, 2009, pp. 1516-1519.
[13] P. Heremans et al., "Polymer and Organic Nonvolatile Memory Devices," *Chem. Mater.*, vol. 23, 2011, pp. 341-358.
[14] R.C.G. Naber et al., "High-Performance Solution-Processed Polymer Ferroelectric Field-Effect Transistors," *Nat. Mater*. vol. 4, 2005, pp. 243-248.
[15] Z. Liu et al., "Memory Effect of a Polymer Thin-Film Transistor with Self-Assembled Gold Nanoparticles in the Gate Dielectric," *IEEE Trans. Nanotechnol.*, vol. 5, no. 4, July 2006, pp. 379-384.
[16] J. Kim et al., "Highly Soluble Poly(thienylenevinylene) Derivatives with Charge-Carrier Mobility Exceeding 1 $cm^2V^{-1}s^{-1}$," *Chem. Mater.*, vol. 23, 2011, pp. 4663-4665.
[17] K. Asadi et al., "Organic Non-volatile Memories from Ferroelectric Phase-Separated Blends," *Nat. Mater*., vol. 7, 2008, pp. 547-550.

**Byung-Do Yang** received his BS, MS, and PhD in electrical engineering and computer science from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Rep. of Korea, in 1999, 2001, and 2005, respectively. He was a senior engineer in the Memory Division of Samsung Electronics, Gyeonggi-Do, Rep. of Korea, in 2005, where he was involved in the design of DRAM. Since 2006, he has been at Chungbuk National University, Cheongju, Rep. of Korea. In 2012, he became an associate professor. His research interests are memory circuits, analog circuits, and power IC designs.

**Jae-Mun Oh** received his BE and MS in electronics engineering from Chungbuk National University, Cheongju, Rep. of Korea, in 2010 and 2012. He is currently working toward his PhD in semiconductor engineering. His research interests are analog circuits and power IC designs.

**Hyeong-Ju Kang** received his BS, MS, and PhD in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Rep. of Korea, in 1998, 2000, and 2005, respectively. From 2005 to 2006, he was with Magnachip Semiconductor, where he participated in the development of a smart card controller. From 2006 to 2009, he worked for GCT Semiconductor to develop baseband modem chips for several digital mobile TV standards. Since 2009, he has been an assistant professor in the School of Computer Science and Engineering at Korea University of Technology and Education. His current research interests include communication modem design, embedded processor design, and computer-aided design algorithms for formal verification.

**Soon-Won Jung** received his BS from Youngdong University, Yeongdong, Rep. of Korea, in 1998 and his MS and PhD from Cheongju University, Cheongju, Rep. of Korea, in 2000 and 2004, respectively, all in electronics engineering. From 2006 to 2007, he was a full-time lecturer with the Department of Computer Engineering, Youngdong University. From 2007 to 2009, he was a postdoctoral researcher with ETRI, Daejeon, Rep. of Korea. He is currently a senior researcher with ETRI. He is the author or coauthor of more than 45 peer-reviewed journal papers. His current research interests include the processing and the characterization of printed electronic devices, nonvolatile memory devices, device physics and process technologies for functional devices, and flexible electronics.

**Yong Suk Yang** received his MS and PhD in physics from Pusan National University, Busan, Rep. of Korea, in 1995 and 1999, respectively. In 2001, he joined ETRI, Daejeon, Rep. of Korea, where he has been involved in research on organic and inorganic energy devices. His current research interests include printed electronics and display by inkjet and large area EHD printing technologies.

**In-Kyu You** received his PhD in material science and engineering from Korea University, Seoul, Rep. of Korea, where his research focused on process development, defect modeling, and electrical properties for electronic materials. He joined the Memory Institute of Hyundai Electronics in December 1995 as a principal technical researcher. From 1995 to 1998, he worked as part of the FeRAM team on a FeRAM process integrated device and on PZT ferroelectric thin film development. He joined ETRI, Daejeon, Rep. of Korea, in 1999 and conducted research on and developed a ferroelectric device. Currently, he focuses on printed electronics, such as TFT and memory-based devices. He is a director of the Korea Printed Electronics Association and the Korea Printed Research Association.