

# Preliminary Works of Contact via Formation of LCD Backplanes Using Silver Printing

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**The fabrication of a thin-film transistor backplane and a liquid-crystal display using printing processes can eliminate the need for photolithography and offers the potential to reduce the manufacturing costs. In this study, we prepare contact via structures through a poly(methyl methacrylate) polymer insulator layer using inkjet printing. When droplets of silver ink composed of a polymer solvent are placed onto the polymer insulator and annealed at high temperatures, the silver ink penetrates the interior of the polymer and generates conducting paths between the top and bottom metal lines through the partial dissolution and swelling of the polymer. The electrical property of various contact via-hole interconnections is investigated using a semiconductor characterization system.**

**Keywords: Organic thin-film transistors, inkjet printing, contact via, silver ink, conductivity, penetration, LCD.**

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## I. Introduction

A liquid-crystal display (LCD) is organized into a number of parts, including backlights, polarizers, glass, liquid crystals, and color filters, each of which requires numerous unit processes for their manufacturing [1], [2]. In the early mass production stage, the most striking feature in terms of cost has been the high proportion of material and component costs, reaching approximately 70% to 75% of the total cost amount [3], [4]. As competition in the LCD industry heats up and investments intensify incrementally, panel prices are decreasing. However, a drop in material prices has not caught up with this downward trend. For this reason, the current cost structure is at a price point that is not attractive to consumers. Although innumerable parts account for the bulk of LCD panel costs, LCD panel makers have reached their limit in shaving panel costs by adjusting the price of each part and are therefore placing more focus on methods and technologies to trim panel costs incurred in the manufacturing process [5].

Figure 1(a) shows the typical structure of a thin-film transistor (TFT) backplane for an LCD panel. The pixels of the LCD panel are addressed in rows and columns, and the column and row wires are attached to transistor switches, one for each pixel [3]. The circuit layout process of a TFT-LCD is very similar to that of semiconductor products. The layers of a semiconductor, insulator, and metal for a TFT-LCD are typically formed using the vacuum deposition and photolithography processes, which are costly and difficult to produce.

Because activities to simplify the procedures, heighten the yields, and speed up the manufacturing processes can have a positive impact on the reductions in the production costs of the

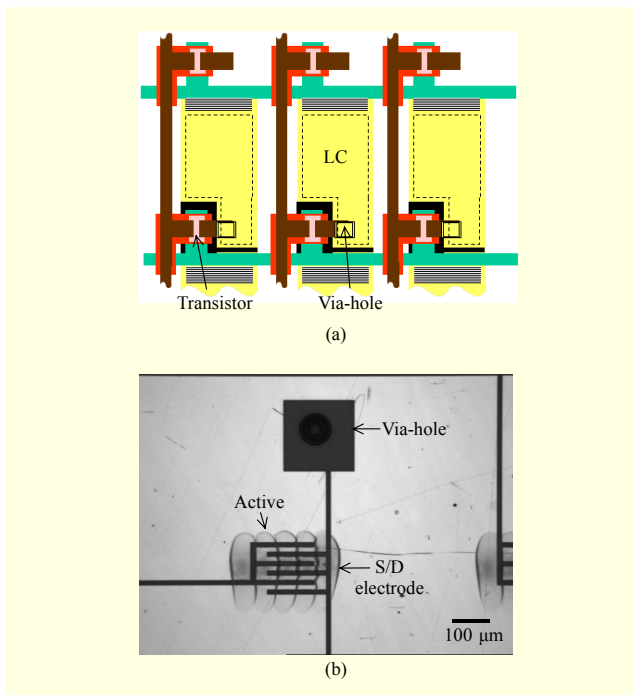


Fig. 1. (a) Top view of LCD backplane and (b) photograph of printed via-hole, active material, and source-drain electrode.

TFT backplane, the interest in LCD display has focused the attention on printing processes, and several printing techniques to pattern electronic parts have been reported [6]-[8]. For printed electronics, contact printing uses a master in a drum or flat plate system, with examples being screen printing, gravure, offset, and micro-contact printing [9]. On the other hand, inkjet printing requires no master, allows digital control of the ejection to provide drop-on-demand (DOD) printing, and is a noncontact process [10]-[12]. Figure 1(b) reveals the typical image of a TFT and via-hole printed on a SiO<sub>2</sub>/Si substrate using inkjet printing.

In 2001, Kawase and others reported that polymer electronic circuits fabricated entirely using a roll-to-roll process have problems with not only TFT devices but also interconnections, via-holes, and resistors [13], [14]. They asserted that the formation of via-holes constitutes a new issue that cannot be solved with the conventional features of inkjet printing because the insulator must be removed locally to achieve a vertical interconnection. They also suggested that via-holes can be created through the selective removal of the poly(vinyl phenol) (PVP) polymer insulator by the inkjet printing of a solvent for the insulator. However, this method has a disadvantage in that it is difficult to apply to various organic insulators and is easy to generate a rough surface of the insulator.

In this paper, we report on the fabrication of contact via-holes by silver printing. The contact via-hole interconnections are

formed during a simple process consisting of inkjet printing of silver ink on a polymer insulator and annealing at a high temperature. To confirm the generation of the via-hole interconnections, we measure the electrical property of metal-insulator-metal capacitors, the transmission image, and the element concentrations. The repeatability of the via-holes is also measured based on the current-voltage ( $I$ - $V$ ) characteristics for 30 samples.

## II. Experimental Methods

Contact via-hole interconnections are developed in a SiO<sub>2</sub> (3,000 Å)/Si wafer, which is prepared as a substrate after cleaning sequentially with acetone and isopropyl alcohol for 10 min during each step and then rinsing with de-ionized water. Au and Cr metals as a bottom electrode are deposited *in situ* on thermally-oxidized silicon using a conventional e-beam evaporator at a pressure of below 10<sup>-4</sup> Pa. Poly(methyl methacrylate) (PMMA, Aldrich, MW=120,000) as a polymer insulator is prepared without further purification. The crosslinking agent, 1,6-bis(trichlorosilyl)hexane (Acro Organics, UK), is purified by distillation under an inert atmosphere. For a 300-nm-thick film, PMMA (80 mg/ml in anhydrous n-butyl acetate) is blended with 1,6-bis(trichlorosilyl) hexane (5 μl); the mixture is then filtered using a 0.1-μm syringe filter and spin-coated at 2,000 rpm onto the substrate. Finally, the PMMA film is annealed on a hot plate at 100°C for 30 min to remove the solvent. All steps are performed in a glove box [15].

The contact via-hole is formed in this structure using an inkjet printing process with conductive silver ink. We use the commercial inks based on organosilver compounds, which are produced by InkTec (Republic of Korea). The silver ink (Ag=15 wt%) consists of organosilver complexes containing carboxylic acid (80%), methanol (15%), and anisole (5%) [16], [17]. An additional 5% of PMMA solvent, dichloromethane (Aldrich, USA), is added to the organosilver ink. The inkjet DOD fabrication of a via-hole array consists of a basic setup utilizing a heated fluid reservoir coupled to a piezoelectric ceramic through which a machined nozzle dispenses uniform polymer droplets onto the substrate mounted to xyz microcontrollers, as illustrated in Fig. 2. The spherical drops, with a diameter of 55 μm, are generated using a Microfab device equipped with a nozzle 50 μm in diameter. The substrate is placed on a movable xyz table, onto which the spherical drops are deposited in a dust-free atmosphere. To achieve an interconnection between the bottom and top electrodes, the droplets of silver ink are precisely dropped onto the PMMA(3000 Å)/Au(1000 Å)/Cr(30 Å)/SiO<sub>2</sub>(3000 Å)/Si area. After the printing, the samples are annealed in a temperature range between 110°C and 170°C for 30 min to

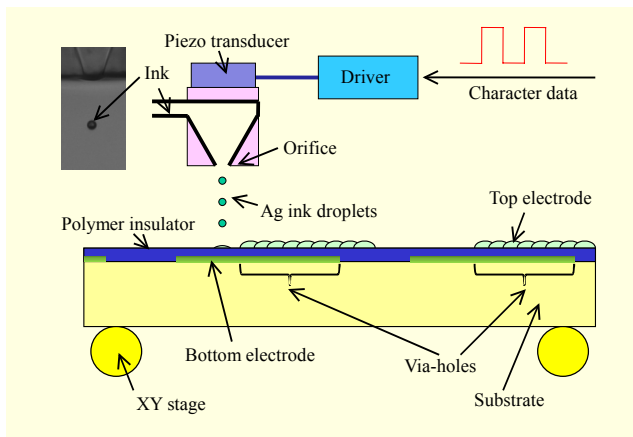


Fig. 2. Schematic image of contact via interconnections produced using inkjet printing method.

remove solvents from the silver film. Finally, Al metal as a top electrode is deposited *in situ* on the printed Ag/PMMA/Au/Cr/SiO<sub>2</sub>/Si samples using an e-beam evaporator at a pressure below 10<sup>-4</sup> Pa.

The electrical property is measured using a semiconductor characterization system (Keithley 4200). The cross-section image and element concentrations are measured using a scanning electron microscope (SEM) and energy dispersive X-ray spectrometry (EDX).

### III. Results and Discussion

In our work, we fabricate an Al/PMMA/Au capacitor with via-hole interconnections using silver ink droplets, as shown in the inset of Fig. 3. The annealing temperature in the via-hole printing process is 150°C for 30 min. Four via-holes are formed in the area overlapping between the Al and Au electrodes. The diameter of each via-hole is approximately 100 μm. Figure 3 shows the *I-V* characteristics of Al/PMMA/Au capacitors with or without via-hole interconnections, which are tested at room temperature and ambient pressure. The *I-V* curve for the Al/PMMA/Au capacitor without via-hole interconnections represents the insulating property of the PMMA polymer precisely, and the leakage current is below 0.15 pA at a voltage of ±1 V. The *I-V* curve for the sample with via-hole interconnections indicates the behavior of a short circuit, as shown in the inset of Fig. 3. In this result, the excessive electric current is limited by the compliance of the semiconductor characterization system.

Figures 4(a) through 4(d) show the cross-sectional images of an Al/printed Ag/PMMA/Au capacitor annealed at various temperatures during the via-hole process. The cross-sections are prepared through ion beam milling utilizing a focused ion beam (FIB), and the images are observed using an SEM. The

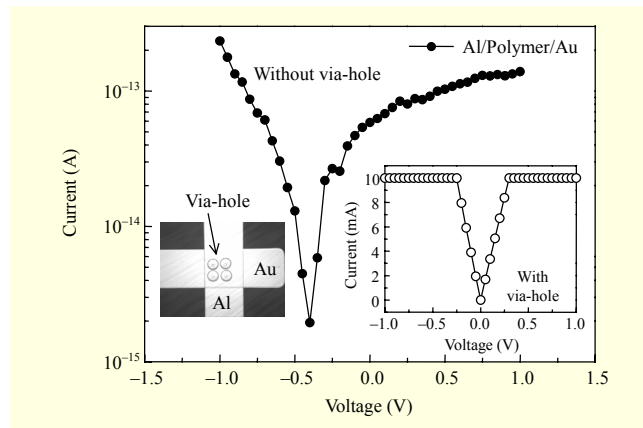


Fig. 3. *I-V* characteristics of Al/PMMA/Au capacitors with or without via-hole interconnections. Inset is photograph of Al/PMMA/Au capacitor with via-hole interconnections using silver ink droplets. Compliance current is 10 mA.

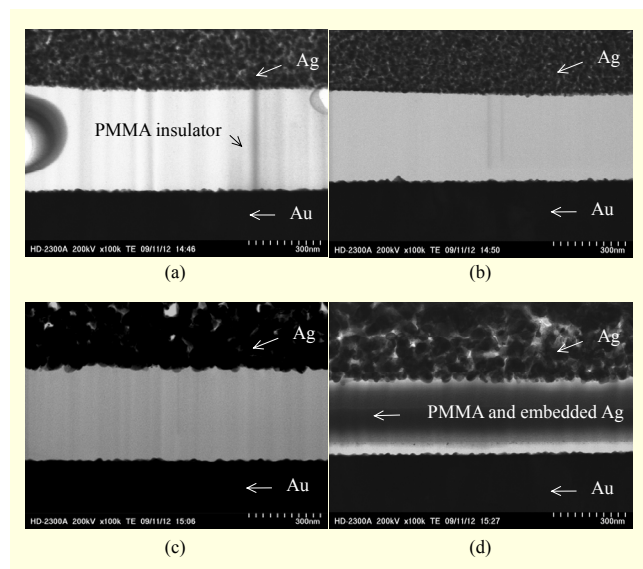


Fig. 4. Cross-sectional SEM images of Al/printed Ag/PMMA/Au capacitor annealed at (a) 110°C, (b) 130°C, (c) 150°C, and (d) 170°C for 30 min.

samples reflected in Figs. 4(a) through 4(d) are annealed at temperatures of 110°C, 130°C, 150°C, and 170°C for 30 min, respectively. In the FIB-SEM images, three shaded regions are observed. The top layer is the printed Ag layer, which displays a dark gray color. As the annealing temperature increases, more densely packed silver layers are observed. The middle layer is a PMMA polymer insulator, which is smooth and a light gray color, as shown in Fig. 4(a). However, when the annealing temperature increases, the thickness of the PMMA decreases and the color changes from light gray to dark gray. The bottom layer is the evaporated Au layer of another dark gray color. EDX studies over the dark gray region indicate the presence of metal ingredients, such as silver and gold.

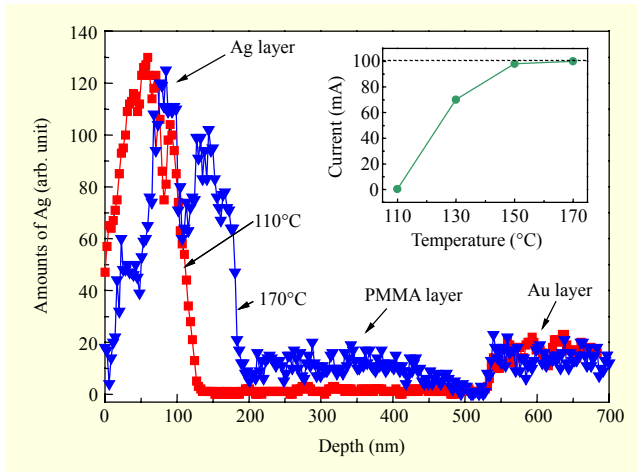


Fig. 5. Depth profiles of silver components in Al/printed Ag/PMMA/Au capacitors measured by EDX. Inset is current at  $V=0.3$  V for samples annealed at 110°C and 170°C for 30 min. Compliance current is 100 mA.

Figure 5 reveals the depth profiles of silver components in Al/printed Ag/PMMA/Au capacitors measured by EDX. The samples are annealed at temperatures of 110°C, 130°C, 150°C, and 170°C for 30 min after the inkjet printing of Ag ink on the PMMA. The region of the Ag, PMMA, and Au layers is distinguished well. The silver amount in the bottom electrode does not necessarily imply a measurement/interpretation error but could actually originate from the porosity of evaporated Au electrodes as used in the experiments. As the annealing temperature increases, the amount of embedded Ag in PMMA increases, and the PMMA then becomes metallic in the area of the via-holes. This result indicates that the color change of PMMA to dark gray may be attributed to an increase in the embedded Ag nanoparticles (NPs) in the PMMA polymer insulator. On the other hand, the EDX analysis of the light gray region in the PMMA indicates a few Ag components. The current at  $V=0.3$  V for the samples annealed within the temperature range between 110°C and 170°C for 30 min are given in the inset of Fig. 5. The compliance current is 100 mA, and the area of via-holes is approximately  $3.14 \times 10^4 \mu\text{m}^2$ . As the annealing temperature is increased, the leakage current of the samples increases to the compliance current. This result indicates that the conducting path through the PMMA insulator might be made during the inkjet printing and annealing processes at a high temperature. In particular, the solvents in Ag ink might play an important role in the embedding of Ag NPs into the PMMA materials by the partial dissolution and swelling of the polymer film. Figure 6 shows a schematic diagram of the Ag NPs and the conducting filament path through the PMMA insulator. Both the penetration of the Ag NPs and the formation of a conducting filament path in the polymer insulator are significant in making a printed via-hole.

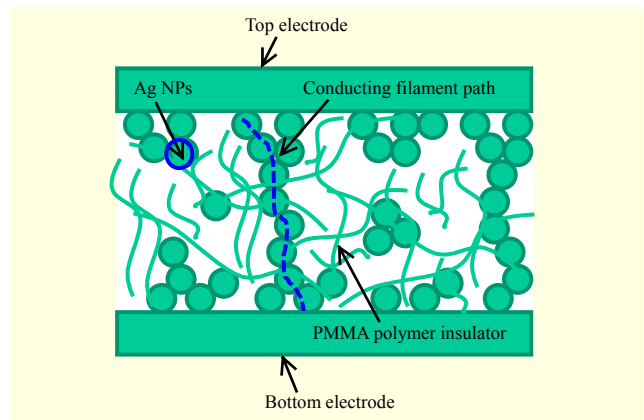


Fig. 6. Schematic diagram of Ag NPs and conducting filament path through PMMA insulator.

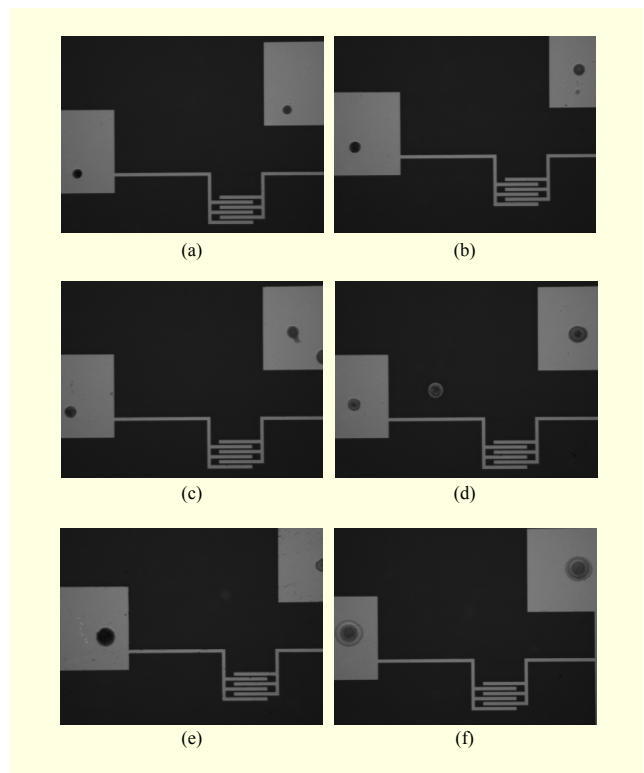


Fig. 7. Optical microscope images of via-hole samples printed using various jetting voltages. Measured sizes of via-holes are approximately (a) 45  $\mu\text{m}$ , (b) 60  $\mu\text{m}$ , (c) 65  $\mu\text{m}$ , (d) 75  $\mu\text{m}$ , (e) 85  $\mu\text{m}$ , and (f) 130  $\mu\text{m}$ .

To increase the integration of printed electronic devices, it is important to reduce the size of the via-holes. Figures 7(a) through 7(f) show optical microscope images of the via-hole samples printed according to various jetting voltages. The operating frequency is 1 kHz and the duty of pulse voltage is half in a cycle. The distance between nozzle and substrate is approximately 0.5 mm, and the temperature is room temperature. The minimum pulse voltage for ejecting the silver



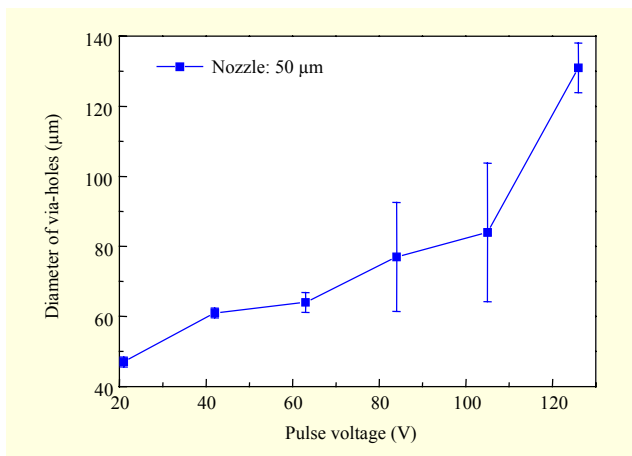


Fig. 8. Plot of pulse voltage dependence of via-hole diameter.

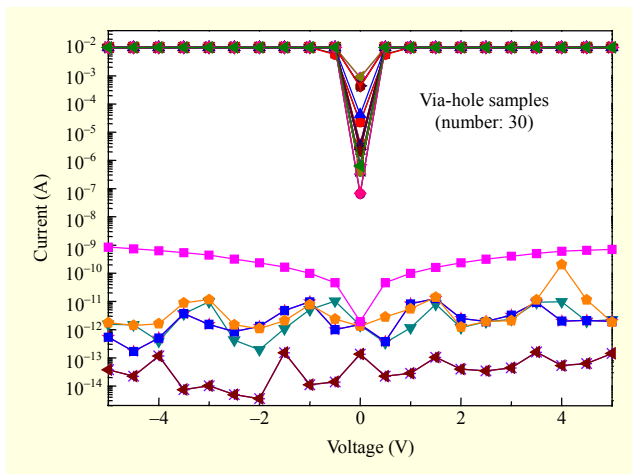


Fig. 9. Plot of current vs. voltage for thirty samples.

ink is approximately 21 V, below which a droplet cannot be formed or ejected. The via-hole result observed at the minimum pulse voltage is shown in Fig. 7(a). The diameter of the via-hole is approximately 45  $\mu\text{m}$ . Figure 8 shows the jetting pulse voltage dependence of the average and standard deviation of diameter of the via-holes. When the jetting voltage increases, both the magnitude and the variation of the diameter increases. At a higher jetting voltage, the droplets from the nozzle have a faster speed but are very irregular in size and direction.

To obtain the repeatability of the printed via-holes, we fabricate thirty Al/printed Ag/PMMA/Au capacitors after the via-hole process and measure the  $I$ - $V$  curves repeatedly. The ramp rate is 20 mV/s. Figure 9 shows a plot of the current versus voltage, which contains all results of the thirty samples. Only the  $I$ - $V$  curves of five samples do not show a normal conducting path property. Eventually, the measured yield of the via-holes is approximately 83.3%.

## IV. Conclusion

In this study, we investigated the fabrication of contact via interconnections in a PMMA polymer insulator and their electric characteristics using  $I$ - $V$  measurements. The DC conductivity of Al/printed Ag/PMMA/Au capacitors was measured for various annealing temperatures. When the annealing temperature increased, the amount of embedded Ag in the PMMA increased and the current of the samples increased to compliance. This result indicates that a conducting path for Ag NPs through the PMMA layer may have been made during the inkjet printing and annealing at a high temperature of above 150°C. The yield obtained in the experiment was approximately 83.3% of the electrical repeatability.

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